Migrating Designs Between IGLOO2 M2GL025 and M2GL050 in the FCS325 Package

Table of Contents

Introduction

This document describes how to migrate designs within the IGLOO®2 field programmable gate array (FPGA) device family between the M2GL025 and M2GL050 devices within the FCS325 package. It addresses restrictions and specifications that need to be considered when moving a design between these devices. This includes pin compatibility between the devices, design and device resources evaluation, I/O banks, standards, and so on. This document also describes the software flow behavior during the migration.

Design Migration

The IGLOO2 FPGA family devices are architecturally compatible with each other. However, attention must be paid to some key areas while migrating a design from one device to another. Following are the specific topics that are discussed in this document:

- Design and Device Evaluation
- I/O Banks and Standards
- Pin Migration and Compatibility
- Power Supply and Board-Level Considerations
- Software Flow

Design and Device Evaluation

One of the initial and main tasks while migrating a design should be to compare the available resources between the two devices. The device resources can be grouped into three different categories:

- High-Performance Memory Subsystem
- Fabric Resources
- On-Chip Oscillators

In addition, necessary design timing analysis and simulations should be performed while migrating designs from one device to another. Each of the following sections focuses on the different aspects of the design and device evaluation categories.

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High-Performance Memory Subsystem

Table 1 provides a high-level summary of the differences between the M2GL025 and M2GL050 high-performance memory subsystem (HPMS) blocks. Based on the different HPMS resources and features, migration from one device to another can be planned to avoid any resource conflicts or issues.

Table 1 • **HPMS Features Per Package or Device**

Feature	FCS325 Package	
	M2GL025 and M2GL025T	**M2GL050 and M2GL050T**
Fabric interfaces (FIC)	1 (FIC_0)	2 (FIC_0 and FIC_1)
Memory subsystem DDR (MDDR)	x18[1]	x18[2]
eNVM (kbytes)	256	256
eSRAM (kbytes)	64	64
eSRAM (non-SECDED) (kbytes)	80	80
SPI, HPDMA, PDMA	1	1

Notes:

1. *DDR supports x18, x16, x9, and x8 modes*
2. *DDR supports x18 and x16 modes*

Fabric Resources

Table 2 gives a high-level summary of the differences between the M2GL025 and M2GL050 fabric resources. Based on the differences, effective logic count, RAM size, and number of I/Os migration can be evaluated and planned from one device to another without any resource conflicts or issues.

Table 2 • **Summary of the Fabric Features Supported Per Device**

Fabric Features (Logic, DSP, and Memory)		FCS325 Package	
		M2GL025 and M2GL025T	**M2GL050 and M2GL050T**
Logic/DSP	Logic Modules (4-Input LUT)	27,696	56,340
	Mathblocks	34	72
	PLLs and CCCs	6	6
Fabric Memory	LSRAM 18K blocks	31	69
	uSRAM 1K blocks	34	72
User I/Os	MSIO (3.3 V max)	94	90
	MSIOD (2.5 V max)	22	22
	DDRIO (2.5 V max)	64	88
	Total user I/Os per package	180	200

On-Chip Oscillators

Table 3 shows the summary of IGLOO2 FPGA on-chip oscillators that are the primary sources for generating free-running clocks.

Table 3 • **On-Chip Oscillator Support Per Device**

Feature	FCS325 Package	
	M2GL025	M2GL050
1 MHz RC oscillator	1	1
50 MHz RC oscillator	1	1
Main crystal oscillator (32 KHz–20 MHz)	1	1

Refer to the *IGLOO2 Clocking Resources User's Guide* for more information.

I/O Banks and Standards

IGLOO2 FPGA I/Os are partitioned into multiple I/O voltage banks. The number of banks depends on the device. There are seven I/O banks in the M2GL025 device and eight I/O banks in the M2GL050 device. Table 4 shows a summary of organization of the I/O banks between the M2GL025 and M2GL050 FPGA devices.

Table 4 • **Organization of the I/O Banks in IGLOO2 FPGA Devices**

I/O Banks	FCS325 Package	
	M2GL025T	M2GL050T
Bank 0	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	MSIO: Fabric	MSIO: Fabric
Bank 2	MSIO: Fabric	MSIO: Fabric
Bank 3	MSIO: JTAG	MSIO: Fabric
Bank 4	MSIO: Fabric	MSIO: JTAG
Bank 5	MSIOD: SERDES_0 or fabric	DDRIO: Fabric
Bank 6	MSIO: Fabric	MSIOD: SERDES_0 or fabric
Bank 7	MSIO: Fabric	MSIOD: Fabric
Bank 8	–	MSIO: Fabric

Package pins VDDIx are the bank power supplies where x indicates the bank number. For example, VDDI0 is bank0 power supply. Figure 1 IGLOO2 FPGA M2GL050T FCS325 I/O Bank Locations and Figure 2 on page 5, IGLOO2 FPGA M2GL025T FCS325 I/O Bank Locations show the different I/O bank locations and numbers per device in the FCS325 package.

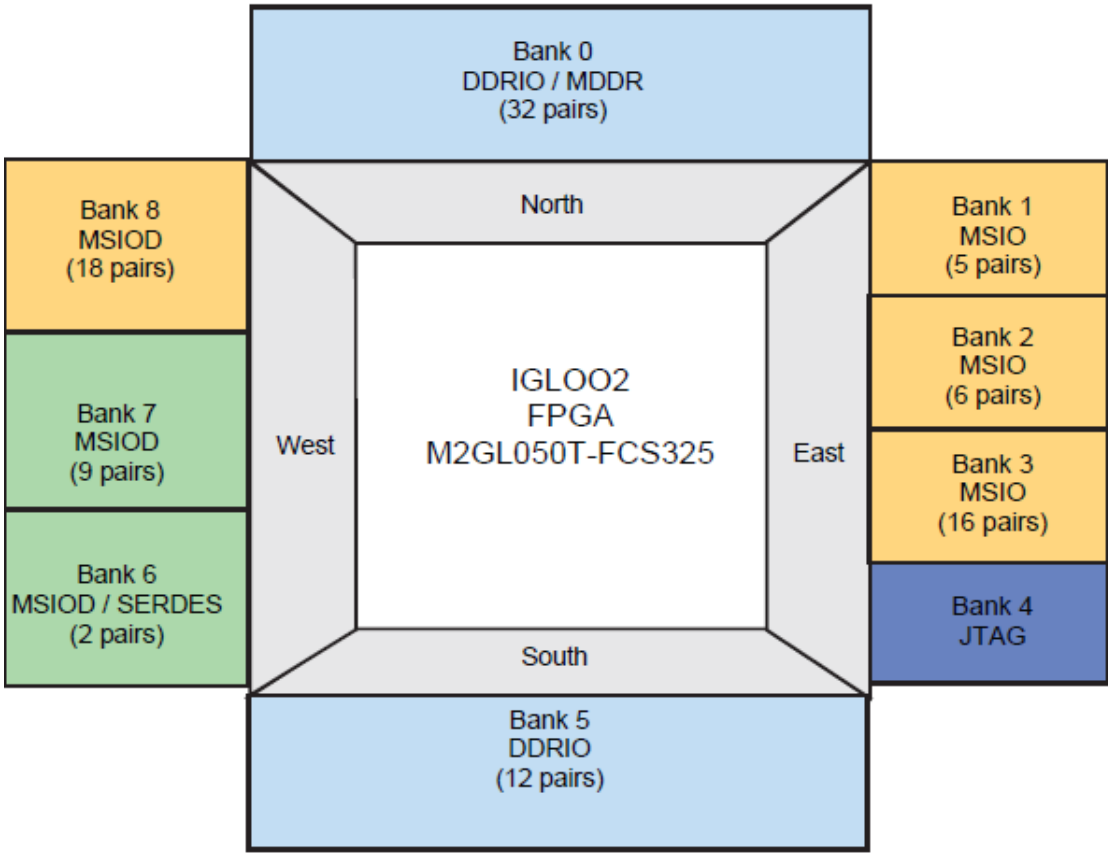

***Figure 1* • IGLOO2 FPGA M2GL050T FCS325 I/O Bank Locations**

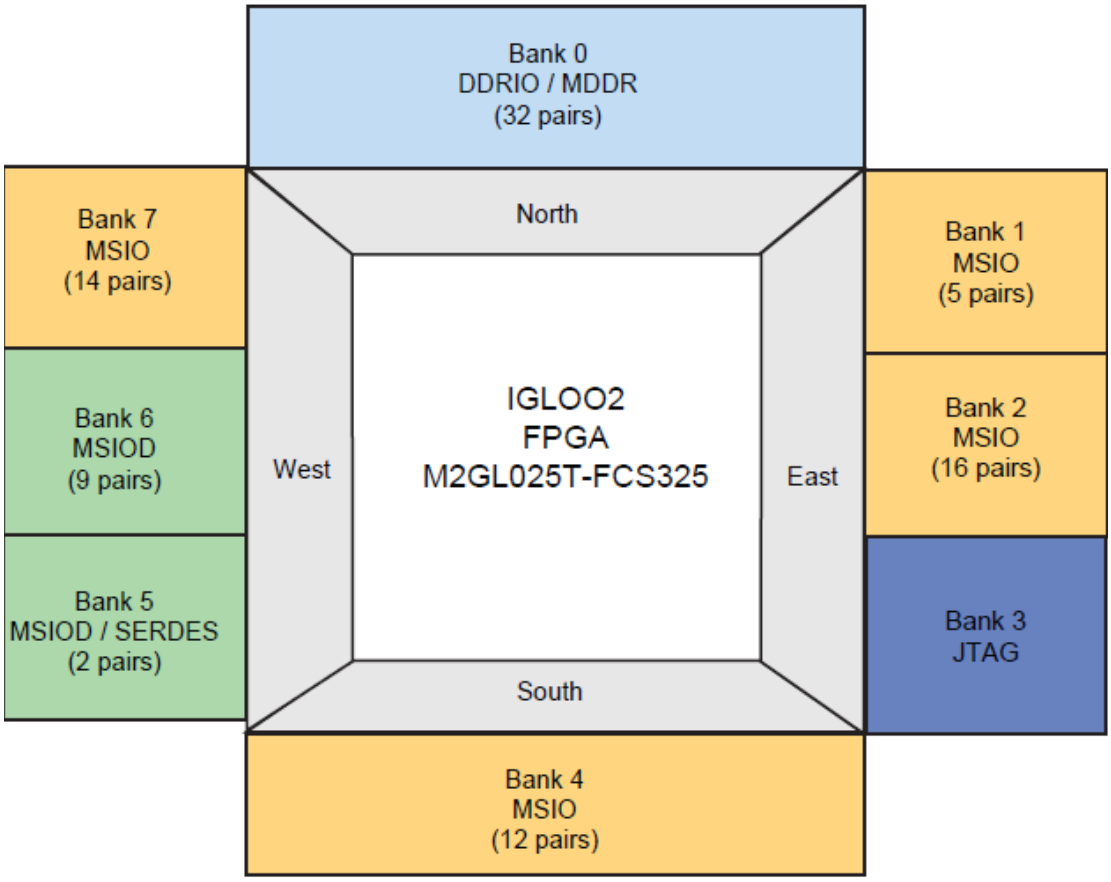

***Figure 2* • IGLOO2 FPGA M2GL025T FCS325 I/O Bank Locations**

An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V standards. MSIOD or DDRIO bank supports 1.2 V, 1.5 V, 1.8 V, or 2.5 V standards. The 3.3 V is not supported for MSIOD or DDRIO I/Os. For more details on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, refer to the "Supported Voltage Standards" table in the IGLOO2 FPGA Fabric User's Guide.

Pin Migration and Compatibility

Although the IGLOO2 FPGA devices and packaging have been designed to allow footprint compatibility for smoother migration, some of the pins have a reduced compatibility feature set between the M2GL025 and M2GL050 devices in the FCS325 package. This section addresses the different aspects of the pin compatibility. The differences can be grouped into the following categories:

- Global Versus Regular Pins
- Available Versus No Connect Pins
- I/Os Technology Compatibility Per Pin or Bank
- Probe Pins

Global Versus Regular Pins

When migrating designs between IGLOO2 FPGA devices, it is important to evaluate the different types of pins that are available per device. The functionality of the same pin can be different between devices. This section focuses on highlighting and comparing the global pins in one device against the other devices. Therefore, migration can be evaluated and planned from one device to another without any resource conflicts or issues.

- Moving from a device, where the I/O is a global pin to a device where the same I/O is a regular pin. In this case, replace the global clock (for example, CLKBUF) with a regular input buffer (for example, INBUF) and then internally promote the signal to a global resource using a CLKINT or synthesis options.
- Moving from a device, where the I/O is a regular pin to a device where the same I/O is a global pin. In this case, replace the INBUF with a CLKBUF or keep the INBUF and internally promote the signal to a global using a CLKINT or synthesis options.

Table 5 provides a comparison between the global pins available in the M2GL025 and M2GL050 devices. The unused global pins are configured as inputs with pull-up resistors by the Libero® System-on-Chip (SoC) software.

For more information, refer to the "FPGA Fabric Global Network Architecture" chapter of the *IGLOO2 Clocking Resources User's Guide*.

Table 5 • **Non-Equivalent Global Pins Comparison Per Device**

Package Pins	FCS325 Pin Names			
	M2GL025	**Bank No**	**M2GL050**	**Bank No**
A18	DDRIO61PB0/**CCC_NW1_CLKI3**	0	DDRIO88PB0	0
AA10	MSIO120NB4/CCC_SW0_CLKI2	4	**DDRIO**147NB5/CCC_SW0_CLKI2	5
R8	MSIO134PB4/VCCC_SE1_CLKI	4	**DDRIO**164PB5/VCCC_SE1_CLKI	5
E15	DDRIO62PB0/MDDR_DQ_ECC1	0	DDRIO87PB0/MDDR_DQ_ECC1/**CCC_NW1_CLKI3**	0
U10	MSIO131PB4/GB11/VCCC_SE0_CLKI	4	**DDRIO**161PB5/GB11/VCCC_SE0_CLKI	5
U11	MSIO125PB4/GB3/CCC_SW0_CLKI3	4	**DDRIO**152PB5/GB3/CCC_SW0_CLKI3	5
U12	MSIO125NB4/GB7/CCC_SW1_CLKI2	4	**DDRIO**152NB5/GB7/CCC_SW1_CLKI2	5
W11	MSIO129PB4/CCC_SW1_CLKI3	4	**DDRIO**159PB5/CCC_SW1_CLKI3	5
Y8	MSIO133PB4/GB15/VCCC_SE1_CLKI	4	**DDRIO**163PB5/GB15/VCCC_SE1_CLKI	5
Y9	MSIO130PB4/VCCC_SE0_CLKI	4	**DDRIO**160PB5/VCCC_SE0_CLKI	5

Table 6 shows the list of global pins that are similar between the two devices.

Table 6 • **Equivalent Global Pins Per Device**

Package Pins	FCS325 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
B20	DDRIO66NB0/CCC_NW0_CLKI2	0	DDRIO92NB0/CCC_NW0_CLKI2	0
B9	DDRIO49PB0/CCC_NE1_CLKI3/MDDR _DQ14	0	DDRIO75PB0/CCC_NE1_CLKI3/MDDR _DQ14	0
C11	DDRIO52PB0/GB8/CCC_NE0 _CLKI3/MDDR_DQS1	0	DDRIO78PB0/GB8/CCC_NE0_CLKI3/MDDR _DQS1	0
C16	DDRIO65NB0/GB4/CCC_NW1_CLKI2	0	DDRIO91NB0/GB4/CCC_NW1_CLKI2	0
D1	MSIO28PB1/GB14/VCCC_SE1_CLKI	1	MSIO42PB1/GB14/VCCC_SE1_CLKI	1
D16	DDRIO65PB0/GB0/CCC_NW0_CLKI3	0	DDRIO91PB0/GB0/CCC_NW0_CLKI3	0
D9	DDRIO50PB0/GB12/CCC_NE1 _CLKI2/MDDR_DQ12	0	DDRIO76PB0/GB12/CCC_NE1 _CLKI2/MDDR_DQ12	0
E11	DDRIO53PB0/MDDR_DQ10/CCC_NE0 _CLKI2	0	DDRIO79PB0/MDDR_DQ10/CCC_NE0 _CLKI2	0
F1	MSIO27PB1/GB10/VCCC_SE0_CLKI	1	MSIO41PB1/GB10/VCCC_SE0_CLKI	1
F2	MSIO26PB1/CCC_NE1_CLKI1	1	MSIO40PB1/CCC_NE1_CLKI1	1
G2	MSIO25PB1/CCC_NE0_CLKI1	1	MSIO39PB1/CCC_NE0_CLKI1	1
K17	MSIO99PB7/CCC_NW0_CLKI0	7	MSIO117PB8/CCC_NW0_CLKI0	8
L17	MSIO98PB7/CCC_NW1_CLKI0	7	MSIO116PB8/CCC_NW1_CLKI0	8
L19	MSIO96PB7/GB6/CCC_NW1_CLKI1	7	MSIO114PB8/GB6/CCC_NW1_CLKI1	8
L20	MSIO97PB7/GB2/CCC_NW0_CLKI1	7	MSIO115PB8/GB2/CCC_NW0_CLKI1	8
N17	MSIOD103PB6/CCC_SW0_CLKI0	6	MSIOD121PB7/CCC_SW0_CLKI0	7
N18	MSIOD102PB6/CCC_SW1_CLKI0	6	MSIOD120PB7/CCC_SW1_CLKI0	7
N2	MSIO20NB2/GB13/VCCC_SE1_CLKI	2	MSIO20NB3/GB13/VCCC_SE1_CLKI	3
P1	MSIO20PB2/GB9/VCCC_SE0_CLKI	2	MSIO20PB3/GB9/VCCC_SE0_CLKI	3
P21	MSIOD100PB6/GB5/CCC_SW1_CLKI1	6	MSIOD118PB7/GB5/CCC_SW1_CLKI1	7
R21	MSIOD101PB6/GB1/CCC_SW0_CLKI1	6	MSIOD119PB7/GB1/CCC_SW0_CLKI1	7
R4	MSIO11PB2/CCC_NE0_CLKI0	2	MSIO11PB3/CCC_NE0_CLKI0	3
R5	MSIO11NB2/CCC_NE1_CLKI0	2	MSIO11NB3/CCC_NE1_CLKI0	3

Refer to the "Dedicated Global I/O Naming Conventions" section in the *IGLOO2 Pin Descriptions*.

Available Versus No Connect Pins

There are pins that have specific functions in one device while those same pins are "no connect" (NC) in the other device. Table 7 lists the summary of these pins.

When moving from a device (where the I/O is an NC pin to a device where the I/O has a defined functionality and is not used) follow the recommended methods for connecting the unused I/Os, depending on the functionality of that I/O. Refer to "Unused Pin Configurations" in the *IGLOO2 Board Design Guidelines Application Note*.

When moving from a device (where the I/O has a defined functionality to a device where the I/O is an NC) then the NC pins can be driven to any voltage or can be left floating with no effect on the operation of the device. NC indicates that the pin is not connected to circuitry within the device.

Table 7 • **Available Versus NC Pins**

Package Pins	FCS325 Pin Names		
	M2GL025	M2GL050	Bank No
E20	NC	MSIO99NB8	8
E21	NC	MSIO99PB8	8
G18	NC	MSIO106NB8	8
H17	NC	MSIO106PB8	8
H2	NC	MSIO37NB2	2
H4	NC	MSIO34NB2	2
H5	NC	MSIO34PB2	2
J1	NC	MSIO37PB2	2
J2	NC	MSIO32NB2	2
J4	NC	MSIO29PB2	2
J5	NC	VDDI2	
K1	NC	MSIO32PB2	2
K2	NC	MSIO29NB2	2
K21	NC	MSIO111PB8	8
K4	NC	MSIO25NB2	2
K5	NC	MSIO25PB2	2
K7	NC	MSIO26NB2	2
L21	NC	MSIO111NB8	8
L7	NC	MSIO26PB2	2
N20	NC	MSIO112PB8	8
N21	NC	MSIO112NB8	8
R11	NC	VREF5	

I/Os Technology Compatibility Per Pin or Bank

Table 8 shows the list of I/Os that would lead to incompatibility with the different technology support while migrating between the M2GL025 and M2GL050 within the FCS325 package. The difference is the type of I/O technology (MSIO versus DDRIO) that is supported on those regular I/Os.

Table 8 • **I/O Standards Compatibility Per Device or Package Pins**

Package Pins	FCS325 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
AA10	MSIO120NB4/CCC_SW0_CLKI2	4	**DDRIO**147NB5/CCC_SW0_CLKI2	5
AA11	MSIO121NB4/PROBE_B	4	**DDRIO**148NB5/PROBE_B	5
AA6	MSIO145PB4	4	**DDRIO**186PB5	5
AA7	MSIO145NB4	4	**DDRIO**186NB5	5
AA8	MSIO130NB4	4	**DDRIO**160NB5	5
R8	MSIO134PB4/VCCC_SE1_CLKI	4	**DDRIO**164PB5/VCCC_SE1_CLKI	5
R9	MSIO134NB4	4	**DDRIO**164NB5	5
U10	MSIO131PB4/GB11/VCCC_SE0_CLKI	4	**DDRIO**161PB5/GB11/VCCC_SE0_CLKI	5
U11	MSIO125PB4/GB3/CCC_SW0_CLKI3	4	**DDRIO**152PB5/GB3/CCC_SW0_CLKI3	5
U12	MSIO125NB4/CCC_SW1_CLKI2	4	**DDRIO**152NB5/CCC_SW1_CLKI2	5
U8	MSIO137PB4	4	**DDRIO**172PB5	5
U9	MSIO137NB4	4	**DDRIO**172NB5	5
V10	MSIO131NB4	4	**DDRIO**161NB5	5
V11	MSIO129NB4	4	**DDRIO**159NB5	5
V6	MSIO142NB4	4	**DDRIO**184NB5	5
V7	MSIO140PB4	4	**DDRIO**177PB5	5
V8	MSIO140NB4	4	**DDRIO**177NB5	5
W11	MSIO129PB4/CCC_SW1_CLKI3	4	**DDRIO**159PB5/CCC_SW1_CLKI3	5
W6	MSIO142PB4	4	**DDRIO**184PB5	5
Y10	MSIO120PB4	4	**DDRIO**147PB5	5
Y11	MSIO121PB4/PROBE_A	4	**DDRIO**148PB5/PROBE_A	5
Y7	MSIO133NB4	4	**DDRIO**163NB5	5
Y8	MSIO133PB4/GB15/VCCC_SE1_CLKI	4	**DDRIO**163PB5/GB15/VCCC_SE1_CLKI	5
Y9	MSIO130PB4/VCCC_SE0_CLKI	4	**DDRIO**160PB5/VCCC_SE0_CLKI	5

The DDRIOs do not support single-ended 3.3 V I/O standards and differential LVPECL, LVDS 3.3 V, LVDS 2.5 V, RSDS BLVDS, MLVDS, and Mini-LVDS I/O standards, as shown in Table 9. To migrate from M2GL025 to M2GL050 successfully, ensure that the correct VDDI power supply is used to power the equivalent banks. Only I/Os with compatible standards can be assigned to the same bank.

Table 9 • **Technology Support Difference Between I/O Types**

I/O Standards	I/O Types	
	MSIO	**DDRIO**
Single-Ended I/O		
LVTTL 3.3 V	Yes	–
LVCMOS 3.3 V	Yes	–
PCI	Yes	–
LVCMOS 1.2 V	Yes	Yes
LVCMOS 1.5 V	Yes	Yes
LVCMOS 1.8 V	Yes	Yes
LVCMOS 2.5 V	Yes	Yes
Voltage-Referenced I/O		
HSTL1.5 V	Yes	Yes
SSTL1.8	Yes	Yes
SSTL 2.5	Yes	Yes
SSTL 2.5 V(DDR1)	Yes	Yes
SSTL 1.8 V(DDR2)	Yes	Yes
SSTL 1.5 V (DDR3)	Yes	Yes
Differential I/O		
LVPECL (input only)	Yes	–
LVDS 3.3 V	Yes	–
LVDS 2.5 V	Yes	–
RSDS	Yes	–
BLVDS	Yes	–
MLVDS	Yes	–
Mini-LVDS	Yes	–

Note: Even though the VDDI might be the same (for example, MSIO 2.5 V and DDRIO 2.5 V), the attributes and features supported might be different between different I/O types (MSIO versus DDRIO). Refer to the "I/O Programmable Features" section in the *IGLOO2 FPGA Fabric User's Guide* for more information on the list of features supported per I/O type.

Probe Pins

Probe pins package locations are compatible between the two devices, but the I/O technology that is supported on these pins is different (MSIO versus DDRIO). Refer to "I/Os Technology Compatibility Per Pin or Bank" section on page 9 for more information. Table 10 shows the different probe I/Os location per device within the FCS325 package.

By default, probe pins are reserved for the probe functionality. Unreserve these pins by **clearing the Reserve Pins for Probes** check box in the Device I/O Settings under Project Setting in the Libero SoC. When the pins are not reserved, the probe I/Os can be used as regular I/Os.

Table 10 • **Probe Pins Per Device**

Package Pins	FCS325 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
AA11	**MSIO**121NB4/PROBE_B	4	**DDRIO**148NB5/PROBE_B	5
Y11	**MSIO**121PB4/PROBE_A	4	**DDRIO**148PB5/PROBE_A	5

Power Supply and Board-Level Considerations

I/O power supply requirements are one of the key aspects to consider for design migrations. Since the migration is within the IGLOO2 FPGA family, there is no issue regarding the core voltage (VDD), charge pumps voltage (VPP), and the analog sense circuit supply of the eNVM voltage (VPPNVM). The ground pins (VSS) are also equivalent between the M2GL025 and M2GL050 devices. Refer to the *IGLOO2 Pin Descriptions* for more details. The bank supply voltages VDDI pins must be connected appropriately. All the bank supplies that are located on the east-side must be powered even if the associated bank I/Os are not used. Refer to the "Recommendation for Unused Bank Supplies" connections table in the *IGLOO2 Board Design Guidelines Application Note* for more information in the case where the specific banks are not used. An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltages and an MSIOD and DDRIO bank supports 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, refer to the "Supported Voltage I/O Standards" table in the *IGLOO2 FPGA Fabric User's Guide*.

The banks have dedicated supplies. Therefore, only I/Os with compatible voltage standards can be assigned to the same I/O voltage bank. The correct bank supply must be used when migrating between the different devices per the appropriate voltages (I/O Standards) selected for the bank.Table 11 shows the different banks power supply compatibility per device in the FCS325 package.

***Table 11* • None Equivalent Power Supplies Per Device**

Package Pins	FCS325 Pin Names	
	M2GL025	M2GL050
AA9	VDDI4	VDDI5
D20	VDDI7	VDDI8
F17	VDDI7	VDDI8
J15	VDDI7	VDDI8
J5	NC	VDDI2
K20	VDDI7	VDDI8
M2	VDDI2	VDDI3
N15	VDDI6	VDDI7
N5	VDDI2	VDDI3
R10	VDDI4	VDDI5
R18	VDDI6	VDDI7
V2	VDDI2	VDDI3
V5	VDDI3	VDDI4
V9	VDDI4	VDDI5
W20	VDDI5	VDDI6

For the other bank supplies that are equivalent, refer to the provided recommendations in the *IGLOO2 Pin Descriptions*.

Any other board-level considerations are common among the two devices. Refer to the *IGLOO2 Board Design Guidelines Application Note* for more details.

Software Flow

The Libero SoC provides the option of reserving pins for moving between different devices within the IGLOO2 FPGA family, where pins within the current device that are not bonded in the destination device can be automatically reserved.

This option is available in the I/O Constraints Editor which can be accessed from the Design Flow window, as shown in Figure 3 on page 13. This is done in the very early stages of the design cycle.

Pins can be reserved as follows:

1. After finishing the Compile stage, select the **I/O Constraints** option from the Design Flow window, as shown in Figure 3.

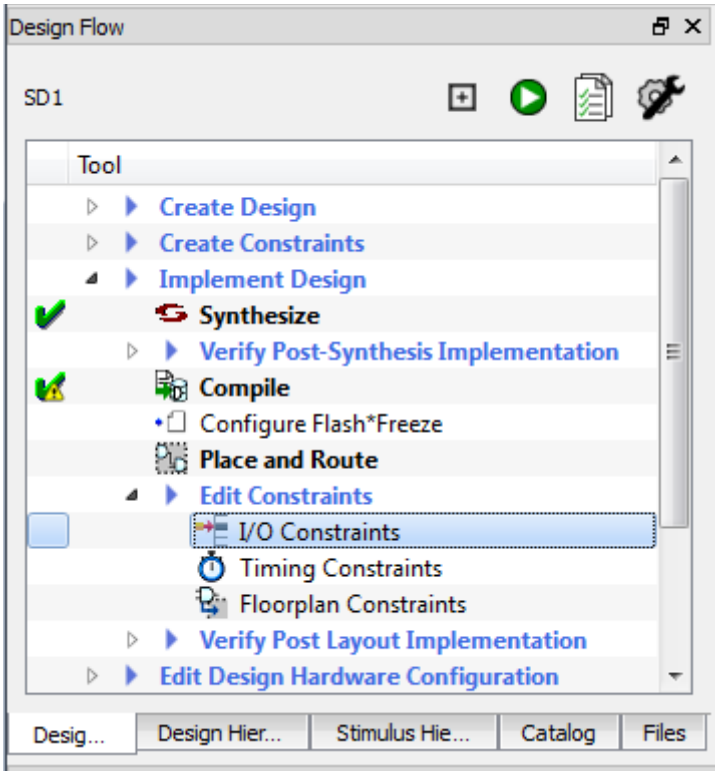

***Figure 3* • I/O Constraint Editor Option part of the Design Flow**

2. Select the **Reserve Pins for Device Migration** option from the Tools menu. The window shown in Figure 4 is displayed.

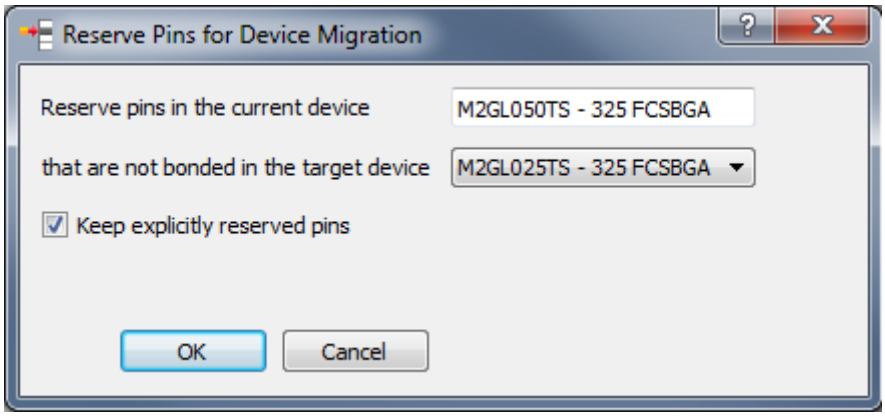

***Figure 4* • Reserve Pins for Device Migration**

The first option shows the device that is currently being used in the Libero SoC project. From the drop-down menu, select the device that is eventually migrated to as the target device. Refer to the Libero SoC software online help for more details on this window and options.

The Libero SoC software provides the option of moving between different devices within the IGLOO2 FPGA family by changing from M2GL025 to M2GL050 and vice-versa using the Project Settings option in the Libero SoC software. Upon changing the device, the Libero SoC validates the features that are used within the design against the supported features within the new targeted device and package. Feedback messages are provided as part of the Libero SoC software flow, listing the different actions taken by Libero SoC and the action required.

The first step that Libero SoC performs upon changing the device, is to invalidate the original design components and the design flows. The message is displayed as shown in Figure 5.

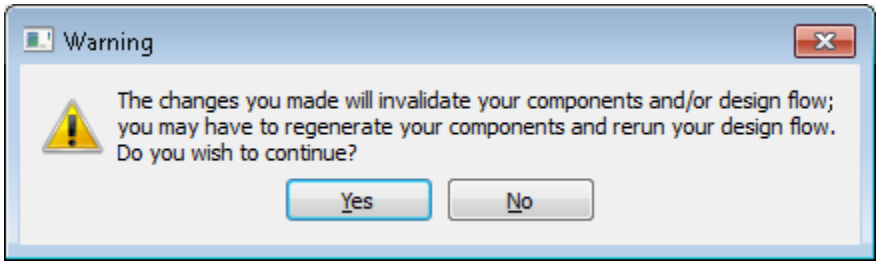

***Figure 5* • Invalidating Component and Design Flow Message**

As part of rerunning the design flow, the Libero SoC checks the different steps needed to be performed for completing and updating the design flow. Furthermore, the Libero SoC converts the HPMS configurations to be compatible with the selected device and package combination.

As part of the HPMS conversion, any changes that were made automatically to be compatible with the device and package selected are printed to the log window. The Libero SoC disables or defaults to different options if the current selected options are not supported in the new targeted device and package.

After the HPMS configuration conversion is done, the HPMS must be regenerated. To regenerate the HPMS component, open the **HPMS component** from the Libero SoC Design Hierarchy Flow window and proceed through the different HPMS pages to complete the generation steps.

Conclusion

This application note describes the design migration among the IGLOO2 FPGA family devices focusing on migration between M2GL025 and M2GL050 within the FCS325 package. The IGLOO2 FPGA family devices share many common architectural features. During design migration, architecture differences between the devices should be kept in mind to ensure a seamless migration flow. Additionally, a key requirement is to run the functional simulation and timing analysis before and after the migration using Microsemi® tools.

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