Migrating Designs Between IGLOO2 M2GL025 and M2GL050 in VF400 Package

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Introduction

This document describes how to migrate designs within the IGLOO®2 field programmable gate array (FPGA) device family between the M2GL025 and M2GL050 devices within the VF400 package. It addresses restrictions and specifications that need to be considered while moving a design between the M2GL025 and M2GL050 devices. This includes pin compatibility between the devices, design and device resources evaluation, I/O banks, standards, and so on. This document also describes the software flow behavior during the migration.

Design Migration

IGLOO2 family devices are architecturally compatible with each other. However, attention must be paid to some key areas while migrating a design from one device to another. The following specific points are discussed in this document:

- Design and Device Evaluation
- I/O Banks and Standards
- Pin Migration and Compatibility
- Power Supply and Board-Level Considerations
- Software Flow

Design and Device Evaluation

One of the initial and main tasks while migrating a design should be to compare the available resources between the two devices. The device resources can be grouped into three different categories:

- High Performance Memory Subsystem
- Fabric Resources
- On-Chip Oscillators

In addition, necessary design timing analysis and simulations should be performed while migrating designs from one device to another.

Each of the following sections focuses on the different aspects of the design and device evaluation categories.

High Performance Memory Subsystem

Table 1 provides a high-level summary of the differences between the M2GL025 and M2GL050 high performance memory subsystem (HPMS) blocks. Based on the different HPMS resources and features, migration from one device to another can be planned to avoid any resource conflicts or issues.

Table 1 • **HPMS Features Per Package or Device**

Feature	VF400 Package	
	M2GL025 and M2GL025T	M2GL050 and M2GL050T
Fabric interfaces (FIC)	1 (FIC_0)	2 (FIC_0 and FIC_1)
Memory subsytem DDR (MDDR)[1]	X18[1]	X18[2]
eNVM (Kbytes)	256	256
eSRAM (Kbytes)	64	64
eSRAM (non-SECDED) (Kbytes)	80	80
SPI, HPDMA, PDMA	2	2
SDRAM through SMC_FIC	Yes	Yes

Notes:

1. *DDR supports x18, x16, x9, and x8 modes*
2. *DDR supports x18 and x16 modes*

Fabric Resources

Table 2 gives a high-level summary of the differences between M2GL025 and M2GL050 fabric resources. Based on the differences, effective logic count, RAM size, and number of I/Os, migration can be evaluated and planned from one device to another without any resource conflicts or issues.

Table 2 • **Summary of the Fabric Features Supported Per Device**

Fabric Features (Logic, DSP, and Memory)		VF400 Package	
		M2GL025 and M2GL025T	M2GL050 and M2GL050T
Logic/DSP	Logic Modules (4-Input LUT)	27,696	56,340
	Mathblocks	34	72
	PLLs and CCCs	6	6
Fabric Memory	LSRAM 18 K blocks	31	69
	uSRAM 1K blocks	34	72
User I/Os	MSIO (3.3 V max)	111	87
	MSIOD (2.5 V max)	32	32
	DDRIO (2.5 V max)	64	88
	Total user I/Os per package	207	207

On-Chip Oscillators

Table 3 shows the summary of IGLOO2 on-chip oscillators that are the primary sources for generating free-running clocks.

Table 3 • **On-Chip Oscillator Support Per Device**

Feature	VF400 Package	
	M2GL025	M2GL050
1 MHz RC oscillator	1	1
50 MHz RC oscillator	1	1

Table 3 • **On-Chip Oscillator Support Per Device**

Feature	VF400 Package	
	M2GL025	M2GL050
Main crystal oscillator (32 KHz - 20 MHz)	1	1
Auxiliary crystal oscillator (32 KHz - 20 MHz)	1	-

Refer to the *IGLOO2 Clocking Resources User Guide* for more information.

I/O Banks and Standards

IGLOO2 I/Os are partitioned into multiple I/O voltage banks. The number of banks depends on the device. There are seven(7) I/O banks in M2GL025 and eight(8) I/O banks in the M2GL050 device. Table 4 shows a summary of organization of the I/O banks between M2GL025 and M2GL050 FPGA devices.

Table 4 • **Organization of the I/O Banks in IGLOO2 Devices**

I/O Banks	VF400 Package	
	M2GL025T	M2GL050T
Bank 0	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	MSIO: fabric	MSIO: fabric
Bank 2	MSIO: fabric	–
Bank 3	MSIO: JTAG	MSIO: fabric
Bank 4	MSIO: fabric	MSIO: JTAG
Bank 5	MSIOD: SERDES_0 or fabric	DDRIO: fabric
Bank 6	MSIOD: fabric	MSIOD: SERDES_0 or fabric
Bank 7	MSIO: fabric	MSIOD: fabric
Bank 8	–	MSIO: fabric

Package pins VDDIx are the bank power supplies where x indicates the bank number. For example, VDDI0 is bank0 power supply. Figure 1 and Figure 2 show the different I/O bank locations and numbers per device in the VF400 package.

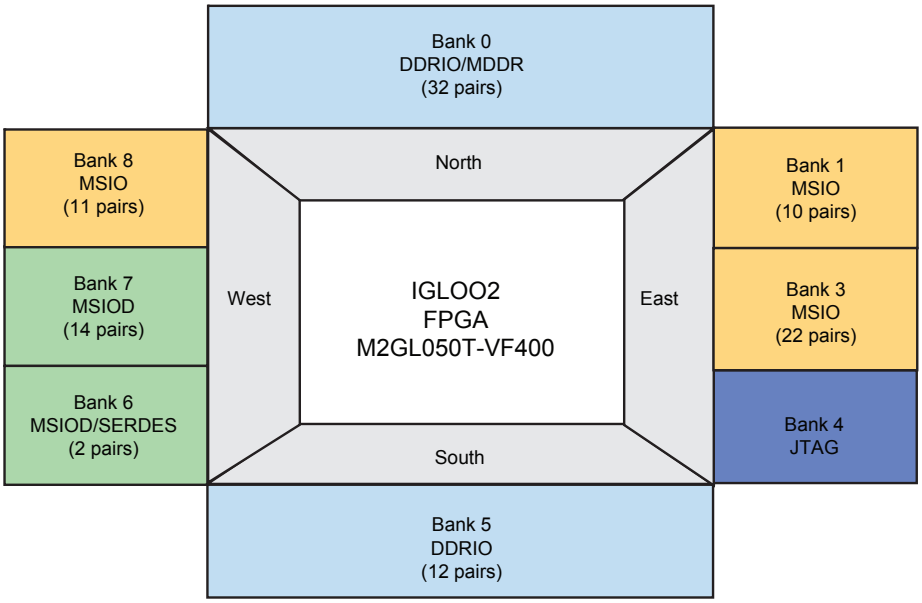

***Figure 1* • IGLOO2 M2GL050T VF400 I/O Bank Locations**

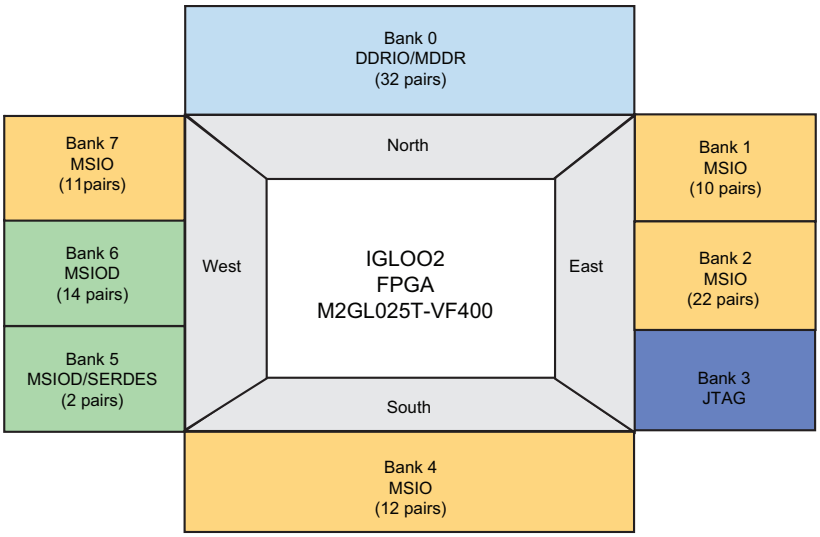

***Figure 2* • IGLOO2 M2GL025T VF400 I/O Bank Locations**

An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltage standards. MSIOD or DDRIO bank supports 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltage standards. The 3.3 V voltage standard is not supported for MSIOD or DDRIO I/Os. For more details on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, refer to the "Supported Voltage Standards" table in the *IGLOO2 FPGA Fabric Architecture User Guide*.

Pin Migration and Compatibility

Although the IGLOO2 devices and packaging have been designed to allow footprint compatibility for smoother migration, some of the pins have a reduced compatibility feature set between M2GL025 and M2GL050 devices in the VF400 package. This section addresses the different aspects of pin compatibility. The differences can be grouped into three categories:

- Global Versus Regular Pins
- Available versus No Connect Pins
- I/Os Technology Compatibility Per Pin or Bank
- Probe Pins

Global Versus Regular Pins

When migrating designs between IGLOO2 devices, it is important to evaluate the different types of pins that are available per device. The functionality of the same pin can be different between devices. This section focuses on highlighting and comparing the global pins in one device against the other devices. Therefore, migration can be evaluated and planned from one device to another without any resource conflicts or issues.

- Moving from a device, where the I/O is a global pin to a device where the same I/O is a regular pin. In this case, replace the global clock (for example, CLKBUF) with a regular input buffer (for example, INBUF) and then internally promote the signal to a global resource using a CLKINT or synthesis options.
- Moving from a device, where the I/O is a regular pin to a device where the same I/O is a global pin. In this case, replace the INBUF with a CLKBUF or keep the INBUF and internally promote the signal to a global using a CLKINT or synthesis options.

Table 5 provides a comparison between the global pins available in M2GL025 and M2GL050 devices. The unused global pins are configured as inputs with pull-up resistors by Libero® System-on-Chip (SoC) software.

For more information, refer to the "FPGA Fabric Global Network Architecture" chapter of the *IGLOO2 Clocking Resources User Guide*.

Table 5 • **Non-Equivalent Global Pins Comparison Per Device**

Package Pin	VF400 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
A3	DDRIO62PB0/MDDR_DQ_ECC1	0	DDRIO87PB0/**CCC_NW1_CLKI3**/MDDR_DQ_ECC1	0
E6	DDRIO61PB0/**CCC_NW1_CLKI3**	0	DDRIO88PB0	0
R13	**MSIO**134PB4/VCCC_SE1_CLKI	4	**DDRIO**164PB5/VCCC_SE1_CLKI	5
U11	**MSIO**125NB4/GB7/CCC_SW1_CLKI2	4	**DDRIO**152NB5/GB7/CCC_SW1_CLKI2	5
U13	**MSIO**133PB4/GB15/VCCC_SE1_CLKI	4	**DDRIO**163PB5/GB15/VCCC_SE1_CLKI	5
V11	**MSIO**125PB4/GB3/CCC_SW0_CLKI3	4	**DDRIO**152PB5/GB3/CCC_SW0_CLKI3	5
V12	**MSIO**130PB4/VCCC_SE0_CLKI	4	**DDRIO**160PB5/VCCC_SE0_CLKI	5
W10	**MSIO**120NB4/CCC_SW0_CLKI2	4	**DDRIO**147NB5/CCC_SW0_CLKI2	5
W13	**MSIO**131PB4/GB11/VCCC_SE0_CLKI	4	**DDRIO**161PB5/GB11/VCCC_SE0_CLKI	5
Y12	**MSIO**129PB4/CCC_SW1_CLKI3	4	**DDRIO**159PB5/CCC_SW1_CLKI3	5

Table 6 shows the list of global pins that are similar between the two devices.

Table 6 • **Equivalent Global Pins Per Device**

Package Pin	VF400 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
A1	DDRIO65PB0/GB0/CCC_NW0_CLKI3	0	DDRIO91PB0/GB0/CCC_NW0_CLKI3	0
A11	DDRIO49PB0/CCC_NE1_CLKI3/MDDR_DQ14	0	DDRIO75PB0/CCC_NE1_CLKI3/MDDR_DQ14	0
B1	DDRIO65NB0/GB4/CCC_NW1_CLKI2	0	DDRIO91NB0/GB4/CCC_NW1_CLKI2	0
C9	DDRIO52PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0	DDRIO78PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0
D10	DDRIO50PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0	DDRIO76PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0
D3	DDRIO66NB0/CCC_NW0_CLKI2	0	DDRIO92NB0/CCC_NW0_CLKI2	0
D9	DDRIO53PB0/CCC_NE0_CLKI2/MDDR_DQ10	0	DDRIO79PB0/CCC_NE0_CLKI2/MDDR_DQ10	0
E18	MSIO28PB1/GB14/VCCC_SE1_CLKI	1	MSIO42PB1/GB14/VCCC_SE1_CLKI	1
F19	MSIO26PB1/CCC_NE1_CLKI1	1	MSIO40PB1/CCC_NE1_CLKI1	1
G1	MSIO97PB7/GB2/CCC_NW0_CLKI1	7	MSIO115PB8/GB2/CCC_NW0_CLKI1	8
G14	MSIO25PB1/CCC_NE0_CLKI1	1	MSIO39PB1/CCC_NE0_CLKI1	1
G17	MSIO27PB1/GB10/VCCC_SE0_CLKI	1	MSIO41PB1/GB10/VCCC_SE0_CLKI	1
G2	MSIO96PB7/GB6/CCC_NW1_CLKI1	7	MSIO114PB8/GB6/CCC_NW1_CLKI1	8
H1	MSIOD100PB6/GB5/CCC_SW1_CLKI1	6	MSIOD118PB7/GB5/CCC_SW1_CLKI1	7
H20	MSIO20NB2/GB13/VCCC_SE1_CLKI	2	MSIO20NB3/GB13/VCCC_SE1_CLKI	3
H5	MSIO98PB7/CCC_NW1_CLKI0	7	MSIO116PB8/CCC_NW1_CLKI0	8
J19	MSIO20PB2/GB9/VCCC_SE0_CLKI	2	MSIO20PB3/GB9/VCCC_SE0_CLKI	3
J2	MSIOD102PB6/CCC_SW1_CLKI0	6	MSIOD120PB7/CCC_SW1_CLKI0	7
J4	MSIOD101PB6/GB1/CCC_SW0_CLKI1	6	MSIOD119PB7/GB1/CCC_SW0_CLKI1	7
J7	MSIO99PB7/CCC_NW0_CLKI0	7	MSIO117PB8/CCC_NW0_CLKI0	8
K7	MSIOD103PB6/CCC_SW0_CLKI0	6	MSIOD121PB7/CCC_SW0_CLKI0	7
M17	MSIO11NB2/CCC_NE1_CLKI0	2	MSIO11NB3/CCC_NE1_CLKI0	3
N16	MSIO11PB2/CCC_NE0_CLKI0	2	MSIO11PB3/CCC_NE0_CLKI0	3

Refer to the "Dedicated Global I/O Naming Conventions" section in the *IGLOO2 Pin Descriptions*.

Available versus No Connect Pins

There are pins that have one specific function in one device while those same pins are "no connect" (NC) in the other device. Table 7 lists the summary of these pins.

Table 7 • **Available versus NC Pins**

Package Pin	VF400 Pin Names	
	M2GL025	M2GL050
Y17	VPP	NC
W17	VPP	NC
P13	NC	VREF5
R11	NC	VREF5

For example, pin Y17 functions as the VPP pin in the M2GL025 while it is an NC in the M2GL050 device. Similarly, P13 pin is an NC in the M2GL025 but it is a VREF5 pin in the M2GL050 device.

When moving from a device, where the I/O is an NC pin to a device where the I/O has a defined functionality and it is not used, follow the recommended methods for connecting the unused I/Os depending on the functionality of that I/O. Refer to "Unused Pin Configurations" in the Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA Application Note.

When moving from a device, where the I/O has a defined functionality to a device where the I/O is an NC, then the NC pins can be driven to any voltage or can be left floating with no effect on the operation of the device. NC indicates that the pin is not connected to circuitry within the device.

I/Os Technology Compatibility Per Pin or Bank

Table 8 shows the list of I/Os that would lead to incompatibility with the different technology support while migrating between M2GL025 and M2GL050 within the VF400 package. The difference is the type of I/O technology (MSIO versus DDRIO) that is supported on those regular I/Os.

Table 8 • **I/O Standards Compatibility Per Device or Package Pins**

Package Pin	VF400 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
R12	**MSIO**134NB4	4	**DDRIO**164NB5	5
R13	**MSIO**134PB4/VCCC_SE1_CLKI	4	**DDRIO**164PB5/VCCC_SE1_CLKI	5
T13	**MSIO**133NB4	4	**DDRIO**163NB5	5
T14	**MSIO**144PB4	4	**DDRIO**184PB5	5
T15	**MSIO**144NB4	4	**DDRIO**184NB5	5
U11	**MSIO**125NB4/GB7/CCC_SW1_CLKI2	4	**DDRIO**152NB5/GB7/CCC_SW1_CLKI2	5
U12	**MSIO**130NB4	4	**DDRIO**160NB5	5
U13	**MSIO**133PB4/GB15/VCCC_SE1_CLKI	4	**DDRIO**163PB5/GB15/VCCC_SE1_CLKI	5
U14	**MSIO**142NB4	4	**DDRIO**181NB5	5
V11	**MSIO**125PB4/GB3/CCC_SW0_CLKI3	4	**DDRIO**152PB5/GB3/CCC_SW0_CLKI3	5
V12	**MSIO**130PB4/VCCC_SE0_CLKI	4	**DDRIO**160PB5/VCCC_SE0_CLKI	5
V14	**MSIO**142PB4	4	**DDRIO**181PB5	5
V15	**MSIO**146NB4	4	**DDRIO**190NB5	5
W10	**MSIO**120NB4/CCC_SW0_CLKI2	4	**DDRIO**147NB5/CCC_SW0_CLKI2	5

Table 8 • **I/O Standards Compatibility Per Device or Package Pins (continued)**

Package Pin	VF400 Pin Names			
	M2GL025	Bank No	M2GL050	Bank No
W12	**MSIO**121NB4/PROBE_B	4	**DDRIO**148NB5/PROBE_B	5
W13	**MSIO**131PB4/GB11/VCCC_SE0_CLKI	4	**DDRIO**161PB5/GB11/VCCC_SE0_CLKI	5
W14	**MSIO**131NB4	4	**DDRIO**161NB5	5
W15	**MSIO**146PB4	4	**DDRIO**190PB5	5
Y10	**MSIO**120PB4	4	**DDRIO**147PB5	5
Y11	**MSIO**121PB4/PROBE_A	4	**DDRIO**148PB5/PROBE_A	5
Y12	**MSIO**129PB4/CCC_SW1_CLKI3	4	**DDRIO**159PB5/CCC_SW1_CLKI3	5
Y13	**MSIO**129NB4	4	**DDRIO**159NB5	5
Y15	**MSIO**145PB4	4	**DDRIO**187PB5	5
Y16	**MSIO**145NB4	4	**DDRIO**187NB5	5

The DDRIOs do not support single ended 3.3 V I/O standards and differential LVPECL, LVDS 3.3 V, LVDS 2.5 V, RSDS BLVDS, MLVDS, and Mini-LVDS I/O standards, as shown in Table 9. To migrate from M2GL025 to M2GL050 successfully, ensure that the correct VDDI power supply is used to power the equivalent banks. Only I/Os with compatible standards can be assigned to the same bank.

Table 9 • **Technology Support Difference Between Different I/O Types**

I/O Standards	I/O Types	
	MSIO	DDRIO
Single-Ended I/O		
LVTTL 3.3V	Yes	–
LVCMOS 3.3V	Yes	–
PCI	Yes	–
LVCMOS 1.2V	Yes	Yes
LVCMOS 1.5V	Yes	Yes
LVCMOS 1.8V	Yes	Yes
LVCMOS 2.5V	Yes	Yes
Voltage-Referenced I/O		
HSTL 1.5V	Yes	Yes
SSTL 1.8	Yes	Yes
SSTL 2.5	Yes	Yes
SSTL 2.5 V(DDR1)	Yes	Yes
SSTL 1.8 V(DDR2)	Yes	Yes
SSTL 1.5 V (DDR3)	Yes	Yes
Differential I/O		
LVPECL (input only)	Yes	–
LVDS 3.3 V	Yes	–
LVDS 2.5 V	Yes	–
RSDS	Yes	–
BLVDS	Yes	–

Table 9 • **Technology Support Difference Between Different I/O Types (continued)**

I/O Standards	I/O Types	
	MSIO	**DDRIO**
MLVDS	Yes	–
Mini-LVDS	Yes	–

Note: Even though the VDDI might be the same (for example, MSIO 2.5 V and DDRIO 2.5 V), the attributes and features supported might be different between different I/O types (MSIO versus DDRIO). Refer to the "I/O Programmable Features" section in the *IGLOO2 FPGA Fabric Architecture User Guide* for more information on the list of features supported per I/O type.

Probe Pins

Probe pins locations are compatible between the two devices. Table 10 shows the different probe I/Os location per device within the VF400 package. By default, probe pins are reserved for the probe functionality. Unreserve these pins by clearing the **Reserve Pins for Probes** check box in the "Device I/O Settings" under Project Setting in Libero SoC software. When the pins are not reserved, the probe I/Os can be used as regular I/Os.

Note: Different I/O technologies are supported on these pins (MSIO versus DDRIO). Refer to "I/Os Technology Compatibility Per Pin or Bank" on page 7 for more information.

Table 10 • **Probe Pins Per Device**

Package Pin	VF400 Pin Names			
	M2GL025	**Bank No**	**M2GL050**	**Bank No**
W12	**MSIO**121NB4/PROBE_B	4	**DDRIO**148NB5/PROBE_B	5
Y11	**MSIO**121PB4/PROBE_A	4	**DDRIO**148PB5/PROBE_A	5

Power Supply and Board-Level Considerations

I/O power supply requirements are one of the key aspects to consider for design migrations. Since the migration is within the IGLOO2 family, there is no issue regarding the core voltage (VDD), charge pumps voltage (VPP), and analog sense circuit supply of the eNVM voltage (VPPNVM). The ground pins (VSS) are also equivalent between M2GL025 and M2GL050 devices. Refer to the *IGLOO2 Pin Descriptions* for more details. The bank supply voltages VDDI pins must be connected appropriately. Refer to the "Recommendation for Unused Bank Supplies" connections table in the Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA Application Note for more information in case where the specific banks are not used. An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltages and an MSIOD and DDRIO bank supports 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, refer to the "Supported Voltage Standards" table in the *IGLOO2 FPGA Fabric Architecture User Guide*.

The banks have dedicated supplies. Therefore, only I/Os with compatible voltage standards can be assigned to the same I/O voltage bank. The correct bank supply must be used when migrating between the different devices per the appropriate voltages (I/O Standards) selected for the bank. Table 11 shows the different banks power supply compatibility per device in the VF400 package.

Table 11 • **Power Supply Compatibility Per Device**

Package Pin	VF400 Pin Names	
	M2GL025	**M2GL050**
F2	VDDI7	VDDI8
G5	VDDI7	VDDI8
H18	VDDI2	VDDI3
J1	VDDI6	VDDI7
J8	VDDI7	VDDI8

***Table 11* • Power Supply Compatibility Per Device (continued)**

Package Pin	VF400 Pin Names	
	M2GL025	**M2GL050**
K4	VDDI6	VDDI7
L17	VDDI2	VDDI3
L8	VDDI6	VDDI7
M20	VDDI2	VDDI3
N14	VDDI2	VDDI3
N3	VDDI6	VDDI7
P16	VDDI2	VDDI3
R14	VDDI3	VDDI4
R19	VDDI2	VDDI3
R3	VDDI5	VDDI6
T12	VDDI4	VDDI5
U15	VDDI4	VDDI5
V18	VDDI2	VDDI3
W11	VDDI4	VDDI5
Y14	VDDI4	VDDI5

For the other bank supplies that are equivalent, refer to the provided recommendations in the *IGLOO2 Pin Descriptions*.

Any other board-level considerations are common among the three devices. Refer to the Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA Application Note for more details.

Software Flow

The Libero® SoC Software provides the option of reserving pins for moving between different devices within the IGLOO2 family where pins within the current device that are not bonded in the destination device can be automatically reserved. This option is available in I/O Constraints Editor which can be accessed from the Design Flow window as shown in Figure 3. This is done in the early stages of the design cycle.

Follow the procedure given below to reserve pins:

1. After finishing the **Compile** process, select the **I/O Constraints** option from the Design Flow window as shown in Figure 3.

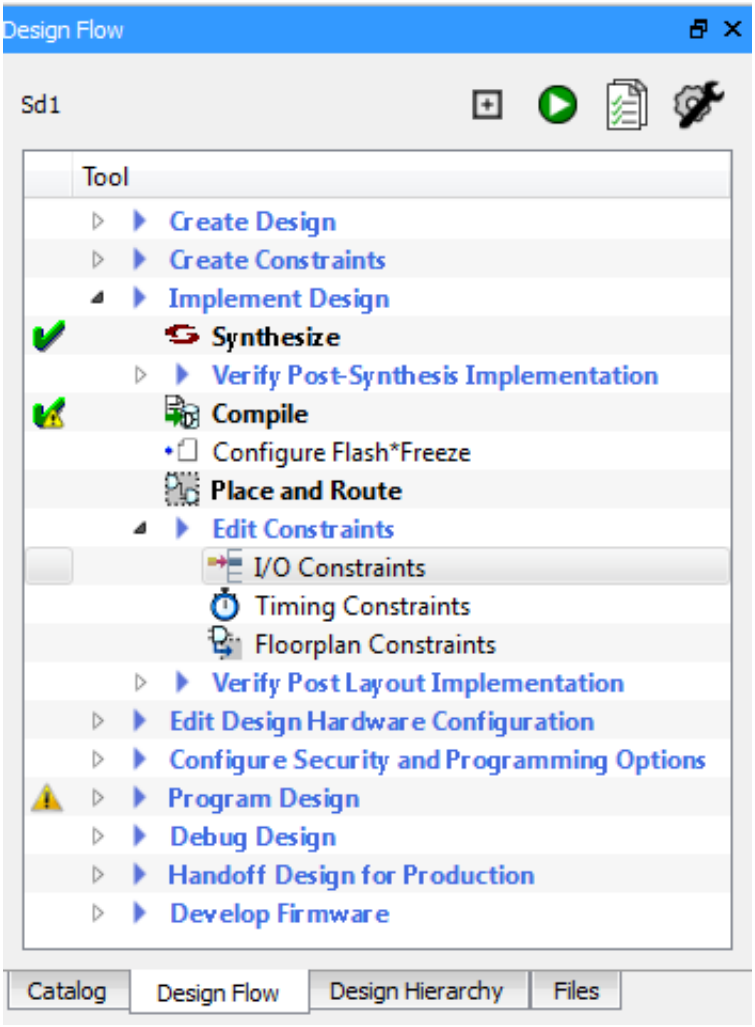

***Figure 3* • I/O Constraint Editor Option part of the Design Flow**

2. Select the **Reserve Pins for Device Migration** option from the Tools menu. The window shown below in Figure 4 is displayed.

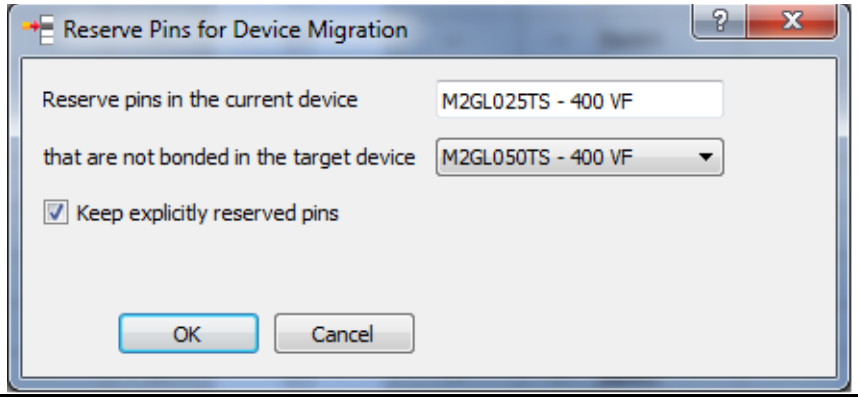

***Figure 4* • Reserve Pins for Device Migration**

The first option shows the device that is currently being used in the Libero SoC project. From the drop-down list, select the device that eventually will be migrated to as the target device. Refer to the Libero Soc software online help for more details on this window and other options.

The Libero SoC software provides the option of moving between different devices within the IGLOO2 family by changing the device selection using the **Project Settings** option in the Libero SoC software. Upon changing the device, Libero SoC software validates the features that are used within the design against the supported features within the new targeted device and package. Feedback messages are provided as part of the Libero SoC software flow listing the different actions taken by Libero SoC and the action required.

The first step that Libero SoC performs upon changing the device is to invalidate the original design components and the design flows. The message is displayed as shown in Figure 5.

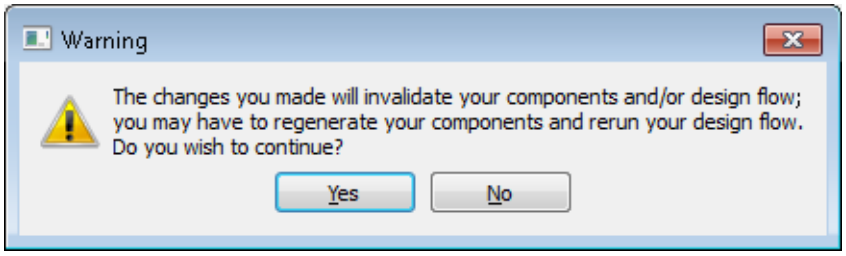

***Figure 5* • Invalidating Component and Design Flow Message**

As part of re-running the design flow, Libero SoC checks the different steps needed to be performed for completing and updating the design flow. Furthermore, Libero SoC converts the HPMS configurations to be compatible with the selected device and package combination.

As part of the HPMS conversion, any changes that were made automatically to be compatible with the device and package selected will be printed to the log window. Libero SoC disables or defaults to different options if the current selected options are not supported in the new targeted device and package.

After the HPMS configuration conversion is done, HPMS must be regenerated. To regenerate the HPMS component, open the HPMS component from **Libero SoC Design Hierarchy Flow** window and proceed through the different HPMS pages to complete the generation.

Conclusion

This application note describes the design migration among IGLOO2 family devices focusing on migration between M2GL025 and M2GL050 within the VF400 package. IGLOO2 family devices share many common architectural features. During design migration, architecture differences between devices should be kept in mind to ensure seamless migration flow. Additionally, a key requirement is to run the functional simulation and timing analysis before and after the migration using Microsemi tools.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Revision	Changes	Page
Revision 1 (February 2014)	First version	

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