AC415
Application Note
Migrating Designs Between SmartFusion2 M2S025 and M2S050, M2S050T(S) and M2S060T(S) Devices in VF400 Package

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 2.0

In revision 2.0, the document was updated to include the migration techniques for M2S060T(S) and M2S050T(S) devices. The following is a summary of the changes made in revision 2.0:

- Table 7, page 7 is added to include the non-equivalent global pins comparison for M2S060T(S) and M2S050T(S) devices.
- Title of Table 6, page 7 is edited as, “Non-Equivalent Global Pins Comparison Per Device for M2S025 and M2S050 Devices.”
- Title of Table 8, page 8 is edited as, “Equivalent Global Pins Per Device for M2S025 and M2S050 Devices.”
- Table 9, page 9 and Table 12, page 12 are added.
- Table 10, page 11 is edited to include the details of available Vs no connect pins, for M2S060T(S) and M2S050T(S) devices.
- Title of Table 11, page 11 is edited as I/O Standards Compatibility Per Device or Package Pins for M2S025 and M2S050 Devices.

1.2 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Migrating Designs Between SmartFusion2 M2S025 and M2S050, M2S050T(S) and M2S060T(S) Devices in VF400 Package

This document describes how to migrate designs within the SmartFusion®2 SoC field programmable gate array (FPGA) family between the M2S025 and M2S050 devices,M2S060T(S) and M2S050T(S) devices, within the VF400 package. It addresses restrictions and specifications that need to be considered while migrating a design between M2S025 and M2S050, M2S060T(S) and M2S050T(S).This includes pin compatibility between the devices, design and device resources evaluation, I/O banks, standards, and so on. This document also describes the software flow behavior during the migration.

2.1 Design Migration

SmartFusion2 family devices are architecturally compatible with each other. However, some key points must be considered, while migrating a design from one device to another. The following specific points are discussed in this document:

2.1.1 Design and Device Evaluation

One of the initial and main tasks while migrating a design should be to compare the available resources between the two devices. The device resources can be grouped into following three categories:

In addition, necessary design timing analysis and simulations should be performed while migrating designs from one device to another.

Each of the following sections focuses on the different aspects of the design and device evaluation.

2.1.1.1 Microcontroller Subsystem

The following table provides a high-level summary of the differences between the M2S025 and M2S050 MSS blocks. Based on the different MSS resources and features, migration from one device to another can be planned to avoid any resource conflicts or issues.

Table 1 • **MSS Features Per Package or Device**

	VF400 Package	
Feature	**M2S025 and M2S025T**	**M2S050 and M2S050T**
ARM® Cortex™-M3 processor + instruction cache	Yes	Yes
Fabric interfaces (FIC)	1 (FIC_0)	2 (FIC_0 and FIC_1)
MSS DDR (MDDR)	X18[1]	X18[2]
eNVM (Kbytes)	256	256
eSRAM (Kbytes)	64	64
eSRAM (non-SECDED) (Kbytes)	80	80

Table 1 • **MSS Features Per Package or Device *(continued)***

	VF400 Package	
Feature	**M2S025 and M2S025T**	**M2S050 and M2S050T**
CAN, 10/100/1000 Ethernet	1	1
High-speed USB	1 (UTMI or ULPI)	-
Multi-Mode UART, SPI, I2C, Timer	2	2
SDRAM through SMC_FIC	Yes (AHBLite interface only)	Yes (AXI or AHBLite Interfaces)

DDR supports x18, x16, x9, and x8 modes
DDR supports x18 and x16 modes

The following sections highlight the differences in the MSS supported features between the two SmartFusion2 devices.

2.1.1.1.1 Soft Memory Controller Fabric Interface

MSS, as a master, through the soft memory controller fabric interface (SMC_FIC) and an SMC in the FPGA fabric can access external bulk memories other than the DDR, such as synchronous dynamic random access memory (SDRAM). Instantiate a soft AMBA high-performance bus (AHB) or advanced extensible interface (AXI) SDRAM memory controller in the FPGA fabric and connect I/O ports to 3.3 V MSIO.

The SMC_FIC can be configured using the MDDR configurator part of the MSS to use either an AXI 64-bit bus interface or a single 32-bit AHB-Lite (AHBL) bus interface. The M2S025 device only supports the AHBLite interface. For vertical migration between the M2S025 and M2S050 devices, common AHBL SMC_FIC interface configuration is used to avoid any conflicts.

2.1.1.1.2 USB Controller

USB is not supported on M2S050 devices. The USB controller provides two types of interfaces, UTMI and ULPI. The USB ULPI interface is connected to four separate groups of MSIO pads on the device. Depending on the size of the device, the group is categorized as ULPI (I/Os) A, ULPI (I/Os) B, ULPI (I/Os) C, and ULPI (I/Os) D interfaces. The set of signals available in each of the four alternative I/Os are the same. The USB I/Os are muxed with other MSS peripherals. The different sets of I/O groups are provided to maximize the flexibility of having the USB operational in the system, regardless of the other MSS peripherals.

The following table shows a summary of the different supported interfaces between M2S025 and M2S050 devices in the VF400 package.

Table 2 • **USB Supported Interfaces Per Device**

	VF400 Package				
Device	**ULPI (I/Os) A**	**ULPI (I/Os) B**	**ULPI (I/Os) C**	**ULPI (I/Os) D**	**UTMI**
M2S025	Yes	Yes	Yes	No	Yes
M2S050	No	No	No	No	No

2.1.1.2 Fabric Resources

The following table gives a high-level summary of the differences between M2S025 and M2S050 fabric resources. Based on the differences, effective logic count, RAM size, and number of I/Os, migration can be evaluated and planned from one device to another without any resource conflicts or issues.

Table 3 • **Summary of the Fabric Features Supported Per Device**

		VF400 Package	
Fabric Features (Logic, DSP, and Memory)		**M2S025 and M2S025T**	**M2S050 and M2S050T**
Logic/DSP	Logic Modules (4-Input LUT)	27,696	56,340
	Mathblocks	34	72
	PLLs and CCCs	6	6
Fabric Memory	LSRAM 18 K blocks	31	69
	uSRAM 1K blocks	34	72
User I/Os	MSIO (3.3 V max)	111	87
	MSIOD (2.5 V max)	32	32
	DDRIO (2.5 V max)	64	88
	Total user I/Os per package	207	207

2.1.1.3 On-Chip Oscillators

The following table shows the summary of SmartFusion2 on-chip oscillators that are the primary sources for generating free-running clocks.

Table 4 • **On-Chip Oscillator Support Per Device**

	VF400 Package	
Feature	**M2S025**	**M2S050**
1 MHz RC oscillator	1	1
50 MHz RC oscillator	1	1
Main crystal oscillator (32 KHz - 20 MHz)	1	1
Auxiliary crystal oscillator (32 KHz - 20 MHz)	1	-

The auxiliary crystal oscillator is dedicated for real-time counter (RTC) clocking as an alternative clock source. See the *SmartFusion2 Clocking Resources User's Guide* for more information.

2.1.2 I/O Banks and Standards

SmartFusion2 I/Os are partitioned into multiple I/O voltage banks. The number of banks depends on the type of the device. There are seven(7) I/O banks in M2S025 and eight(8) I/O banks in the M2S050 device. The following table shows a summary of organization of the I/O banks between M2S025 and M2S050 FPGA devices.

Table 5 • **Organization of the I/O Banks in SmartFusion2 Devices**

	VF400 Package	
I/O Banks	**M2S025T**	**M2S050T**
Bank 0	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric
Bank 1	MSIO: MSS or fabric	MSIO: MSS or fabric

Table 5 • **Organization of the I/O Banks in SmartFusion2 Devices *(continued)***

	VF400 Package	
I/O Banks	**M2S025T**	**M2S050T**
Bank 2	MSIO: MSS or fabric	–
Bank 3	MSIO: JTAG/SWD	MSIO: MSS or fabric
Bank 4	MSIO: fabric	MSIO: JTAG/SWD
Bank 5	MSIOD: SERDES_0 or fabric	DDRIO: fabric
Bank 6	MSIOD: fabric	MSIOD: SERDES_0 or fabric
Bank 7	MSIO: fabric	MSIOD: fabric
Bank 8		MSIO: fabric

Package pins VDDIx, are the bank power supplies where x indicates the bank number. For example, VDDI0 is bank0 power supply. The following figure and Figure 2 on page 6 show the different I/O bank locations and numbers per device in the VF400 package.

Figure 1 • **SmartFusion2 M2S050 VF400 I/O Bank Locations**

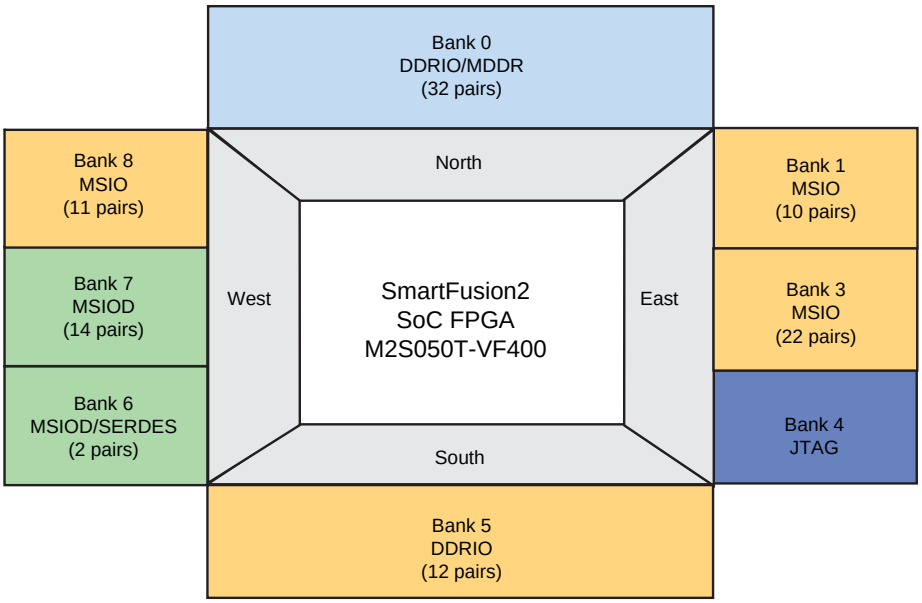
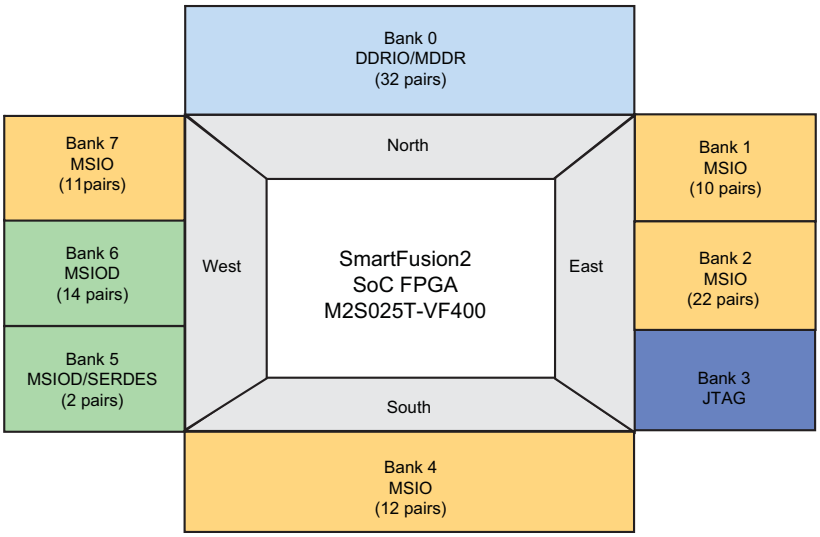


Figure 2 • **SmartFusion2 M2S025 VF400 I/O Bank Locations**



An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltage standards. MSIOD or DDRIO bank supports 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltage standards. The 3.3 V voltage standard is not supported for MSIOD or DDRIO I/Os. For more details on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, see the “Supported Voltage Standards” table in the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

2.1.3 Pin Migration and Compatibility

The SmartFusion2 devices and packaging have been designed to allow footprint compatibility for smoother migration but some of the pins have a reduced compatibility feature set between M2S025 and M2S050 devices in the VF400 package. This section addresses the different aspects of pin compatibility. The differences can be grouped into the following categories:

- Global Versus Regular Pins, page 6
- Available versus No Connect Pins, page 10
- I/O Technology Compatibility Per Pin or Bank, page 11
- Oscillator Pins, page 13
- Probe Pins, page 14

2.1.3.1 Global Versus Regular Pins

When migrating designs between SmartFusion2 devices, it is important to evaluate the different types of pins that are available per device. The functionality of the same pin can be different between devices. This section focuses on highlighting and comparing the global pins in one device against the other devices.

- When migrating from a device, where the I/O is a global pin to a device where the same I/O is a regular pin, replace the global clock (for example, CLKBUF) with a regular input buffer (for example, INBUF) and internally promote the signal to a global resource using a CLKINT or synthesis options.
- When migrating from a device, where the I/O is a regular pin to a device where the same I/O is a global pin, replace the INBUF with a CLKBUF or keep the INBUF and internally promote the signal to global using a CLKINT or synthesis options.

Table 6, page 7 and Table 7, page 7 provide a comparison between the global pins available in M2S025 and M2S050, M2S060T(S) and M2S050T(S) devices respectively. The unused global pins are configured as inputs with pull-up resistors by Libero® SoC software.

For more information, see the “FPGA Fabric Global Network Architecture” chapter of the *SmartFusion2 Clocking Resources User’s Guide*.

Table 6 • **Non-Equivalent Global Pins Comparison Per Device for M2S025 and M2S050 Devices**

Package Pin	VF400 Pin Names			
	M2S025	**Bank No**	**M2S050**	**Bank No**
A3	DDRIO62PB0/MDDR_DQ_ECC1	0	DDRIO87PB0/**CCC_NW1_CLKI3**/MDDR_DQ_ECC1	0
E6	DDRIO61PB0/**CCC_NW1_CLKI3**	0	DDRIO88PB0	0
R13	MSIO134PB4/VCCC_SE1_CLKI	4	**DDRIO**164PB5/VCCC_SE1_CLKI	5
U11	MSIO125NB4/GB7/CCC_SW1_CLKI2	4	**DDRIO**152NB5/GB7/CCC_SW1_CLKI2	5
U13	MSIO133PB4/GB15/VCCC_SE1_CLKI	4	**DDRIO**163PB5/GB15/VCCC_SE1_CLKI	5
V11	MSIO125PB4/GB3/CCC_SW0_CLKI3	4	**DDRIO**152PB5/GB3/CCC_SW0_CLKI3	5
V12	MSIO130PB4/VCCC_SE0_CLKI	4	**DDRIO**160PB5/VCCC_SE0_CLKI	5
W10	MSIO120NB4/CCC_SW0_CLKI2	4	**DDRIO**147NB5/CCC_SW0_CLKI2	5
W13	MSIO131PB4/GB11/VCCC_SE0_CLKI	4	**DDRIO**161PB5/GB11/VCCC_SE0_CLKI	5
Y12	MSIO129PB4/CCC_SW1_CLKI3	4	**DDRIO**159PB5/CCC_SW1_CLKI3	5

Table 7 • **Non-Equivalent Global Pins Comparison Per Device for M2S060T(S) and M2S050T(S) Devices**

Package Pin	M2S060T(S)	Bank No	M2S050T(S)	Bank No
A3	DDRIO77PB1/MDDR_DQ_ECC1	1	DDRIO87PB0/CCC_NW1_CLKI3/MDDR_DQ_ECC1	0
E6	DDRIO76PB1/CCC_NW1_CLKI3	1	DDRIO88PB0	0
R13	MSIO179PB6/VCCC_SE1_CLKI	6	DDRIO164PB5/VCCC_SE1_CLKI	5
U11	MSIO167NB6/GB7/CCC_SW1_CLKI2	6	DDRIO152NB5/GB7/CCC_SW1_CLKI2	5
U13	MSIO178PB6/GB15/VCCC_SE1_CLKI	6	DDRIO163PB5/GB15/VCCC_SE1_CLKI	5
V11	MSIO167PB6/GB3/CCC_SW0_CLKI3	6	DDRIO152PB5/GB3/CCC_SW0_CLKI3	5
V12	MSIO175PB6/VCCC_SE0_CLKI	6	DDRIO160PB5/VCCC_SE0_CLKI	5

Table 7 • **Non-Equivalent Global Pins Comparison Per Device for M2S060T(S) and M2S050T(S) Devices *(continued)***

W10	MSIO162NB6/CCC_SW0_CLKI2	6	DDRIO147NB5/CCC_SW0_CLKI2	5
W13	MSIO176PB6/GB11/VCCC_SE0_CLKI	6	DDRIO161PB5/GB11/VCCC_SE0_CLKI	5
Y12	MSIO174PB6/CCC_SW1_CLKI3	6	DDRIO159PB5/CCC_SW1_CLKI3	5

The following tables show the list of global pins that are similar between the respective devices.

Table 8 • **Equivalent Global Pins Per Device for M2S025 and M2S050 Devices**

	VF400 Pin Names			
Package Pin	**M2S025**	**Bank No**	**M2S050**	**Bank No**
A1	DDRIO65PB0/GB0/CCC_NW0_CLKI3	0	DDRIO91PB0/GB0/CCC_NW0_CLKI3	0
A11	DDRIO49PB0/CCC_NE1_CLKI3/MDDR_DQ14	0	DDRIO75PB0/CCC_NE1_CLKI3/MDDR_DQ14	0
B1	DDRIO65NB0/GB4/CCC_NW1_CLKI2	0	DDRIO91NB0/GB4/CCC_NW1_CLKI2	0
B12	DDRIO45NB0/MDDR_CLK_N	0	DDRIO59NB0/MDDR_CLK_N	0
B13	DDRIO45PB0/MDDR_CLK	0	DDRIO59PB0/MDDR_CLK	0
B19	MSIO33NB1/MMUART_0_CLK/GPIO_29_B/USB_NXT_C	1	MSIO47NB1/MMUART_0_CLK/GPIO_29_B	1
C9	DDRIO52PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0	DDRIO78PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0
D10	DDRIO50PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0	DDRIO76PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0
D3	DDRIO66NB0/CCC_NW0_CLKI2	0	DDRIO92NB0/CCC_NW0_CLKI2	0
D9	DDRIO53PB0/CCC_NE0_CLKI2/MDDR_DQ10	0	DDRIO79PB0/CCC_NE0_CLKI2/MDDR_DQ10	0
E18	MSIO28PB1/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C	1	MSIO42PB1/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B	1
F19	MSIO26PB1/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B	1	MSIO40PB1/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B	1
G1	MSIO97PB7/GB2/CCC_NW0_CLKI1	7	MSIO115PB8/GB2/CCC_NW0_CLKI1	8
G14	MSIO25PB1/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B	1	MSIO39PB1/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B	1
G2	MSIO96PB7/GB6/CCC_NW1_CLKI1	7	MSIO114PB8/GB6/CCC_NW1_CLKI1	8
H1	MSIOD100PB6/GB5/CCC_SW1_CLKI1	6	MSIOD118PB7/GB5/CCC_SW1_CLKI1	7
H20	MSIO20NB2/GB13/VCCC_SE1_CLKI/GPIO_26_A	2	MSIO20NB3/GB13/VCCC_SE1_CLKI/GPIO_26_A	3

Table 8 • **Equivalent Global Pins Per Device for M2S025 and M2S050 Devices *(continued)***

	VF400 Pin Names			
Package Pin	**M2S025**	**Bank No**	**M2S050**	**Bank No**
H5	MSIO98PB7/CCC_NW1_CLKI0	7	MSIO116PB8/CCC_NW1_CLKI0	8
J19	MSIO20PB2/GB9/VCCC_SE0_CLKI/GPIO_25_A	2	MSIO20PB3/GB9/VCCC_SE0_CLKI/GPIO_25_A	3
J2	MSIOD102PB6/CCC_SW1_CLKI0	6	MSIOD120PB7/CCC_SW1_CLKI0	7
J4	MSIOD101PB6/GB1/CCC_SW0_CLKI1	6	MSIOD119PB7/GB1/CCC_SW0_CLKI1	7
J7	MSIO99PB7/CCC_NW0_CLKI0	7	MSIO117PB8/CCC_NW0_CLKI0	8
K7	MSIOD103PB6/CCC_SW0_CLKI0	6	MSIOD121PB7/CCC_SW0_CLKI0	7
M17	MSIO11NB2/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A	2	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A	3
N16	MSIO11PB2/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A	2	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A	3
P2	MSIOD119PB5/SERDES_0_REFCLK1_P	5	MSIOD146PB6/SERDES_0_REFCLK1_P	6
P3	MSIOD119NB5/SERDES_0_REFCLK1_N	5	MSIOD146NB6/SERDES_0_REFCLK1_N	6
R1	MSIOD118PB5/SERDES_0_REFCLK0_P	5	MSIOD145PB6/SERDES_0_REFCLK0_P	6
R2	MSIOD118NB5/SERDES_0_REFCLK0_N	5	MSIOD145NB6/SERDES_0_REFCLK0_N	6

Table 9 • **Equivalent Global Pins Per Device for M2S060T(S) and M2S050T(S) Devices**

	VF400 Pin Names			
Package Pin	**M2S060T(S)**	**Bank No**	**M2S050T(S)**	**Bank No**
A1	DDRIO80PB1/GB0/CCC_NW0_CLKI3	1	DDRIO91PB0/GB0/CCC_NW0_CLKI3	0
A11	DDRIO64PB1/MDDR_DQ14/CCC_NE1_CLKI3	1	DDRIO75PB0/CCC_NE1_CLKI3/MDDR_DQ14	0
B1	DDRIO80NB1/GB4/CCC_NW1_CLKI2	1	DDRIO91NB0/GB4/CCC_NW1_CLKI2	0
C9	DDRIO67PB1/MDDR_DQS1/GB8/CCC_NE0_CLKI3	1	DDRIO78PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0
D10	DDRIO65PB1/MDDR_DQ12/GB12/CCC_NE1_CLKI2	1	DDRIO76PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0
D3	DDRIO81NB1/CCC_NW0_CLKI2	1	DDRIO92NB0/CCC_NW0_CLKI2	0
D9	DDRIO68PB1/MDDR_DQ10/CCC_NE0_CLKI2	1	DDRIO79PB0/CCC_NE0_CLKI2/MDDR_DQ10	0

Table 9 • **Equivalent Global Pins Per Device for M2S060T(S) and M2S050T(S) Devices *(continued)***

	VF400 Pin Names			
Package Pin	**M2S060T(S)**	**Bank No**	**M2S050T(S)**	**Bank No**
E18	MSIO43PB2/GB14/VCCC_SE1_CLKI	2	MSIO42PB1/GB14/VCCC_SE1_CLKI	1
F19	MSIO41PB2/CCC_NE1_CLKI1	2	MSIO40PB1/CCC_NE1_CLKI1	1
G1	MSIO124PB9/GB2/CCC_NW0_CLKI1	9	MSIO115PB8/GB2/CCC_NW0_CLKI1	8
G14	MSIO40PB2/CCC_NE0_CLKI1	2	MSIO39PB1/CCC_NE0_CLKI1	1
G2	MSIO123PB9/GB6/CCC_NW1_CLKI1	9	MSIO114PB8/GB6/CCC_NW1_CLKI1	8
H1	MSIOD142PB8/GB5/CCC_SW1_CLKI1	8	MSIOD118PB7/GB5/CCC_SW1_CLKI1	7
H20	MSIO20NB4/GPIO_26_A/GB13/VCCC_SE1_CLKI	4	MSIO20NB3/GB13/VCCC_SE1_CLKI	13
H5	MSIO125PB9/CCC_NW1_CLKI0	9	MSIO116PB8/CCC_NW1_CLKI0	8
J19	MSIO20PB4/GPIO_25_A/GB9/VCCC_SE0_CLKI	4	MSIO20PB3/GB9/VCCC_SE0_CLKI	3
J2	MSIOD144PB8/CCC_SW1_CLKI0	8	MSIOD120PB7/CCC_SW1_CLKI0	7
J4	MSIOD143PB8/GB1/CCC_SW0_CLKI1	8	MSIOD119PB7/GB1/CCC_SW0_CLKI1	7
J7	MSIO126PB9/CCC_NW0_CLKI0	9	MSIO117PB8/CCC_NW0_CLKI0	8
K7	MSIOD145PB8/CCC_SW0_CLKI0	8	MSIOD121PB7/CCC_SW0_CLKI0	7
M17	MSIO11NB4/CCC_NE1_CLKI0	4	MSIO11NB3/CCC_NE1_CLKI0	3
N16	MSIO11PB4/CCC_NE0_CLKI0	4	MSIO11PB3/CCC_NE0_CLKI0	3
P15	MSIO12PB4/SPI_0_CLK	4	MSIO12PB3/SPI_0_CLK	3

See, “Dedicated Global I/O Naming Conventions” section in the *SmartFusion2 Pin Descriptions*.

2.1.3.2 Available versus No Connect Pins

There are pins that have one specific function in one device but are “no connect” (NC) in another device. The following table lists the summary of these pins.

For example, pin Y17 functions as the XTLOSC_AUX_EXTAL pin in the M2S025 while it is an NC in the M2S050 device. Similarly, P13 pin is an NC in the M2S025 but it is a VREF5 pin in the M2S050 device.

When migrating from a device, where the I/O is an NC pin to a device where the I/O has a defined functionality but not used, follow the recommended methods for connecting the unused I/Os, depending on the functionality of that I/O. See “SmartFusion2 Unused Pin Configurations” in the *SmartFusion2 Board Design Guidelines Application Note*.

When migrating from a device, where the I/O has a defined functionality to a device where the I/O is an NC, the NC pins can be driven to any voltage or can be left floating with no effect on the operation of the device. NC indicates that the pin is not connected to circuitry within the device.

Table 10 • **Available versus NC Pins**

	VF400 Pin Names			
Package Pin	**M2S025**	**M2S050**	**M2S060T(S)**	**M2S050T(S)**
Y17	XTLOSC_AUX_EXTAL	NC	VPP	NC
W17	XTLOSC_AUX_XTAL	NC	VPP	NC
P13	NC	VREF5	NC	VREF5
R11	NC	VREF5	NC	VREF5

2.1.3.3 I/O Technology Compatibility Per Pin or Bank

The following table and Table 12, page 12 show the list of I/Os that would lead to incompatibility due to different I/O technologies supported, while migrating between M2S025 and M2S050 devices and M2S060T(S) and M2S050T(S) devices within the VF400 package. The difference is the type of I/O technology (MSIO Vs DDRIO) that is supported on those regular I/Os.

Table 11 • **I/O Standards Compatibility for Package Pins for M2S025 and M2S050 Devices**

Package Pin	VF400 Pin Names			
	M2S025	**Bank No**	**M2S050**	**Bank No**
R12	**MSIO**134NB4	4	**DDRIO**164NB5	5
R13	MSIO134PB4/VCCC_SE1_CLKI	4	DDRIO164PB5/VCCC_SE1_CLKI	5
T13	MSIO133NB4	4	DDRIO163NB5	5
T14	MSIO144PB4	4	DDRIO184PB5	5
T15	MSIO144NB4	4	DDRIO184NB5	5
U11	MSIO125NB4/GB7/CCC_SW1_CLKI2	4	DDRIO152NB5/GB7/CCC_SW1_CLKI2	5
U12	MSIO130NB4	4	DDRIO160NB5	5
U13	MSIO133PB4/GB15/VCCC_SE1_CLKI	4	DDRIO163PB5/GB15/VCCC_SE1_CLKI	5
U14	MSIO142NB4	4	DDRIO181NB5	5
V11	MSIO125PB4/GB3/CCC_SW0_CLKI3	4	DDRIO152PB5/GB3/CCC_SW0_CLKI3	5
V12	MSIO130PB4/VCCC_SE0_CLKI	4	DDRIO160PB5/VCCC_SE0_CLKI	5
V14	MSIO142PB4	4	DDRIO181PB5	5
V15	DDRIO181PB5	4	DDRIO190NB5	5
W10	MSIO120NB4/CCC_SW0_CLKI2	4	DDRIO147NB5/CCC_SW0_CLKI2	5
W12	MSIO121NB4/PROBE_B	4	DDRIO148NB5/PROBE_B	5
W13	MSIO131PB4/GB11/VCCC_SE0_CLKI	4	DDRIO161PB5/GB11/VCCC_SE0_CLKI	5
W14	MSIO131NB4	4	DDRIO161NB5	5
W15	MSIO146PB4	4	DDRIO190PB5	5
Y10	MSIO120PB4	4	DDRIO147PB5	5

Table 11 • **I/O Standards Compatibility for Package Pins for M2S025 and M2S050 Devices *(continued)***

Package Pin	VF400 Pin Names			
	M2S025	**Bank No**	**M2S050**	**Bank No**
Y11	MSIO121PB4/PROBE_A	4	DDRIO148PB5/PROBE_A	5
Y12	MSIO129PB4/CCC_SW1_CLKI3	4	DDRIO159PB5/CCC_SW1_CLKI3	5
Y13	MSIO129NB4	4	DDRIO159NB5	5
Y15	MSIO145PB4	4	DDRIO187PB5	5
Y16	MSIO145NB4	4	DDRIO187NB5	5

Table 12 • **I/O Standards Compatibility for Package Pins for M2S060T(S) and M2S050T(S) Devices**

Package Pin	VF400 Pin Names			
	M2S060T(S)	**Bank No**	**M2S050T(S)**	**Bank No**
R12	MSIO179NB6	6	DDRIO164NB5	5
T13	MSIO178NB6	6	DDRIO163NB5	5
T14	MSIO191PB6	6	DDRIO184PB5	5
T15	MSIO191NB6	6	DDRIO184NB5	5
U12	MSIO175NB6	6	DDRIO160NB5	5
U14	MSIO187NB6	6	DDRIO181NB5	5
V14	MSIO187PB6	6	DDRIO181PB5	5
V15	MSIO195NB6	6	DDRIO190NB5	5
W12	MSIO163NB6/PROBE_B	6	DDRIO148NB5/PROBE_B	5
W14	MSIO176NB6	6	DDRIO161NB5	5
W15	MSIO195PB6	6	DDRIO190PB5	5
Y10	MSIO162PB6	6	DDRIO147PB5	5
Y11	MSIO163PB6/PROBE_A	6	DDRIO148PB5/PROBE_A	5
Y13	MSIO174NB6	6	DDRIO159NB5	5
Y15	MSIO199PB6	6	DDRIO187PB5	5
Y16	MSIO199NB6	6	DDRIO187NB5	5

The DDRIOs do not support single ended 3.3 V I/O standards and differential LVPECL, LVDS 3.3 V, LVDS 2.5 V, RSDS BLVDS, MLVDS, and Mini-LVDS I/O standards, as shown in the following table. To migrate between M2S025 and M2S050 successfully, ensure that the correct VDDI power supply is used to power the equivalent banks. Only I/Os with compatible standards can be assigned to the same bank.

Table 13 • **Technology Support Difference Between Different I/O Types**

	I/O Types	
I/O Standards	**MSIO**	**DDRIO**
Single-Ended I/O		
LVTTL 3.3V	Yes	–
LVCMOS 3.3V	Yes	–
PCI	Yes	–
LVCMOS 1.2V	Yes	Yes

Table 13 • **Technology Support Difference Between Different I/O Types**

	I/O Types	
I/O Standards	**MSIO**	**DDRIO**
LVCMOS 1.5V	Yes	Yes
LVCMOS 1.8V	Yes	Yes
LVCMOS 2.5V	Yes	Yes
Voltage-Referenced I/O		
HSTL 1.5V	Yes	Yes
SSTL 1.8	Yes	Yes
SSTL 2.5	Yes	Yes
SSTL 2.5 V(DDR1)	Yes	Yes
SSTL 1.8 V(DDR2)	Yes	Yes
SSTL 1.5 V (DDR3)	Yes	Yes
Differential I/O		
LVPECL (input only)	Yes	–
LVDS 3.3 V	Yes	–
LVDS 2.5 V	Yes	–
RSDS	Yes	–
BLVDS	Yes	–
MLVDS	Yes	–
Mini-LVDS	Yes	–

Note: Even though the VDDI may be the same (for example, MSIO 2.5 V and DDRIO 2.5 V), the attributes and features supported may be different between different I/O types (MSIO versus DDRIO). For more information on the list of features supported per I/O type, see “I/O Programmable Features” section in the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

2.1.3.4 Oscillator Pins

SmartFusion2 devices include two crystal oscillators, main crystal oscillator and auxiliary crystal oscillator.

Note: SmartFusion2 M2S050 devices do not have an auxiliary crystal oscillator.

The auxiliary crystal oscillator is dedicated for RTC clocking as an alternative clock source. Both the main and auxiliary crystal oscillators have two I/O pads, as shown in the following table, which can be connected externally to a crystal, a ceramic resonator, or an RC circuit.

When migrating from a device, where the I/O is an NC pin to a device where the I/O has a defined functionality but not used, follow the recommended methods for connecting the unused I/Os depending on the functionality of that I/O. For more information see, “SmartFusion2 Unused Pin Configurations” in the *SmartFusion2 Board Design Guidelines Application Note*.

When migrating from a device, where the I/O has a defined function to a device where the I/O is an NC, the NC pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

Table 14 • **Crystal Oscillator Pins Per Device**

	VF400 Pin Names	
Package Pin	**M2S025**	**M2S050**
W17	XTLOSC_AUX_XTAL	NC
Y17	XTLOSC_AUX_EXTAL	NC
Y18	XTLOSC_MAIN_XTAL	XTLOSC_MAIN_XTAL
W18	XTLOSC_MAIN_EXTAL	XTLOSC_MAIN_EXTAL

2.1.3.5 Probe Pins

Probe pin locations are compatible between the two devices. The following table shows different probe I/Os location per device within the VF400 package. By default, probe pins are reserved for the probe functionality. Unreserve these pins by clearing the **Reserve Pins for Probes** check box in the "**Device I/O Settings"** under Project Setting in Libero SoC software. When the pins are not reserved, the probe I/Os can be used as regular I/Os.

Note: Different I/O technologies are supported on these pins (MSIO versus DDRIO). See I/O Technology Compatibility Per Pin or Bank, page 11 for more information.

Table 15 • **Probe Pins Per Device**

Package Pin	**VF400 Pin Names**			
	M2S025	**Bank No**	**M2S050**	**Bank No**
W12	**MSIO**121NB4/PROBE_B	4	**DDRIO**148NB5/PROBE_B	5
Y11	**MSIO**121PB4/PROBE_A	4	**DDRIO**148PB5/PROBE_A	5
Package Pins	**M2S060T(S)-VF400**	**Bank No**	**M2S050T(S)-VF400**	**Bank No**
W12	MSIO163NB6/PROBE_B	6	DDRIO148NB5/PROBE_B	5
Y11	MSIO163NB6/PROBE_A	6	DDRIO148PB5/PROBE_A	5

2.1.4 Power Supply and Board-Level Considerations

I/O power supply requirements are one of the key aspects to consider for design migrations. Since the migration is within the SmartFusion2 family, there is no issue regarding the core voltage (VDD), charge pumps voltage (VPP), and analog sense circuit supply of the eNVM voltage (VPPNVM). The ground pins (VSS) are also equivalent between M2S025 and M2S050 devices. See the *SmartFusion2 Pin Descriptions* for more details. The bank supply VDDI Pins must be connected to appropriate voltage. All the bank supplies that are located on the east-side must be powered even if the associated bank I/Os are not used. When specific banks are not used, see, "Recommendation for Unused Bank Supplies" connections table in the *SmartFusion2 Board Design Guidelines Application Note* for more information. An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltages and an MSIOD and DDRIO bank supports 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltages. For more details on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, see the "Supported Voltage Standards" table in the *SmartFusion2 FPGA Fabric Architecture User's Guide*.

The banks have dedicated supplies. I/Os with compatible voltage standards can only be assigned to the same I/O voltage bank. The correct bank supply must be used when migrating between the different

devices as per the appropriate voltages (I/O Standards) selected for the bank. The following tables show power supply compatibility per device in the VF400 package for different banks.

Table 16 • **Power Supply Compatibility Per Device for M2S025 and M2S050 Devices**

	VF400 Pin Names	
Package Pin	**M2S025**	**M2S050**
F2	VDDI7	VDDI8
G5	VDDI7	VDDI8
H18	VDDI2	VDDI3
J1	VDDI6	VDDI7
J8	VDDI7	VDDI8
K4	VDDI6	VDDI7
L17	VDDI2	VDDI3
L8	VDDI6	VDDI7
M20	VDDI2	VDDI3
N14	VDDI2	VDDI3
N3	VDDI6	VDDI7
P16	VDDI2	VDDI3
R14	VDDI3	VDDI4
R19	VDDI2	VDDI3
R3	VDDI5	VDDI6
T12	VDDI4	VDDI5
U15	VDDI4	VDDI5
V18	VDDI2	VDDI3
W11	VDDI4	VDDI5
Y14	VDDI4	VDDI5

Table 17 • **Power Supply Compatibility Per Device for M2S060T(S) and M2S050T(S) Devices**

Package Pin	**M2S060T(S)**	**M2S050T(S)**
A17	VDDI1	VDDI0
A7	VDDI1	VDDI0
B20	VDDI2	VDDI1
C13	VDDI1	VDDI0
C3	VDDI1	VDDI0
D16	VDDI1	VDDI0
E19	VDDI2	VDDI1
E9	VDDI1	VDDI0
F2	VDDI9	VDDI8
G10	VDDI1	VDDI0
Package Pin	**M2S060T(S)**	**M2S050T(S)**

Table 17 • Power Supply Compatibility Per Device for M2S060T(S) and M2S050T(S) Devices *(continued)*

G12	VDDI1	VDDI0
G15	VDDI2	VDDI1
G5	VDDI9	VDDI8
G8	VDDI1	VDDI0
H18	VDDI4	VDDI3
J1	VDDI8	VDDI7
J8	VDDI9	VDDI8
K4	VDDI8	VDDI7
L17	VDDI4	VDDI3
L8	VDDI8	VDDI7
M20	VDDI4	VDDI3
N14	VDDI4	VDDI3
N3	VDDI8	VDDI7
P16	VDDI4	VDDI3
R14	VDDI5	VDDI4
R19	VDDI4	VDDI3
R3	VDDI7	VDDI6
T12	VDDI6	VDDI5
U15	VDDI6	VDDI5
W11	VDDI6	VDDI5
Y14	VDDI6	VDDI5

For other bank supplies that are equivalent, see the provided recommendations in the *SmartFusion2 Pin Descriptions*.

Board-level considerations are common among the three devices. See the *SmartFusion2 Board Design Guidelines Application Note* for more details.

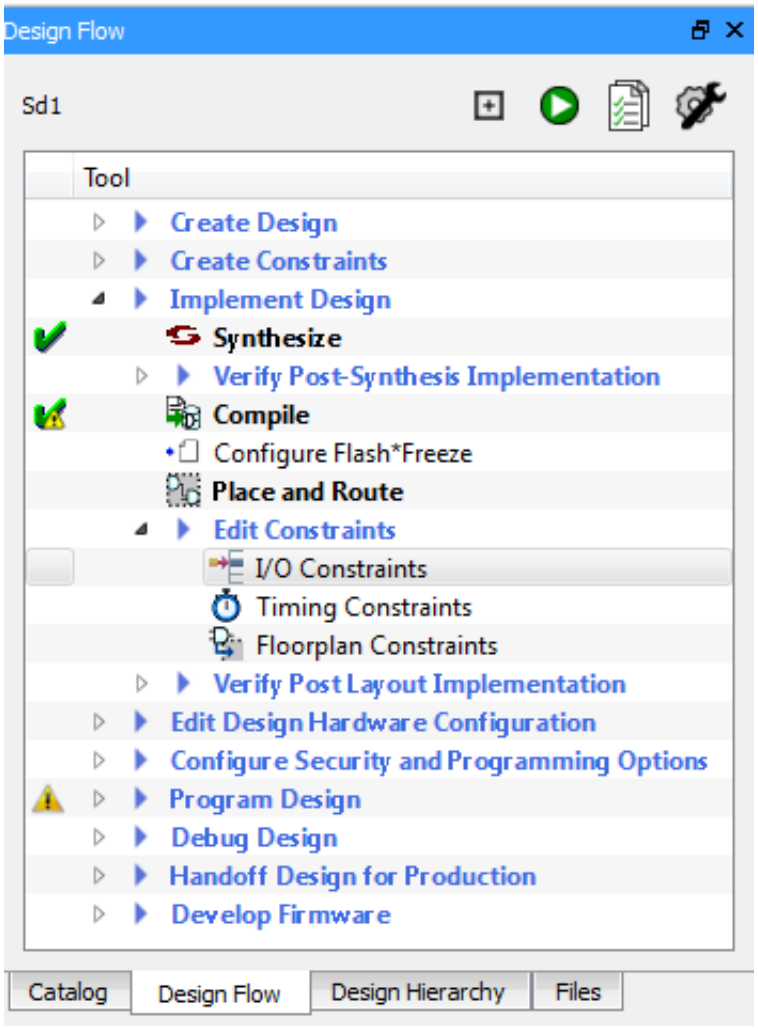
2.1.5 Software Flow

The Libero SoC Software provides the option of reserving pins for migration between different devices within the SmartFusion2 family where pins within the current device that are not bonded to the destination device can be automatically reserved. This option is available in **I/O Constraints Editor** which can be accessed from the **Design Flow** window as shown in Figure 3, page 17. This step is performed in the early stages of the design cycle.

The following procedure is done to reserve pins:

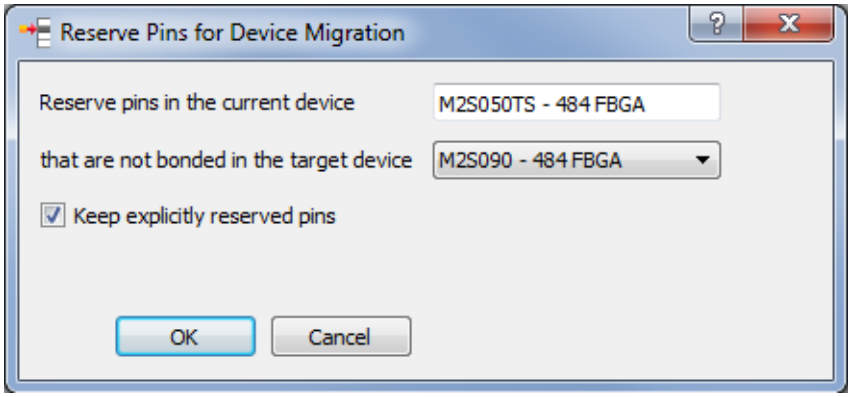
1. After finishing the **Compile** process, select the **I/O Constraints** option from the **Design Flow** window as shown in the following figure.

Figure 3 • **I/O Constraint Editor Option part of the Design Flow**



2. Select the **Reserve Pins for Device Migration** option from the Tools menu. The following figure shows the displayed window.

Figure 4 • **Reserve Pins for Device Migration**

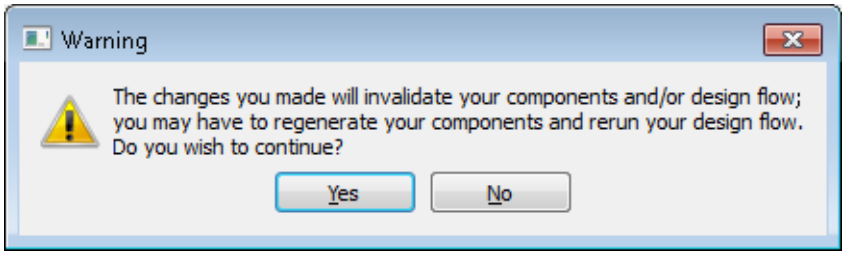


The first option shows the device that is currently being used in the Libero SoC project. From the drop-down list, select the device that eventually will be migrated to the target device. See, *Libero Soc software online help* for more details on this window and other options.

The Libero SoC software provides the option of migration between different devices within the SmartFusion2 family by modifying the device selection, using the **Project Settings** option in the Libero SoC software. Upon changing the device, Libero SoC software validates the features that are used within the design against the supported features within the new targeted device and package. Feedback messages are provided as part of the Libero SoC software flow, listing the different actions taken by Libero SoC.

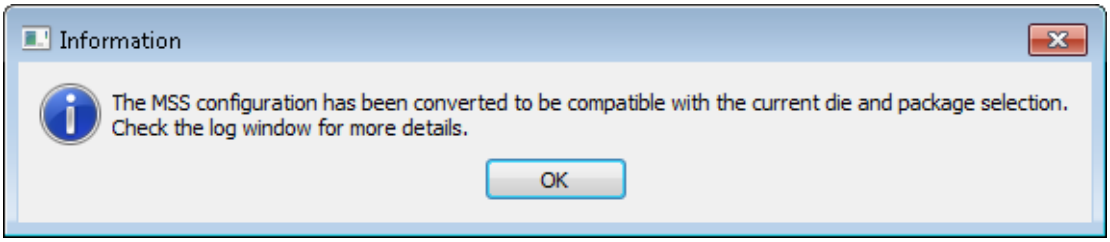
The first step that Libero SoC performs upon changing the device is to validate the original design components and the design flows. The message is displayed as shown in the following figure.

Figure 5 • **Invalidating Component and Design Flow Message**



As part of re-running the design flow, Libero SoC checks the different steps needed to be performed for completing and updating the design flow. Furthermore, Libero SoC converts the MSS configurations to be compatible with the selected device and package combination. It displays the message as shown in the following figure.

Figure 6 • **Converting the MSS Configurations**



As part of the MSS conversion, any changes that were made automatically to be compatible with the selected device and package, will be printed to the log window. Libero SoC disables or defaults to different options, if the current selected options are not supported in the new targeted device and package.

After the MSS configuration conversion is done, the MSS must be regenerated. To regenerate the MSS component, open the MSS component from **Libero SoC Design Hierarchy Flow** window and proceed through different MSS pages to complete the generation.

2.2 Conclusion

This application note describes the design migration among SmartFusion2 family devices focusing on migration between M2S025 and M2S050,M2S060T(S) and M2S050T(S) devices within the VF400 package. During design migration, architecture differences between devices should be considered to ensure seamless migration flow. A key requirement is to run the functional simulation and timing analysis using Microsemi tools, before and after the migration.