UG0468
User Guide
Space Vector Modulation v4.1

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Power Matters.™

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- Added the IP version to the document title.
- Removed Configuration Parameter section from Hardware Implementation, page 4.

1.2 Revision 4.0

Removed FSM related information from SVM Hardware Implementation and Configuration Parameters sections (SAR 69654).

1.3 Revision 3.0

Changed the block name from SVPWM to SVM throughout the document (SAR 64768).

1.4 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated the title of the user guide (SAR 63243).
- Updated Min-Max Method, page 2 section and removed Direct Injection of Third Harmonic section (SAR 63243).
- Updated Table 1, page 4 and Table 2, page 5 (SAR 63243).
- Removed Appendix (SAR 63243).

1.5 Revision 1.0

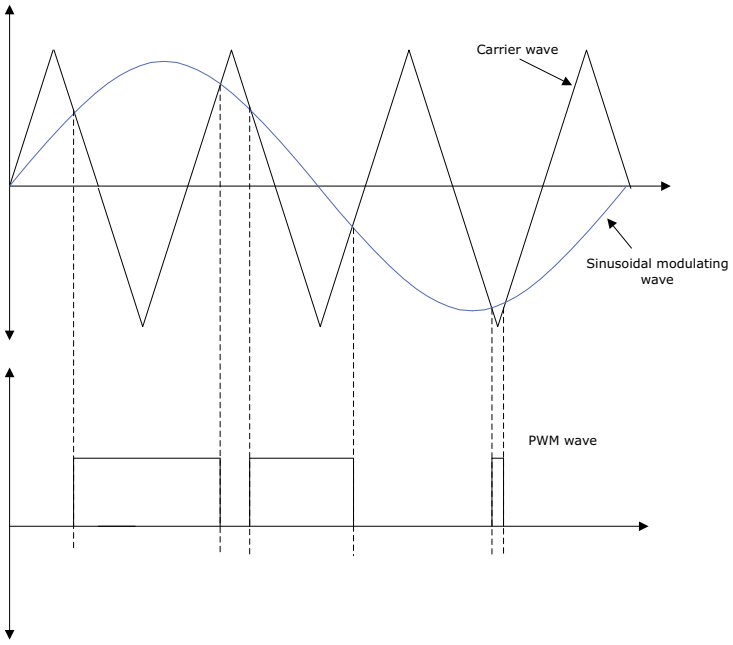
Revision 1.0 was the first publication of this document.

2 Introduction

Space vector modulation (SVM) is an improved technique for generating a fundamental sine wave that provides a higher voltage to the motor in a 3-phase system, lower total harmonic distortion, and controls the number of short pulses in the PWM waveform.

A sinusoidal PWM drive cannot provide a line-line output voltage as high as the line supply.

Figure 1 • **Sinusoidal PWM Waveform**



SVM is a technique that is used to increase the output voltage of PWM drive and reduce the number of short pulses. The strategy used in SVM technique is to modify the modulation of sine waves (input phase voltages) to increase the inverter voltage gain and also to reduce inverter losses.

2.1 Min-Max Method

There are many techniques to implement SVM out of which Min-Max method requires least computation and is used in the IP block. The third harmonic voltage is generated from min and max values of instantaneous 3-phase reference voltages. The third harmonic voltage (V_{3H}) is calculated as:

$$V_{3H} = \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2}$$

The computed third harmonic voltage is added to each phase voltage to get space vector modulated reference.

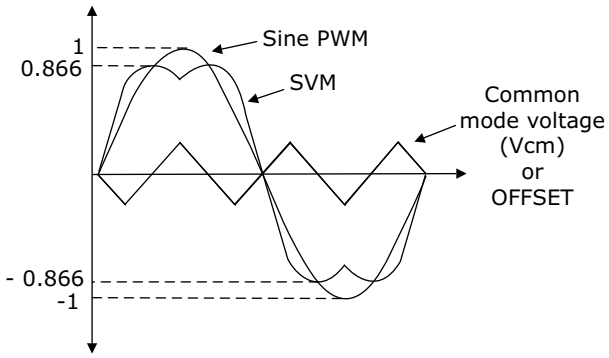
$$V_{SA} = V_A - V_{3H}$$

$$V_{SB} = V_B - V_{3H}$$

$$V_{SC} = V_C - V_{3H}$$

The addition of third harmonic reduces the peak of the reference signal by 15% and hence allows more fundamental without reaching over-modulation. Even though third harmonic is added in phase voltages, it does not appear in line voltages because it is common mode voltage. As a result, there is no third harmonic current but only fundamental current. For a given modulation index, the peak modulation voltage is farther from the peak carrier voltage. Thus, the number of short pulses is minimized. To utilize the DC bus fully, the voltages must be scaled up by 15% in one of the blocks that follows the SVM in the FOC loop.

Figure 2 • **SVM Min-Max Method**

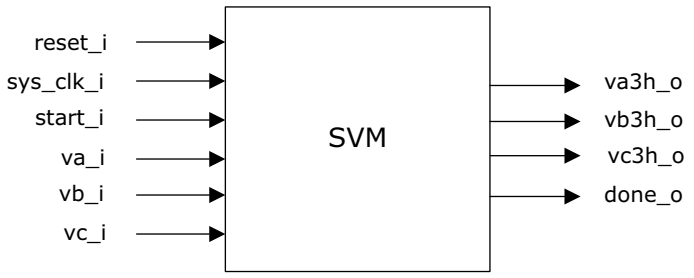


If the output should be a unity peak value and the reduction in peak introduced by the block is 0.866, the factor k must be 1.155 (k * 0.866 = 1, k=1/0.866).This implies that there is a 15.5 percent boost introduced in the phase voltage, which results in better utilization of the DC bus.

3 Hardware Implementation

The following figure shows the block diagram of the SVM block implemented.

Figure 3 • **SVM Hardware Block Diagram**



The SVM block is a control unit which implements the Min-Max method discussed in the Min-Max Method, page 2. The computations involved in the Min-Max method are performed within the block.

The entire system is synchronized with a system clock given to sys_clk_i and controlled by a finite state machine (FSM) and then implemented in the SVM block.

3.1 Inputs and Outputs

The following table lists the description of the input and output ports of the SVM block.

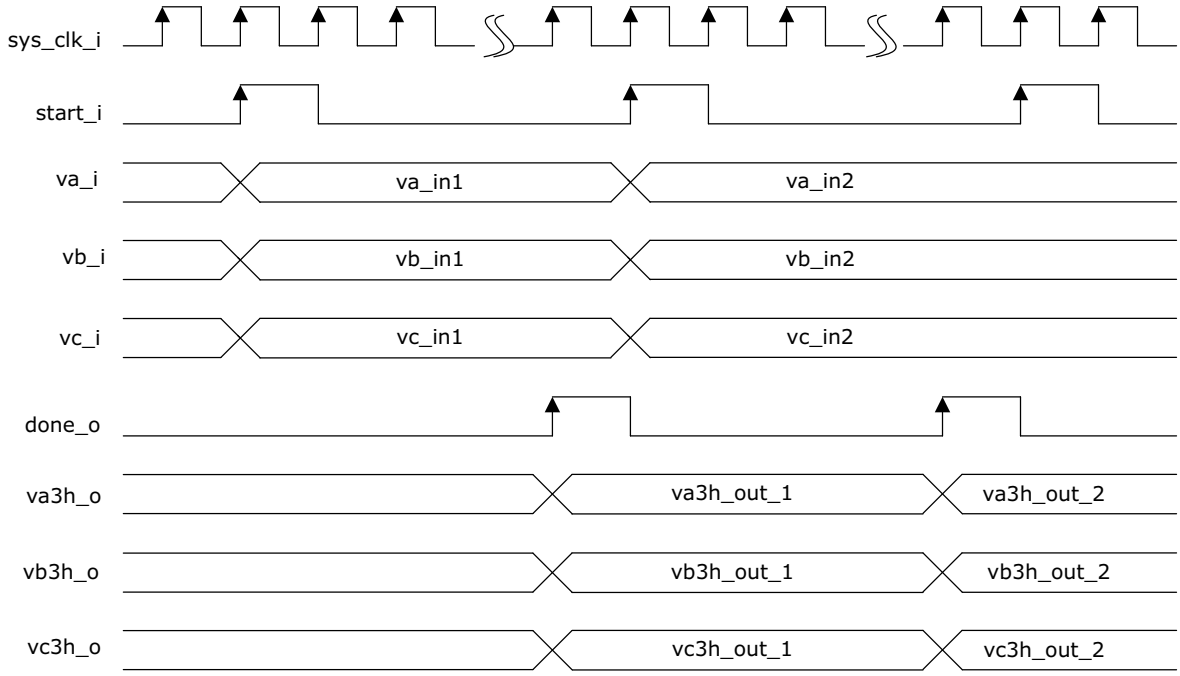
Table 1 • **Inputs and Outputs of SVM**

Signal Name	Direction	Description
sys_clk_i	Input	System clock
reset_i	Input	Active Low asynchronous reset signal to design
start_i	Input	A single bit start signal that must go high for one clock cycle to start SVM computations
va_i	Input	Input phase voltage (va)
vb_i	Input	Input phase voltage (vb)
vc_i	Input	Input phase voltage (vc)
va3h_o	Output	Output voltage signal corresponding to input phase voltage va_i, with the third harmonic component
vb3h_o	Output	Output voltage signal corresponding to input phase voltage vb_i, with the third harmonic component
vc3h_o	Output	Output voltage signal corresponding to input phase voltage vc_i, with the third harmonic component
done_o	Output	A single bit signal which goes High for one clock cycle to indicate that all the computations are done and output corresponding to given inputs is obtained

3.2 Timing Diagram

The following figure shows the timing diagram of the SVM block.

Figure 4 • **SVM Timing Diagram**



3.3 Resource Utilization

The following table lists the resource utilization report of the SVM in the SmartFusion®2 system-on-chip (SoC) field programmable gate array (FPGA) device.

Table 2 • **SVM Resource Utilization**

Resource	Usage
Sequential elements	90
Combinational logic	240
MACC	0
RAM1kx18	0
RAM64x18	0