Unified Synchronization Solution for Mobile Backhaul

This white paper is a joint collaboration between Symmetricom and PMC-Sierra.

About PMC

PMC is the semiconductor innovator transforming networks that connect, move and store big data. Building on a track record of technology leadership, the Company is driving innovation across storage, optical and mobile networks. PMC's highly integrated solutions increase performance and enable next-generation services to accelerate the network transformation. WWW.PMCS.COM

SyncWorld® ECOSYSTEM PROGRAM

To meet new synchronization and timing requirements that support the transition to packetized backhaul networks and 4G / LTE mobile platforms, Symmetricom® has established the SyncWorld® Ecosystem Program to enable interoperability and cooperation among the vendors who will deliver on service providers' advanced networking requirements.

In today's mobile backhaul, a cell site router or gateway that can exist in the form of a pizza box or a small chassis and placed near base stations. In addition to providing traffic aggregation, transport, and other data plane/control plane functions, such cell site routers also need to provide synchronization to the base stations. This usually involves the following two primary objectives:

- The ability to acquire synchronization from various available sources
- The ability to select the best source with fallback protection

The definition of synchronization depends on the type of base station. 2G or 3G FDD base stations require a stable frequency and a frequency sync precision of 50 ppb. 4G base stations require extra phase lock which is usually delivered in the form of a one second (1Hz) frame pulse phase - aligned with the seconds tick of a global reference such as TAI or UTC (also known as 1PPS). Once the 1PPS phase lock is acquired, Time of Day (ToD) synchronization is easily achievable.

There are different technologies to acquire frequency or phase synchronization such as:

- For frequency synchronization: IEEE 1588, GPS, Synchronous Ethernet (SyncE), T1/E1, SONET/SDH, xDSL, xPON
- For phase synchronization: IEEE 1588, GPS, IEEE 802.1as

Many of the above synchronization technologies are mature and widely deployed and hence not difficult to implement a solution for each one of them. In fact, this is what is done today. The bigger challenge is to integrate them to build a unified solution that can deliver the desired objectives with minimum cost and development effort.

What is Unified Synchronization?

As shown in Figure 1, a unified synchronization solution has inputs that include all possible timing reference (master) sources a system looks to support simultaneously and outputs that are a combination of clock, 1PPS and ToD information. The outputs should lock to the selected master source at any time, through an extended Phase Lock Loop (PLL) or Frequency Lock Loop (FLL) function. The master source is dynamically selected based on certain criteria that includes the stratum level, quality and the run-time status of all available input sources. All sources, even when they are not selected as the master source, should be monitored at all times so as to provide fallback protection and very little disruption on reference switching.

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The extended PLL supports not only the conventional PLL functions such as frequency synthesis needed to generate a desired output clock frequency, and a servo algorithm to lock output frequency to a master source, but should also include a frame pulse creation and phase alignment capabilities.

It is possible and may be desirable to have a different master source for frequency and phase synchronization. For example, a system that has only Ethernet interfaces, can select SyncE for frequency synchronization, and IEEE 1588 for 1PPS and ToD synchronization. The system can fall back to IEEE 1588 for both frequency and phase synchronization when SyncE becomes unavailable.

A unified solution should also include integral support for all control plane stacks such as Sync Status Message (SSM) for BITS, Ethernet Synchronization Message Channel (ESMC) for SyncE and Precision Time Protocol (PTP) for IEEE 1588.

Design Considerations

Performance and cost optimization are two major needs of any system design. In the unified synchronization solution, performance is predominantly determined by the following factors:

- A properly selected local oscillator with sufficient stability
- Hardware assisted time-stamping of the arrival/departure of PTP event messages and the occurrence of other events to support IEEE 1588 based synchronization to achieve a measure of high accuracy
- A hardware based frequency synthesizer with sufficient accuracy for the frequency control of the output clock
- A robust servo algorithm that can track the master source quickly and accurately
- Quick detection of any impairment in the input timing source

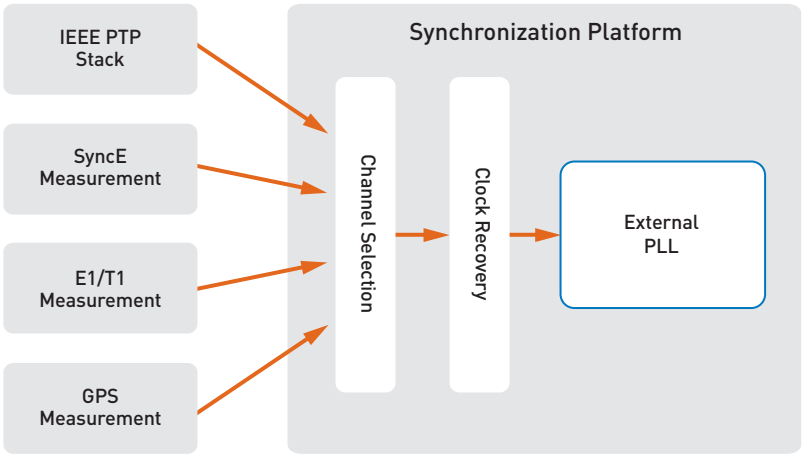

Figure 1. Functional diagram of a unified synchronization solution

- Intelligent selection of a master source with a smooth transition during switch over

One way of reducing the total cost is to minimize the use of hardware components, and to move as many functions as possible to a software plus firmware implementation. Listed below are examples of some functions that when implemented as a software-firmware combination will offer some excellent benefits compared to a hardware solution, such as:

- A servo runs on a CPU to produce clock recovery and filtering functions when coupled with a built-in synthesizer function on a network processor lowers the overall system cost due to the elimination of a hardware PLL
- The programmable and upgradable nature of the servo lends itself better for future proof (extensible and flexible)
- In general, a software solution offers higher flexibility when integrating with other software functions and reducing the overall system design and integration effort

At the core of any cell site router there exists a packet processor that is used for data path processing. Since the IEEE 1588 packets and SyncE interfaces share the same Ethernet ports with the packet processor, a few of the conventional data path vendors include hardware assisted synchronization functions and blocks with their packet processor. Some of the state-of-the-art packet/network processors now offer hardware assisted time-stamping circuit, IEEE 1588 timestamp counters, on-the-fly timestamp insertion or updating, and SyncE clock extraction functions. This allows a further reduction of dedicated hardware components required to implement a unified synchronization solution.

By moving as much functionality as possible into a software implementation, and by using the built-in hardware support from packet/network processors for those functions that can only be achieved in hardware, a unified synchronization solution can be implemented with a reduced Bill of Material (BOM) cost while still delivering acceptable performance.

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Implementation Example

The unified synchronization solution has been implemented and verified as a joint effort by PMC-Sierra and Symmetricom. The hardware implementation is based on one main component – a Winpath3 (WP3) network processor, with some small amount of additional logic that can be easily implemented with a small low density CPLD or FPGA.

WP3 is a network processor that will handle all the data path traffic in a cell site router. It terminates up to 16 Gigabit Ethernet (GE) ports, as well as 16 T1/E1 lines. WP3 also embeds necessary hardware supports for unified synchronization when processing and forwarding the Ethernet and TDM traffic. Specifically, it features:

- Hardware implemented timestamp counters compliant with IEEE 1588 format
- Hardware implemented time-stamping capability on packet arrival and departure on any GE port
- Timestamp insertion on packet departure (for "one-step" IEEE 1588 operation)
- A clock synthesizer for output frequency generation
- 1PPS output and input
  - Ability to support IEEE 1588 Ordinary Clock and Boundary Clock
- Residence time calculation and correction
  - Ability to support IEEE 1588 Transparent Clock
- Extraction and output of SyncE clocks from GigE Serdes lanes
  - Ability to support SyncE slave
- Synchronize GigE Serdes transmit clock to external reference
  - Ability to support SyncE master
- Embedded CPU (MIPS architecture processor)

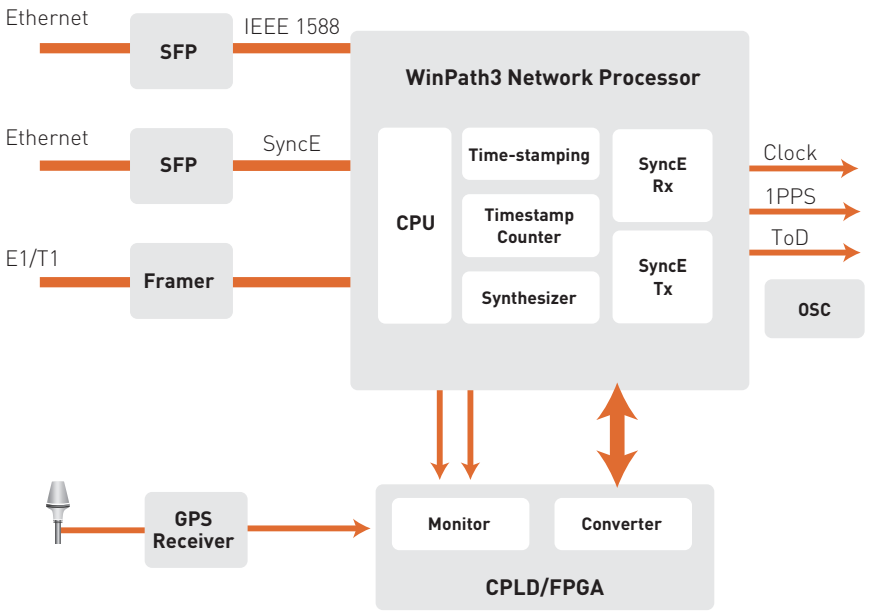

Figure 2. Example of hardware implementation of a unified synchronization solution

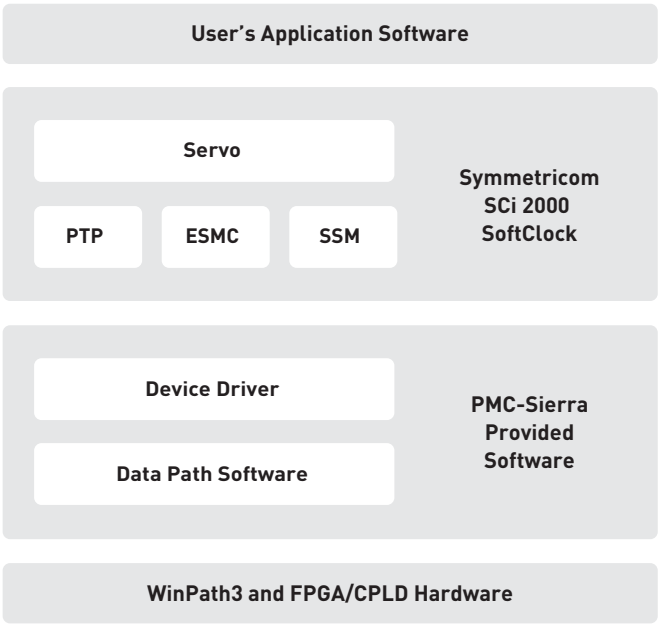

Figure 3. Example of software implementation of a unified synchronization solution

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Some CPLD/FPGA resources are used to implement glue logic and other additional functions needed for GPS input, as well as clock monitoring circuits. In the example being discussed, there is no dedicated device or external component added to implement a synchronization solution except for the local oscillator. All functions are implemented on network processor and a low cost, low density FPGA or CPLD.

Symmetricom's SCi 2000 SoftClock software package has been ported to the Linux operating system to run on the WP3 network processor and integrates a best-in-class servo algorithm and control stacks for IEEE 1588, SyncE and BITS, enabling it to do a smooth fallback between different timing sources.

This implementation has been verified to pass all G.8261 performance tests. The implementation provides a low cost, fully integrated and high performance synchronization solution. It is a truly turnkey solution for anyone looking for a unified synchronization solution for cell site router or gateway equipment for today's mobile backhaul.

Conclusion

New designs of cell site routers or gateways are looking for the next generation of synchronization solutions, which involves the unification of various synchronization technologies as a completely integrated solution. Such a solution needs to be low cost, high performance and turnkey. By implementing clock recovery, filtering and other functions in software-firmware combination and selecting data path processors with built-in hardware synchronization support are two important strategies to achieve this goal. PMC-Sierra's WinPath3 network processor and Symmetricom's SCi 2000 SoftClock have been integrated to deliver a solution that is ideal for next generation mobile backhaul.

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