The MAC – A Miniature Atomic Clock

R. Lutwak and P. Vlitas
Symmetricom - Technology Realization Center
Beverly, MA
U.S.A.
RLutwak@Symmetricom.com

M. Varghese and M. Mescher
Charles Stark Draper Laboratory
Cambridge, MA
U.S.A.

D.K. Serkland and G.M. Peake
Sandia National Laboratories†
Albuquerque, NM
U.S.A.

Abstract— **The authors are developing a chip-scale atomic clock (CSAC), more than two orders of magnitude smaller and lower power than any existing technology. As an intermediate milestone, en route to the ultimate CSAC objectives, we have developed a Miniature Atomic Clock (MAC), combining the low-power CSAC physics package with a low-parts count, low-power digital control and microwave system. The MAC is a complete packaged atomic clock, with overall size of 10 cm^3, power consumption <200 mW, and short-term stability $\sigma_y(\tau) \approx 4 \times 10^{-10} \tau^{-1/2}$.**

The MAC provides a valuable testbed for the further development and refinement of the CSAC physics package as well as for the development of the CSAC control electronics prior to undertaking the costly and time-consuming size-reduction effort which will be necessary to meet the ultimate CSAC objectives. The MAC itself may find applications in commercial and military timing systems which require the relatively small size and power consumption of the MAC now, rather than wait for the evolution of the 1 cm^3, 30 mW CSAC.

I. Introduction

Atomic clocks play an essential role in the timing and synchronization of modern communications and navigation systems. To date, the relatively large size and power consumption of existing technologies have prevented the deployment of precise timing in portable, battery-powered applications. However, the demand for high precision timing in portable devices is steadily increasing with the emergence of broadband and secure communications and precise location and navigation systems.

Since 2002, the authors have been developing a Chip-Scale Atomic Clock (CSAC), with an emphasis on small size, low-power, and batch fabrication techniques for lower cost. The design goals include short-term stability of $\sigma_y(\tau\text{=1hr}) < 1 \times 10^{-11}$, with a total power consumption of less than 30 mW and overall device volume of <1 cm^3. At PTTI 2002, we reported on initial experimental investigations leading to the decision to develop an architecture based on the coherent-population-trapping (CPT) interrogation technique [1]. At PTTI 2003 we reported on experimental measurements comparing CPT interrogation on the D1 and D2 resonance lines of cesium and leading to the decision to base the CSAC on the D1 resonance [2]. At PTTI 2004 we described the architecture and initial development of a novel folded-optics interrogation geometry and an ultra-low power physics package, capable of realizing the stability goals of the CSAC, while consuming less than 10 mW [3]. The mechanical and thermal aspects of the physics package have been explored in greater detail in [4].

In this paper, we report on the development of a prototype MAC, a Miniature Atomic Clock, combining the physics package described previously with a low-parts count, low-power digital control system, and a relatively low power microwave system.

II. MAC Physics Package

A. Architecture

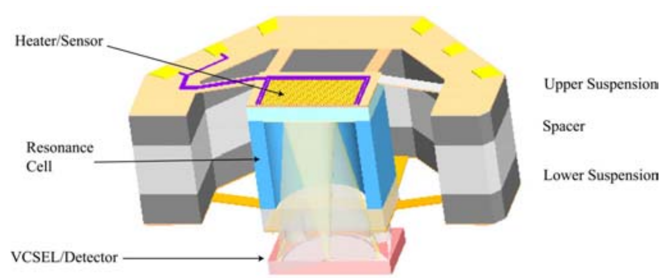


Figure 1. Physics Package Architecture

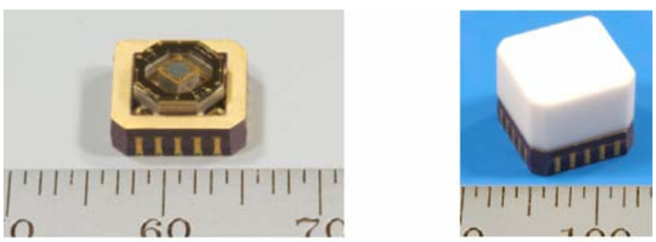
The MAC physics package is illustrated in Figure 1, above. For complete details of the physics package design, please refer to [3]. The resonance cell is comprised of a silicon body 2 mm square and 1.5 mm thick with anodically-bonded Pyrex® windows. The sealed cell contains a small amount of metallic cesium as well as a temperature-

---

† Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000

This work is supported by the Defense Advanced Research Products Agency, Contract # NBCHC020050.

compensated mixture of buffer gases. The cell is illuminated from below by a Vertical-Cavity Surface-Emitting Laser (VCSEL), which is located at the center of an annular Resonant-Cavity Photodiode (RCPD). Light from the VCSEL is circularly polarized by transmission through a $\lambda/4$ phase retarder before entering the cell. The polarized light enters the cell through the lower Pyrex® window and is retro-reflected back onto the RCPD by the mirrored inner surface of the upper window, passing through the cesium vapor twice in the round-trip. The natural divergence of the VCSEL beam effectively interrogates the entire cell volume along the propagation path. The cell assembly is suspended by rugged, thermally-isolating, polyimide tethers and is temperature stabilized at 80°C by a resistive platinum heater, patterned on the upper support. Electrical connections to and from the physics assembly are also patterned onto the polyimide, so that their dimensions (and thermal resistance) may be dictated by electrical, rather than mechanical, requirements. The suspensions are fabricated from spin-on photodefinable polyimide on a silicon substrate, and released by a backside through-etch of the silicon to produce the top and bottom (dark gray) suspension assemblies in Figure 1. A controlled strain is created in the polyimide tethers during the assembly process by the spacer between the suspensions, which is slightly shorter than the length of the resonance cell assembly. The magnitude of the strain is optimized for ruggedness and vibration isolation.



(a) (b)

Figure 2. Physics package in ceramic LCC

The complete physics package assembly is mounted in an off-the-shelf ceramic leadless chip carrier as shown in Figure 2. A ceramic cover may be brazed to seal the physics package in vacuum to eliminate heat loss via gaseous convection and conduction. With vacuum sealing the physics package is able to operate at an oven temperature of 80°C in a 25°C ambient, while dissipating <10 mW.

One unique characteristic of this physics package architecture, compared to other proposed CSAC designs, is that the VCSEL is temperature stabilized at the resonance cell operating temperature. This places extraordinary demands on the VCSEL, both because of reduced reliability at elevated temperatures and also because it demands stringent tolerance on the VCSEL wavelength. This compromise is inescapable in developing a clock intended for insertion in real-world applications. The minimum acceptable operating temperature range for any electronic component is 0-50°C and many commercial and military atomic clock applications require operation from -40°C to 85°C. The power budget of the CSAC (and MAC) does not provide for thermoelectric cooling of the VCSEL and thus it is necessary to stabilize the VCSEL temperature by heating above the operating ambient. Given this requirement, and accounting for the fixed power dissipation from the VCSEL itself, the minimum operating temperature for the VCSEL must be >70°C. The maximum temperature must be kept as low as possible for improved reliability. The choice of cesium over rubidium for the alkali metal in the physics package permits the resonance cell to operate optimally at 70-80°C and leads naturally to integrating the VCSEL with the resonance cell. Thus, within the requirements of delivering a low-power MAC deployable in real-world ambient conditions, the folded-optics architecture described herein provides the optimum compromise between size and power and VCSEL reliability and process yield.

B. Performance

A prototype physics package, designated PS-055, has been tested, utilizing laboratory-scale electronics, including a high-resolution low-phase-noise microwave synthesizer and analog servos for the temperature control and laser- and clock-servos. The prototype physics package is not vacuum-sealed and thus exhibits higher sensitivity to changes in the laboratory ambient temperature than can be expected from a vacuum-packaged device. Typical stability data is shown below in Figure 3.

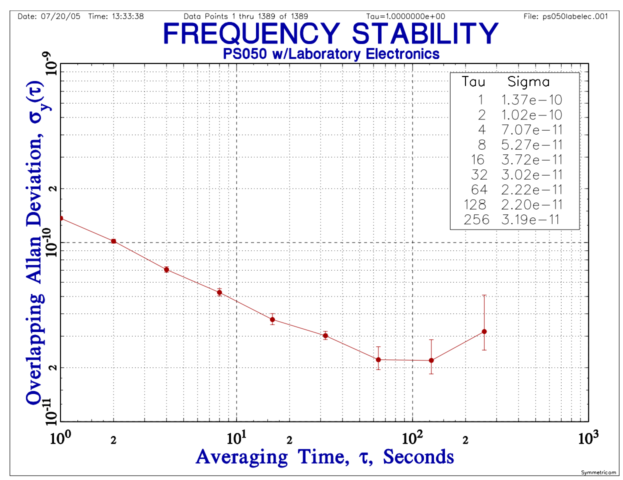


Figure 3. Stability of CSAC Physics w/Laboratory Electronics

Figure 3 represents approximately 15 minutes of CSAC physics package stability data, taken in a laboratory environment. The short-term stability displays the $\tau^{-1/2}$ behavior characteristic of atomic frequency standards. In this data set, the stability is $\sigma_y(\tau) \approx 1.5\text{x}10^{-10}\ \tau^{-1/2}$, from τ=1 to τ=100 seconds, roughly 4X better than the DARPA CSAC objective. The stability deviates from ideal $\tau^{-1/2}$ behavior at τ > 100 seconds, due principally to sensitivity to changes in our laboratory ambient temperature.

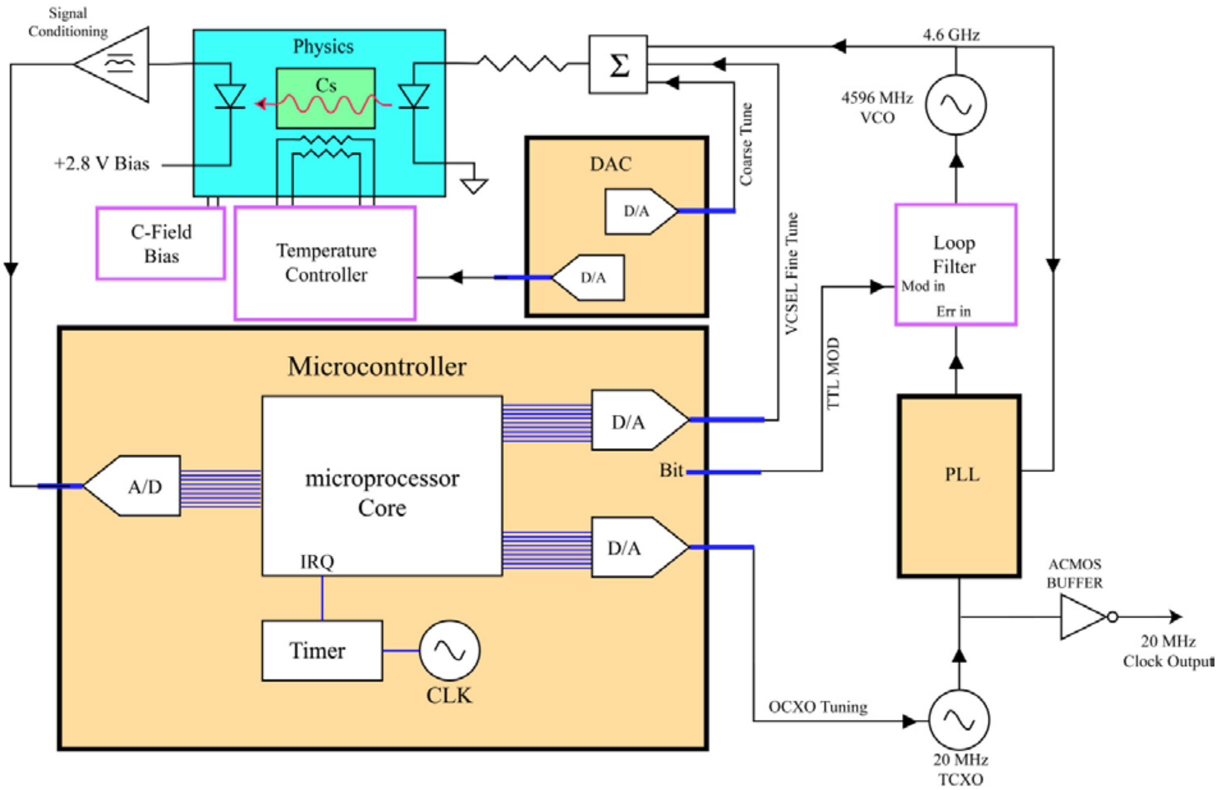


Figure 4. MAC block diagram

III. MAC Clock Architecture

In order to minimize component count, and thereby size and power consumption, many of the analog functions of traditional atomic clock architecture are implemented algorithmically in the MAC firmware. In addition to the physics package, the system consists principally of a microprocessor, analog signal conditioning, and the microwave synthesizer. The MAC operates from a single external 3.3 V supply, with internal regulators providing secondary regulation to 3.0 V and 2.8 V for the analog signal chain and the microwave synthesizer, respectively.

A block diagram of the MAC is shown above in Figure 4.

A. Signal Processing

The central controller of the MAC is a Texas Instruments MSP430 microcontroller, which includes high-speed analog-to-digital (ADC) and digital-to-analog (DAC) converters within the microprocessor package, operates from a primary supply of 3.3 VDC, and exhibits power consumption of less than 4 mW at 4 MHz processor speed. The microcontroller also provides a temperature-compensated voltage reference, which is externally filtered, buffered, and used throughout the system, as well as an on-chip UART to support external RS-232 communication. Additional DAC channels are provided by an external serially-programmed DAC. Compared to the two on-chip DACs, the external DAC channels provide higher resolution (16 bits vs. 12 bits) but are much slower to update.

B. Microwave Synthesizer

The microwave system is diagrammed on the right in Figure 4. A simple LC voltage-controlled oscillator (VCO), tunable around $\nu_{HF}/2$ = 4.6 GHz, is phase-locked to a 20 MHz temperature-compensated quartz oscillator (TCXO). The short-term stability of the local oscillator is thus determined by the stability of the TCXO, rather than by the VCO itself. The modulation of the clock interrogation frequency is injected into the loop filter of the PLL so that it appears on the VCO, without appearing on the output signal. While this approach does not allow us to precisely tune the output frequency, as would be possible with a direct-digital synthesizer, it does allow the output of a nearly standard frequency (20.0 MHz +/- 1 part in 10^8), which may be analyzed with standard frequency measurement tools, without exceeding the MAC power budget. The cost of this approach is the increase in size and power consumption due to the added components, roughly 6 mW for the TCXO, 13 mW for the dual-modulus integer PLL, and 40 mW for the VCO.

C. Laser and Clock Servos

The current input of the VCSEL includes several components: DC bias, audio frequency modulation (AF), and the 4.6 GHz RF. The DC bias is provided by the summation of coarse tuning from a slow external DAC and a fine tuning component from the fast onchip DAC. The AF modulation and servo loop correction are applied to the

VCSEL via the fast DAC. A passive network is used to sum the 4.6 GHz RF with the DC bias and AF modulation.

The optical signal from the RCPD is amplified by a single channel operational amplifier with a gain profile that has been optimized to fully exploit the resolution of the ADC at DC as well as at the laser and RF modulation frequencies. The signal is rapidly digitized by the microprocessor and the error signals are demodulated and isolated by digital filters implemented in firmware. The laser and RF error signals are integrated in firmware and applied to two DACs, which control the laser DC bias and TCXO tuning respectively.

D. Protoype Electronics

The MAC electronics were prototyped on brassboard and refined through three iterations of printed-circuit board development. A prototype PCB is shown below in Figure 5.

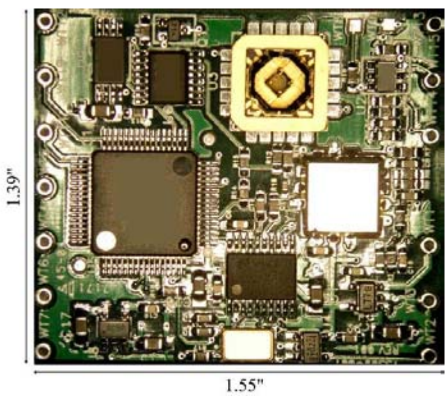


Figure 5. MAC Prototype PCB

The brassboard and first prototype PCB were tested with our laboratory-scale physics package which, with optimal electronics, demonstrates $\sigma_y(\tau)<5x10^{-11}\tau^{-1/2}$. Initial firmware development and system-level debugging was performed with this optimum signal source and an operating frequency standard was demonstrated with $\sigma_y(\tau) \approx 1x10^{-10}\ \tau^{-1/2}$.

E. Power Budget

The power budget for the MAC is summarized in TABLE I.

TABLE I. MAC POWER BUDGET

System	Component	Power
Signal Processing	MicroController	8 mW
	16-Bit DACs	7 mW
	Analog	12 mW
Physics	Heater Power	4 mW
	VCSEL Power	3 mW
	C-Field	5 mW
Microwave/RF	4.6 GHz VCO	40 mW
	PLL	17 mW
	20 MHz TCXO	7 mW
	Output Buffer	2 mW
Power Regulation & Passive Losses		3 mW
Total		108 mW

The physics package, operating in vacuum, consumes only 12 mW, including 5 mW dissipated in providing the magnetic bias field. The physics package power could be reduced to <10 mW either by increasing the number of turns of the bias coil (currently 40) or by replacing the bias coil with permanent magnets, though this would sacrifice the capability for frequency fine tuning via the bias field. The control electronics consume 27 mW, which could be reduced further by taking better advantage of microprocessor "sleep" modes, utilizing a lower-power DAC, and/or redesigning the analog signal chain to take advantage of lower power operational amplifiers. The power consumption is dominated by the microwave system, particularly the 4.6 GHz VCO, which consumes 1/3 of the total power budget of the MAC. This may be reduced significantly as recent advances in MEMs-based microwave resonators and low-power oscillators become commercially available [5].

F. Packaging

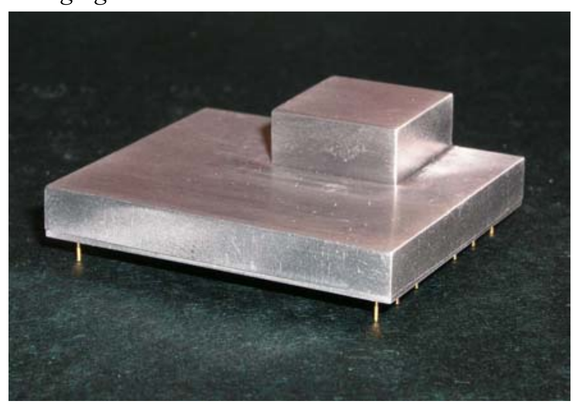


Figure 6. Photograph of the MAC prototype

Figure 6 shows a photograph of a MAC prototype. The outer packaging is machined from high-permeability mu-metal bar stock for magnetic shielding. The unusual "top-hat" shape accommodates the physics package, which is somewhat taller than other components on the populated PCB. This complex and expensive packaging concept was conceived to meet the 10 cm^3 volume goal. In a practical device, the packaging could be a simple right-parallelepiped of drawn mu-metal at approximately 100X lower cost, albeit at somewhat higher total displacement volume. The overall volume of the prototype shown above, including packaging and pins, is 9.97 cm^3.

IV. MAC CHARACTERIZATION AND TEST

Three complete MACs have been assembled, based on three PCB revisions, and tested with 5 unique physics packages.

A. MAC Test Fixture

Figure 7. Prototype MAC Installed in test fixture

Figure 7 shows a photograph of MAC-3 (top center) installed in the MAC test fixture. The test fixture provides regulated +3.3 VDC to the MAC. In addition, the test fixture provides buffer amplifiers for the AC and DC analog monitor signals, a buffer for the 20 MHz clock output, an LED lock indicator, microprocessor reset pushbutton, and level translators to interface the MAC RS-232 with a standard PC serial port. The panel display on the test fixture indicates the current (in mA) provided to the +3.3 VDC power input of the MAC. A connector on the test fixture provides access to the microprocessor's JTAG programming port, permitting in situ modification of the MAC firmware via a standard PC parallel port. In the picture, MAC-3 is operating under normal conditions, drawing (3.3 V x 31.5 mA) = 104 mW.

Vacuum sealing of the physics package was not attempted in this phase of development. As such, additional power (51 mW in MAC-3) must be provided to maintain the 80 ºC operating temperature. The test fixture includes an additional 5V regulated supply which is connected to an auxiliary heater input pin on the MAC. Note that this auxiliary heater power is not included in the display of Figure 7. Including the auxiliary heater power, the total power consumption of MAC-3 is 155 mW.

B. Atomic Spectra

Figure 8, below, shows the optical absorption resonance of MAC-3, including physics package PS-055. The DC analog signal monitor of the MAC was recorded on a digital storage oscilloscope while the VCSEL DC bias current was swept under microprocessor control.

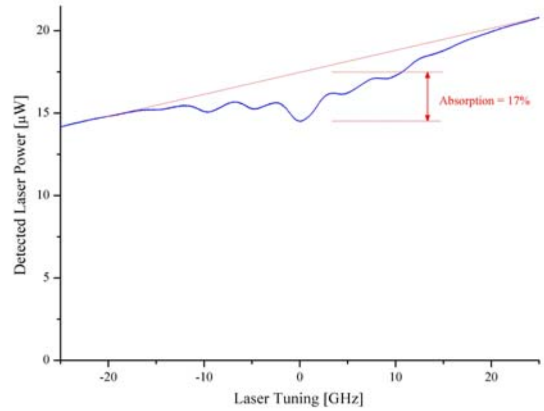


Figure 8. Laser absorption spectrum

The optical absorption spectrum exhibits the typical features of CPT spectroscopy. The linear background slope reflects the power tuning of the VCSEL. The absorption dips are separated by $\nu_{HF}/2$ = 4.6 GHz. The maximum absorption occurs when the VCSEL carrier is tuned to midway between the two principal D1 absorption lines of cesium, separated by ν_{HF} = 9.2 GHz, such that the two first-order sidebands are maximally scattered by the atomic vapor.

Note that the optical absorption, on resonance, is only 17%, which is somewhat lower than the desired 50% for optimum CPT contrast [6]. This reflects compromise between the cell geometry, VCSEL tuning, and available microwave power and differs between physics packages.

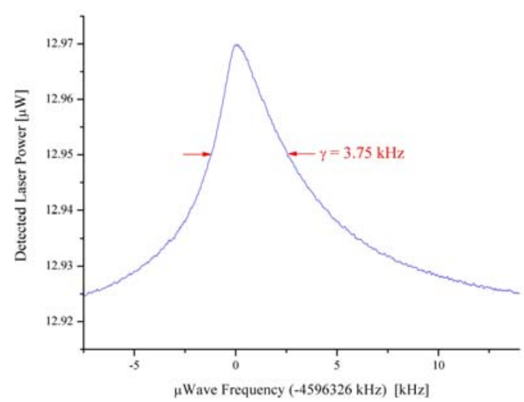


Figure 9. CPT "clock" resonance

Figure 9 shows the CPT resonance observed in MAC-3. Under microprocessor control, the laser was locked to the central absorption feature of Figure 8 and the microwave frequency was swept by ≈5 ppm by varying the DAC on the tuning input of the 20 MHz TCXO. The CPT resonance has a linewidth (FWHM) of γ = 3.75 kHz, corresponding to resonance Q = 10^6.

C. Experimental Results

MAC-3 was operated for several days in the test fixture as shown in Figure 7, during which time the servo algorithms were refined and optimized for the installed physics package PS-055. The frequency of the 20 MHz output was measured against the Symmetricom Master Clock with a Timing Solutions Model 5110 time interval analyzer. A typical frequency record is shown below in Figure 10.

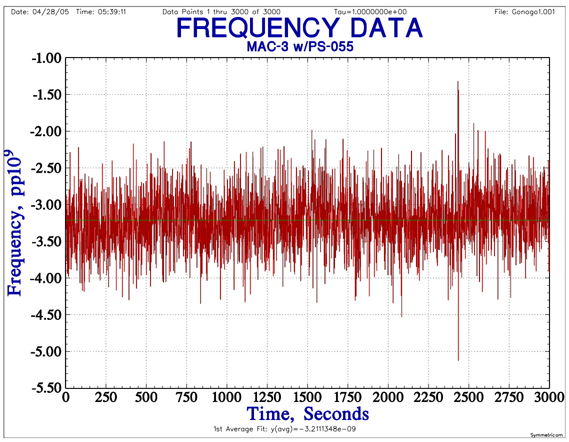


Figure 10. MAC-3 Frequency Record

The Allan deviation of this data set is shown below in Figure 11, along with the project goal of $\sigma_y(\tau) < 6x10^{-10}\ \tau^{-1/2}$. MAC-3 exhibits a 1-second intercept of $\sigma_y(\tau=1) \approx 4x10^{-10}$ and continues to improves as $\sigma_y(\tau) \propto \tau^{-1/2}$ out to τ=100 seconds.

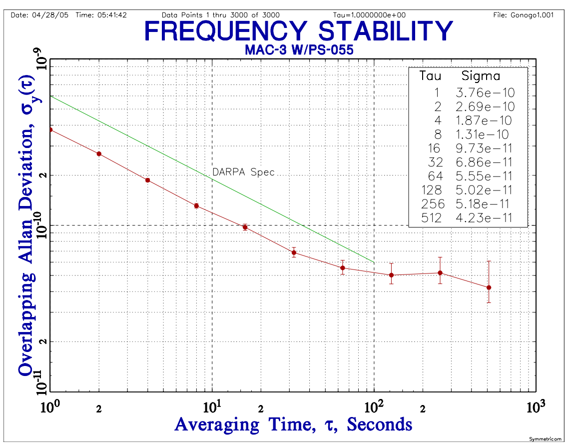


Figure 11. MAC-3 Short-term Stability

Note that the instability of MAC-3, which includes the physics package PS-055, is roughly 3X higher than that of PS-055 when tested with our laboratory electronics, as shown in Figure 3. This is principally due to the limited resolution of the ADCs and DACs compared to that of the purely analog servos in our laboratory electronics.

CONCLUSIONS

We have demonstrated a complete 10 cm^3 Miniature Atomic Clock (MAC), which demonstrates short-term stability of $\sigma_y(\tau) \approx 4x10^{-10}\ \tau^{-1/2}$ for τ=1-100 seconds while consuming only 155 mW of power. We have demonstrated that the design is capable of operating with only 105 mW of power with the incorporation of a vacuum-sealed physics package and have identified additional avenues for further improvement in power consumption.

ACKNOWLEDGMENTS

The authors wish to acknowledge the following team members for valuable technical, theoretical, and moral support: J. Deng, D. Emmons, and R.M. Garvey of Symmetricom, K.M. Geib, V.M. Montano, A.T. Ongstad, and T.W. Hargett of Sandia National Laboratories, and J. McElroy, J. LeBlanc, and G. Tepolt of the Charles Stark Draper Laboratory.

REFERENCES

[1] R. Lutwak, D. Emmons, W. Riley, and R.M. Garvey, "The Chip-Scale Atomic Clock – Coherent Population Trapping vs. Conventional Interrogation", *Proceedings of the 34th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting*, December 3-5, 2002, Reston, VA, pp. 539-550.

[2] R. Lutwak, et. al., "The Chip-Scale Atomic Clock – Recent Development Progress", *Proceedings of the 35th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting*, December 2-4, 2003, San Diego, CA, pp. 467-478

[3] R. Lutwak, et. al., "The Chip-Scale Atomic Clock – Low-Power Physics Package", *Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting*, December 7-9, 2004, Washington, DC, pp. 339-354.

[4] M. Mescher, R. Lutwak, and M. Varghese, "An Ultra-Low_power Physics Package for a Chip-Scale Atomic Clock," *Transducers '05, IEEE International Conference on Solid-State Sensors and Actuators*, June 5-9, 2005, Seoul, Korea, in press.

[5] see, for example, H. Zhang, J.J. Kim, W. Pang, H. Yu and E.S. Kim, "5GHz Low-phase-noise Oscillator Based on FBAR with Low TCF," *Transducers '05, IEEE International Conference on Solid-State Sensors and Actuators*, June 5-9, 2005, Seoul, Korea, in press.

[6] S. Knappe, J. Kitching, L. Hollberg, and R. Wynands, Appl. Phys. B **74**, 217 (2002)