

PD-IM-7548 Evaluation System User Guide Including:

PD69108 – PoE Manager, PD69100 – PoE Controller

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Reference Documents

- IEEE 802.3af-2003 Standard, DTE Power via MDI
- IEEE802.3at-2009 Standard, DTE Power via MDI
- PD69108 datasheet, catalogue number 06-0057-058
- PD69100 datasheet, catalogue number 06-0069-058
- Application note 185: Designing a D69108/PD69104 48-port Enhanced PoE Systems, catalogue number 06-0080-080
- Application note 186: Layout Design Guidelines for PD69108/PD69104 PoE Systems, catalogue number 06-0081-080
- PD63000 & PD69000/G Serial Communication Protocol User Guide, catalogue number 06-0032-056
- Software GUI user guide catalog number 06-0027-05

The above documents can be obtained via Microsemi customer support. To access other documents, go to our website at http://www.microsemi.com/, and under Tech Support\Documentation look up the relevant documents.





5.2 5.3

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1 About this Guide

1.1 Objectives

This user guide provides both a description and operation procedures for Microsemi's PD-IM-7458 evaluation system. This system is used to evaluate the performance of DB's (daughterboard) PoE applications.

1.2 Audience

This user guide is intended for qualified personnel, meaning operators and technicians who have a background in basic electronics.

1.3 Organization

This guide is divided into several sections:

| Chapter 1 | "About this Guide" which describes the objectives, audience and organization. |
|-----------|---|
| Chapter 2 | "Introduction" which gives an overview of the main functions, features, physical characteristics, and ordering information. |
| Chapter 3 | "Physical Description" which provides a physical description of the components (switches, jumpers, connectors). |
| Chapter 4 | "Electrical Characteristics" which lists the electrical characteristics of the PoE evaluation system. |
| Chapter 5 | "Installation" which describes the installation process. |



2 Introduction

Microsemi's PD-IM-7458 evaluation system consists of: PD-IM-7500 MB Motherboard (see Figure 2), PD-DB-7548 Daughterboard (see Figure 3), power supply, case, and cables. Evaluation system (Figure 1) provides designers with the needed environment to evaluate the performance and implementation of PD69108-PoE Manager and PD69100-PoE Controller mounted on PD-DB-7548 Daughterboard.

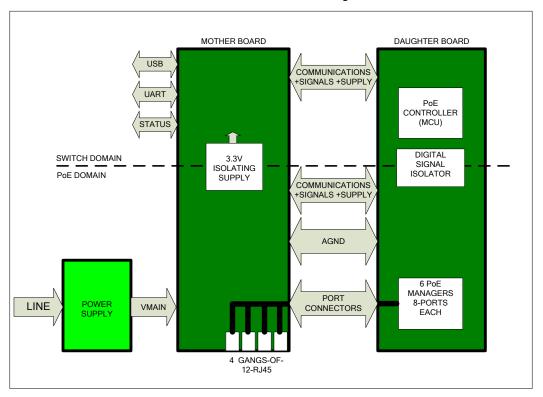


Figure 1:PD-IM-7458 Evaluation System Block Diagram

This document details the steps and connection instructions required to install and operate this board.

Evaluation Board enables PoE designers to evaluate Microsemi's PoE solution with maximum flexibility and ease in configuration.



Figure 2: PD-IM-7500 MB (Motherboard) Evaluation Board - General View



Figure 3: PD-DB-7458 (Daughterboard) Evaluation Board - General View

VMAIN power supply can output 225W. It supplies power via connector J6 (Vmain) and J7 (AGND).



Figure 4: Power Supply

Enclosure houses power supply, motherboard and the daughterboard.

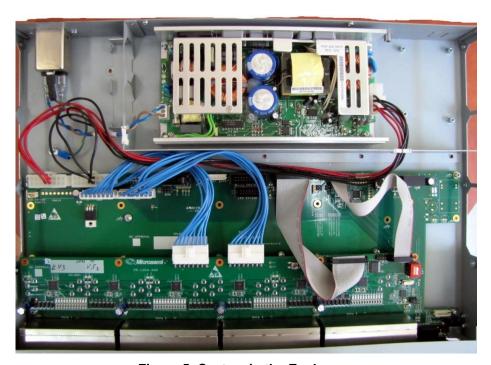


Figure 5: System in the Enclosure



2.1 Evaluation Board/System Ordering Information

The following table lists EVB ordering information.

| Ordering Number | Description | |
|-----------------|---|--|
| PD-IM-7548 | 48 ports PoE system: MB evaluation board (PD-IM-7500), DB evaluat | |
| | board (PD-DB-7548) in an enclosure with power supply. | |

2.2 Evaluation System Features

- Four gangs (each contains 12 X RJ45 connectors)
- Switch domain isolated from PoE domain
- Switch domain USB interface
- Switch domain UART (RS232) interface
- External power supplies interface
- PoE Manager Manual Reset (on daughterboard)
- PoE Controller Manual Reset (on motherboard)
- There are no pulse transformers or common mode chocks per port
- Evaluation system working temperature: 0° to +50°C
- RoHS compliant

2.3 Evaluation System Interfaces & Connections

Board has several interfaces:

- RJ45: Running from MB to PD (powered device) (MB:J29-J32)
- Ports Interface: Ports connection between MB (J22-J25) and DB (J12-J15)
- Vin Connectors: DC in (Vmain) connection to MB (J6, J7), and MB (J15, J18) to DB (J7, J8)
- Communication and Indication: Communication and indication signals transferred from MB (J2, J3) to DB (J4, J6)
- Isolated Host Control and Indication: Hosting system to MB (J4)
- Isolated USB: USB to UART communication between hosting system and MB (U7)
- Isolated RS232: RS232 communication between hosting system and MB (J33)
- Isolated UART: UART communication between hosting system and MB (J26)
- Isolated I²C: I²C communication between hosting system and MB (J14)
- External Power Supplies: 'Power good' signals coming from power supplies indicates operational/failed power supply to MB (J1)
- JTAG/SWD: PoE controller burning interface to DB (J18)

2.4 Physical Characteristics

Table 1 lists evaluation system's physical characteristics.

Table 1: Physical Characteristics

| Parameter | Value |
|-----------------------------|------------------------------|
| Mechanical dimensions: MB | 420 x 168 x 30mm (l x w x h) |
| Mechanical dimensions: DB | 420 x 50 x 20mm (l x w x h) |
| Mechanical dimensions: Case | 435 x 305 x 42mm (l x w x h) |



3 Physical Description

3.1 Switches and Jumpers

Evaluation system comprises switches and jumpers used to select the desired configuration states of the board. Default configurations are indicated as 'default'.

3.1.1 UART Communication Selection

There are three UART communication options:

- USB to UART (connecting USB cable to U7).
 For this connection a driver for CP210x should be installing. The driver can be downloaded from http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx
- RS232 to UART (connecting RS232 cable to J33)
- UART input (connecting UART cable to J26)

Using J11 and J12 jumpers, these three options can be selected.

Table 2: UART Communication Selection

| RS232 to UART | USB to UART | UART input |
|---------------------------------|---------------------------------|--------------------|
| J11 – N.C | J11 – Short from pin "1" to "2" | Short from J11 pin |
| J12 – Short from pin "1" to "2" | J12 – N.C | 2 to J12 pin 2 |

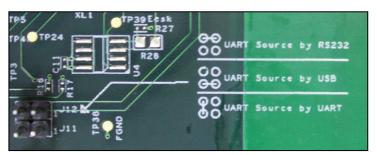


Figure 6: UART Communication Selection (J11, J12)

3.1.2 Reset Button

The dedicated Reset push button SW1 (see Figure 7) resets DB PoE controller PD69100.



Figure 7: Reset Push Button (SW1)

3.2 Connectors

The following sections provide a general and detailed description of the board connectors.

3.2.1 Connectors Table

The Evaluation system's connectors are listed in Table 3.



Table 3: Connector List

| Number | Connector | Name | Description |
|--------|--|------------------------------|---|
| 1 | MB: J29-J32 | RJ45 Connectors | 48 'RJ45' ports connecting MB to Powered Device load |
| 2 | MB: J22-J25 DB: J12-J15 | Port Connection | Port connection (Vport_pos and Vport_neg) between MB and DB implemented by using four connectors |
| 3 | MB: J6, J7, J15, J16, J18 DB: J7, J8 | Vin Connectors | DC in (Vmain) connection used to power MB and DB Evaluation systems. |
| 4 | MB: J2, J3 DB: J4, J6 | Communication and Indication | Communication (UART, I ² C and ESPI) and indication signals (reset, disable etc) running between MB and DB, using flat cables connected to J2 (PoE domain) and J3 (Host Domain) connectors |
| 5 | MB: J4 | Isolated External HOST | Control and indication signals running between an external hosting system and MB (Host Domain on the daughterboard), of limited use as most of the communication is via USB, UART, and RS232. |
| 6 | MB: U7 | Isolated USB | USB communication coming from hosting system (U7), converted to UART or I ² C communication and directed to DB (Host Domain on daughterboard) |
| 7 | MB: J33 | Isolated RS232 | RS232 signal levels coming from the hosting system (J33) and converted to UART signal levels, then directed to DB (Host Domain on daughterboard) |
| 8 | MB: J26 | Isolated UART | UART interface from hosting system and MB, then directed to DB (Host Domain on daughterboard) |
| 9 | MB: J16 | LEDs Indication | Not Used |
| 10 | MB: J8 | Daisy Chaining | Not Used |
| 11 | MB: J1 | External Power Supplies | 'Power Good' indication signals coming from power supplies, indicating operating/failed power supply status. It is also a hot-swap signal for hot swappable PoE applications. |
| 12 | MB: J5 | Tester | Not Used |
| 13 | MB: J13 | BDM | Not Used |
| 14 | DB: J5 | LED Stream | Port's status presented via LEDs indication signals running to LED board |
| 15 | DB: J18 | JTAG | PoE Controller burning interface |

3.2.2 Connectors Detailed Explanation

The numbering is in reference to the numbers given in Table 3.

1. RJ45 Connectors (see Figure 8)

There are four dedicated RJ45 connectors; each contains 12 RJ45 ports.

| Pin No. (Each RJ45) | Signal Name | Description |
|---------------------|-------------------|-------------------------------|
| 4, 5 | SPARE - Vport_Pos | The PoE's Positive spare port |
| 7, 8 | SPARE - Vport_Neg | The PoE's Negative spare port |
| 1, 2 | DATA - Vport_neg | The PoE's negative data port |
| 3, 6 | DATA - Vport_neg | The PoE's positive data port |

Manufacturer: FOXCONN

Manufacture part number: JM371B3-KD10-4F



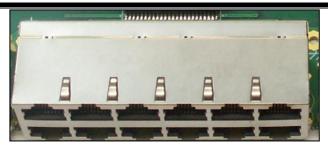


Figure 8: RJ45 Connectors

Note: 4-Pair accessory cable is provided to support 4 pairs applications that want to use the EVB as 4 pairs ports. The provided cable combines 2 selected ports into one data+spare RJ45 port as used in 4 pairs applications.

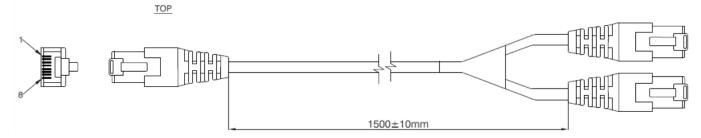


Figure 9: 4 Pairs RJ45 accessory cable diagram

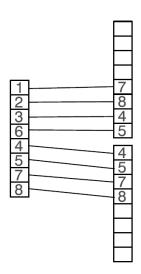


Figure 10: 4 Pairs RJ45 accessory cable connection diagram

2. Port Connection (see Figure 11)

Ports Connection (spare_NEG, spare_POS, data_NEG and data_POS) between MB's RJ45 and DB PoE circuitry is utilized by four connectors.

| Pin No. | Signal Name | Description |
|--|-------------|---------------------------|
| 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45 | spare_NEGx | PoE's negative spare port |
| 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46 | spare_POSx | PoE's positive spare port |



| 3, 7, 11, 15, 19, 23, 27,31, 35, 39, 43, 47 | data_NEGx | PoE's negative data port | |
|--|-----------|--------------------------|--|
| 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48 | data_POSx | PoE's positive data port | |

Manufacturer: CviLux

Manufacture part number: CH57482M100-PA

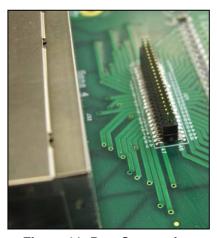


Figure 11: Port Connection

3. Vin Connectors (see Figure 12)

DC in (Vmain) connection is used for powering the MB and DB Evaluation systems. 44 V_{DC} > Vmain> 57 V_{DC} .

MB: J6

| Pin No. | Signal Name | Description |
|---------|---------------|--|
| 1-16 | Vmain (Vin +) | Main positive voltage (referenced to AGND) |

MB: J7

| Pin No. | Signal Name | Description |
|---------|--------------|---------------|
| 1-16 | AGND (Vin -) | Analog ground |

Manufacturer: CviLux

Manufacture part number: CP01-316130

MB: J17

| Pin No. | Signal Name | Description |
|---------|---------------|--|
| 1-8 | Vmain (Vin +) | Main positive voltage (referenced to AGND) |

MB: J15. DB: J7

| Pin No. | Signal Name | Description |
|---------|---------------|--|
| 1 | Vmain (Vin +) | Main positive voltage (referenced to AGND) |
| 2-8 | AGND (Vin -) | Analog ground |

MB: J18. DB: J8

| Pin No. Signal Name | | Description | |
|---------------------|---------------|--|--|
| 1 | Vmain (Vin +) | Main positive voltage (referenced to AGND) | |
| 2-8 | AGND (Vin -) | Analog ground | |

Manufacturer: CviLux

Manufacture part number: CI5208P1VOO



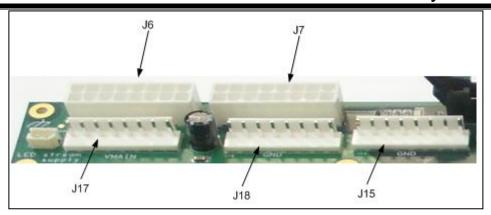


Figure 12: Vin Connectors

4. Communication and Indication (see Figure 13)

Communication (UART, I²C and ESPI) and indication signals (reset, disable, etc.) run between MB and DB using flat cables connected to J2 (PoE domain) and J3 (Host Domain) connectors.

MB: J3, DB: J6

| Pin No. | Signal Name | Description | | |
|--------------|----------------------------|---|--|--|
| 1 | xReset_IN_isolated | Reset signal sent from hosting system | | |
| 2 | xDisable_ports_isolated | Disable signal sent from hosting system | | |
| 3 | xSystem_ok_isolated | System_ok signal sent from hosting system | | |
| 4 | RTS | Reserved | | |
| 5 | xInt_out_isolated | Int_out signal sent from hosting system | | |
| 6 | reserved | Reserved | | |
| 7 | 3_3V_iso | 3.3 VDC sent from hosting system (isolated from PoE domain), referenced to 'GND_Floating' | | |
| 8, 13, 16 | GND_Floating | Hosting system ground (isolated from PoE domain) | | |
| 9 | UART_Tx_isolated | Tx signal (transmit), direction sent from PoE controller (3.3V tolerate) | | |
| 10 | UART_Rx_isolated | Rx signal (receive), to PoE controller (3.3V tolerate) | | |
| 11 | SDA_auto_mode_isolated | I ² C SDA: data I ² C signal between hosting system and PD69108 | | |
| 12 | SCL_auto_mode_isolated | I ² C SCL: clock I ² C signal between hosting system and PD69108 | | |
| 14 | SDA_enhanced_mode_isolated | I ² C SDA: Data I ² C signal between hosting system and PD69100 | | |
| 15 | SCL_enhanced_mode_isolated | I ² C SCL: Clock I ² C signal between hosting system and PD69100 | | |

Manufacturer: CviLux

Manufacture part number: CH74162V100

MB: J2, DB: J4

| Pin No. | Signal Name | Description | | |
|---------|----------------|---|--|--|
| 1 | PG0 | Power good signal, power supply status indication | | |
| 2 | PG1 | Power good signal, power supply status indication | | |
| 3 | PG2 | Power good signal, power supply status indication | | |
| 4 | PG3 | Power good signal, power supply status indication | | |
| 5 | xReset_IN | Reset signal to PoE application (used for cascading purposes) | | |
| 6 | xDisable_ports | Disable_ports signal to PoE application (used for cascading purposes) | | |
| 7 | xPoE_RESET | Reset signal to PD69108 ICs (used for cascading purposes) | | |
| 8 | xHSWP | Hot Swap control signal, used when PoE application is hot swappable | | |
| 9 | BKGD | PoE controller burning signal | | |



| Pin No. | Signal Name | Description |
|---------|-------------------|---|
| 10, 11, | GND_D | Digital ground at PoE domain |
| 17, 18, | | |
| 21, 23, | | |
| 24, 29 | | |
| 12, 13 | Reserved | Reserved |
| 12 | SDA_in_auto_mode | I ² C SDA_in – Data I ² C signal (used for cascading purposes) |
| 14 | SDA_out_auto_mode | I ² C SDA_out – Data I ² C signal (used for cascading purposes) |
| 15 | SCL_auto_mode | I ² C SCL – Clock I ² C signal (used for cascading purposes) |
| 19 | LED_SCK | Clock LED signal – Running to LED indication board |
| 20 | LED_DATA | Data LED signal – Running to LED indication board |
| 22 | LED_Latch | Latch LED signal – Running to LED indication board |
| 25 | ESPI_CS | ESPI 'chip select' signal (used for cascading purposes) |
| 26 | ESPI_MOSI | ESPI 'master out slave in' signal (used for cascading purposes) |
| 27 | ESPI_MISO | ESPI 'master in' slave out' signal (used for cascading purposes) |
| 28 | ESPI_SCK | ESPI clock (used for cascading purposes) |
| 30 | VAUX3P3 | 3.3 VDC = VAUX3P3 and 3V3_AUX, application's reference voltage |
| | | (isolated from hosting system domain), referenced to 'GND_D' |

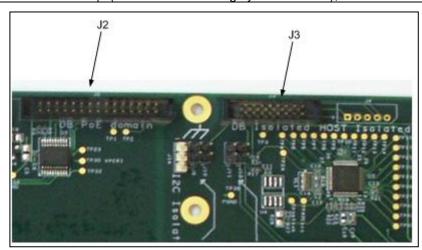


Figure 13: Communication and Indication Connectors

Manufacturer: CviLux

Manufacture part number: CH74302V100

5. Isolated External Host (see Figure 14)

This host transmits control and indication signals beween hosting system and MB. There is limited use for this connector as most communication is via USB, RS232 or UART.

MB: J4

| Pin No. | Signal Name | Description |
|---------|-------------------------|--|
| 1 | xReset_IN_isolated | Reset signal from hosting system |
| 2 | xDisable_ports_isolated | Disable signal from hosting system |
| 3 | xInt_out_isolated | Int_out signal from hosting system |
| 4 | xSystem_ok_isolated | System_ok signal from hosting system |
| 5 | GND_Floating | Hosting system ground (isolated from PoE domain) |

Manufacturer: CviLux

Manufacture part number: CI25-05P1V00





Figure 14: Isolated External Host

6. Isolated USB Interface (see Figure 15)

This interface supplies USB communication coming from hosting system (U7), converted to UART or I²C communication and directed to DB (Isolation circuitry on daughterboard).

MB: U7

| Pin No. | Signal Name | Description | |
|---------|-------------|-----------------------------|--|
| 1 | Vbus | Voltage supply from USB bus | |
| 2 | D- | Dedicated USB signal | |
| 3 | D+ | Dedicated USB signal | |
| 4 | GND F | Floating ground | |

Manufacturer: Samtec

Manufacture part number: USB-B-S-S-B-TH



Figure 15: Isolated USB Interface

7. Isolated RS232 (see Figure 16)

RS232 signals level comes from hosting system and has been converted to UART signals levels, then directed to DB (Isolation circuitry on daughterboard)

MB: J33

| Pin No. | Signal Name | Description | |
|---------------------|-------------|--|--|
| 1, 4, 6, 7, 8, 9 | N.C | Not connected | |
| 2 | Rx_RS232 | Rx RS232 level signal (receive), between the hosting system and the MB | |



| 3 | Tx_RS232 | Tx RS232 level signal (transmit), between the hosting system and the MB |
|---|----------|---|
| 5 | GND_F | Floating ground |

- Manufacturer: Coxoc
- Manufacture part number: 205A-09MGPBBA3

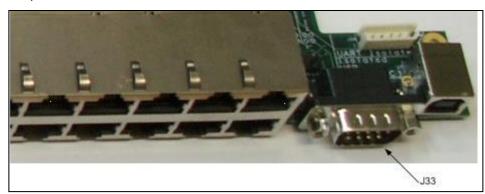


Figure 16: Isolated RS232

8. Isolated UART Interface (see Figure 17)

UART interface from hosting system and MB, then directed to DB (Isolation circuitry on daughterboard).

MB: J26

| Pin No. | Signal Name | Description | | |
|---------|------------------|---|--|--|
| 1 | 3_3V_iso | 3.3 VDC coming from hosting system (isolated from PoE domain), referenced | | |
| | | to 'GND_Floating' | | |
| 2 | UART_Rx_isolated | Rx UART level signal (receive), between hosting system and MB (3.3 VDC) | | |
| 3 | UART_Tx_isolated | Tx UART level signal (transmit), between hosting system and MB (3.3 VDC) | | |
| 4 | GND_F | Floating ground | | |
| 5 | N.C | Not connected | | |

- Manufacturer: CviLux
- Manufacture part number: CI25-05P1V00



Figure 17: Isolated UART Interface

9. LEDs Indication (see Figure 18)

This interface controls port status indication LEDs. Using four dedicated signals, LEDs indicate ports status (on, off, and so on)



DB: J5

| Pin No. | Signal Name | Description | | | |
|---------|---------------------|---|--|--|--|
| 1 | MOSI_B | Data LED signal running to LED indication board ('b' – buffered signal) | | | |
| 2 | +5V | | | | |
| 3 | SCK_B | Clock LED signal running to LED indication board ('b' – buffered signal) | | | |
| 4 | FGND | Floating ground | | | |
| 5 | LED_latch_b | Latch LED signal running to LED indication board ('b' – buffered signal) | | | |
| 6 | Led_output_enable_b | Enable LED signal running to LED indication board ('b' – buffered signal) | | | |

Manufacturer: CviLux

Manufacture part number: CH87-142V200



Figure 18: LEDs Indication

10. Daisy Chain (not used)

MB: J8

11. External Power Supplies Indication (see Figure 19)

This interface supplies 'Power Good' indication signals coming from power supplies, indicating operating/failed power supply's status and hot-swap signal for a hot swappable PoE application.

MB: J1

| Pin No. | Signal Name | Description | | |
|---------|-------------|--|--|--|
| 1 | PG0 | 'Power good' signal – power supply status indication | | |
| 2 | PG1 | 'Power good' signal – power supply status indication | | |
| 3 | PG2 | 'Power good' signal – power supply status indication | | |
| 4 | PG3 | 'Power good' signal – power supply status indication | | |
| 5 | GND_D | Digital ground at PoE domain | | |
| 6 | xHSWP | Hot Swap control signal, indicating PoE application is hot swappable | | |

Manufacturer: CviLux

Manufacture part number: CI25-06P1V00



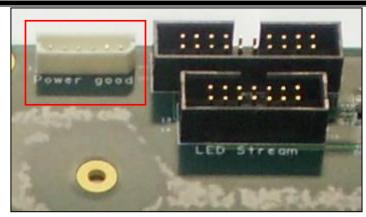


Figure 19: External Power Supplies



Electrical Characteristics

The evaluation system's electrical characteristics are described below:

| Parameter | Symbol | Min. | Max. | Units |
|--|--------|------|------|-------|
| Main DC supply Vmain | | 44 | 57 | V |
| Port Isolation to chassis | | - | 1.5 | kVrms |
| All communication's Isolation to chassis | | - | 1.5 | kVrms |

MB's electrical characteristics depend on daughterboard to which it is connected.



5 Installation

This chapter describes the steps required for installing and operating PD-IM-7548 Evaluation system. Some necessary precautions:

- Verify board's power supply is turned on before peripheral devices are turned on.
- Connect all required peripherals prior to powering board.
- Do not hot swap any components!
- Verify board is well configured prior to turning on power supply.

5.1 Mechanical Assembly

| Step | Action | Comments | | |
|------|----------------------------|--|--|--|
| 1 | Assemble Line Filter | | | |
| 2 | Assemble Power Supply | Mount power supply with 4 screws to enclosure Mount all required cables | | |
| 3 | Assemble Motherboard | Assemble 5 spacers for DB Assemble MB with 13 screws to enclosure Recommended USB communication: install jumper on J11 Mount all required cables | | |
| 4 | Assemble Daughterboard | Mount DB with 5 spacers to accommodate LED Display board Mount all required cables | | |
| 5 | Assemble LED Display Board | Mount LED Display board with 5 screws Mount all required cables Mount light pipes as required | | |

5.2 Electrical Assembly

| # | Cable | Source | Destination | Comments |
|---|------------------------------|------------------|------------------|--------------|
| 1 | Internal Line Power | Line Filter | Power Supply/CN1 | |
| 2 | 48V | Power Supply/CN2 | MB/J6/J7 | |
| 3 | Analog Ground 1 | MB/J18 | DB/J8 | |
| 4 | Analog Ground 2 | MB/J15 | DB/J7 | |
| 5 | PoE Domain Signals | MB/J2 | DB/J4 | |
| 6 | Host (Switch) Domain Signals | MB/J3 | DB/J6 | |
| 7 | Display Data | DB/J5 | LED Display/J4 | Custom Cable |

5.3 Initial Configuration

It is highly important to verify that Evaluation board is properly configured prior to starting any operation. Refer to *Software GUI user guide, catalogue number 06-0027-056* for detailed information related to software and GUI used for Enhance Mode operation.



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Revision History

| Revision Level / | Para. Affected | Description |
|--------------------|----------------|------------------------------|
| Date | | |
| 0.1 / 14 July 2011 | | Initial revision |
| 0.2 / 6 Apr 2014 | | Add 4 pair cable description |

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