Total Ionizing Dose Test Report

No. 13T-RTSX72SU-CQ256-D1WWA1

September 26, 2013

Table of Contents

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 40 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 100 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO_2)
5. Propagation Delay	Passed 100 krad (SiO_2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D1WWA1
Quantity Tested	6
Serial Number	100 krad(SiO_2): 7422, 7437 60 krad(SiO_2): 7442, 7459 40 krad(SiO_2): 7508, 7579
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

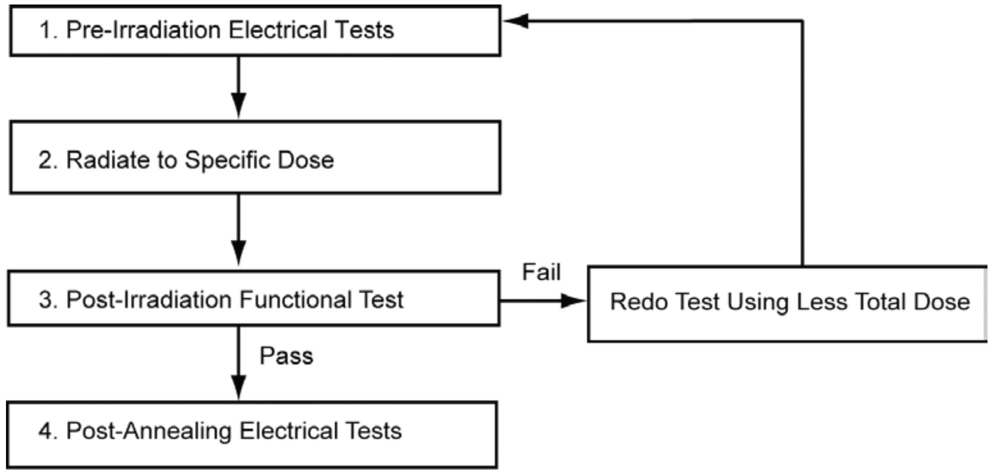


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VTIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation, post-irradiation—right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
7422	100 krad	1.33	266	172	1.01	218	151
7437	100 krad	2.21	346	243	1.04	243	166
7442	60 krad	1.10	78	21	0.75	22	38
7459	60 krad	1.06	23	19	1.04	24	34
7508	40 krad	1.07	4	4	1.01	4	4
7579	40 krad	1.06	4	4	1.05	4	4

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in this test, is defined as the highest ICCA/ICCI in the RTSXSU spec sheet of 25 mA.

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT.

There are unexpected ICCI increases during irradiation, as shown in Figures 3 through 7, where the ICCI would drop back at some points of time. The suspect is an intermittent continuity problem of the socket on the test board. The post-anneal ICCI measurements are more stable.

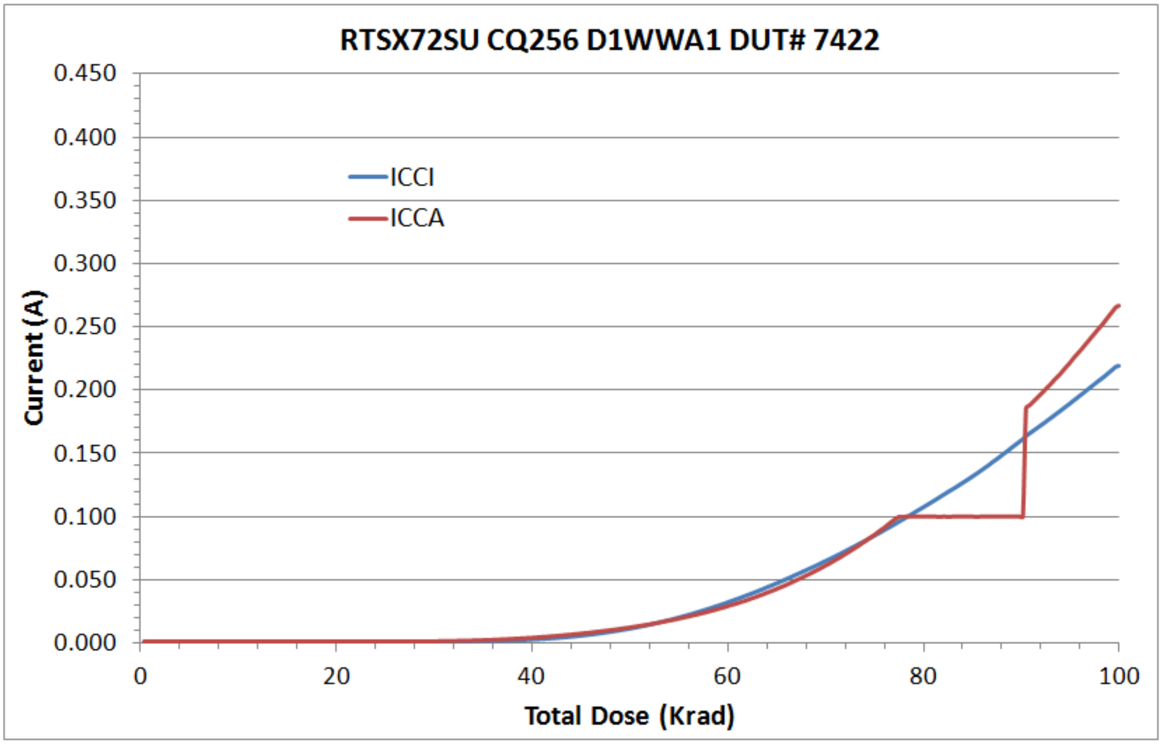


Figure 2 DUT 7422 Influx ICCA and ICCI

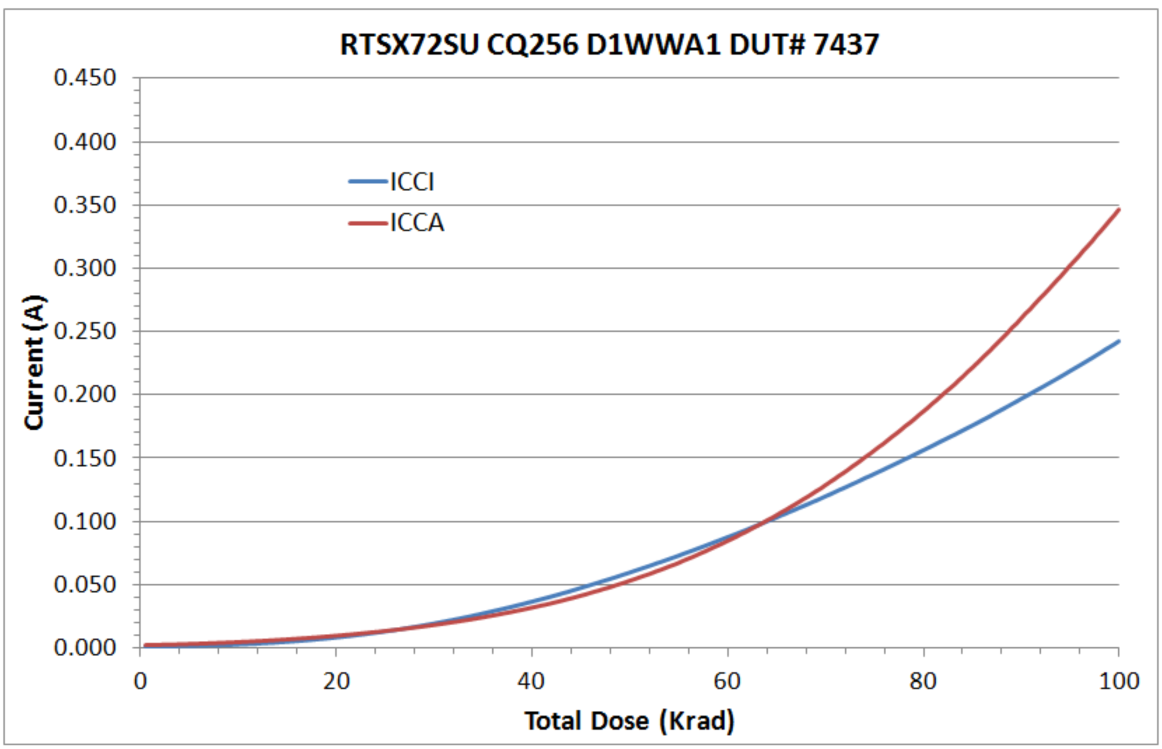


Figure 3 DUT 7437 Influx ICCA and ICCI

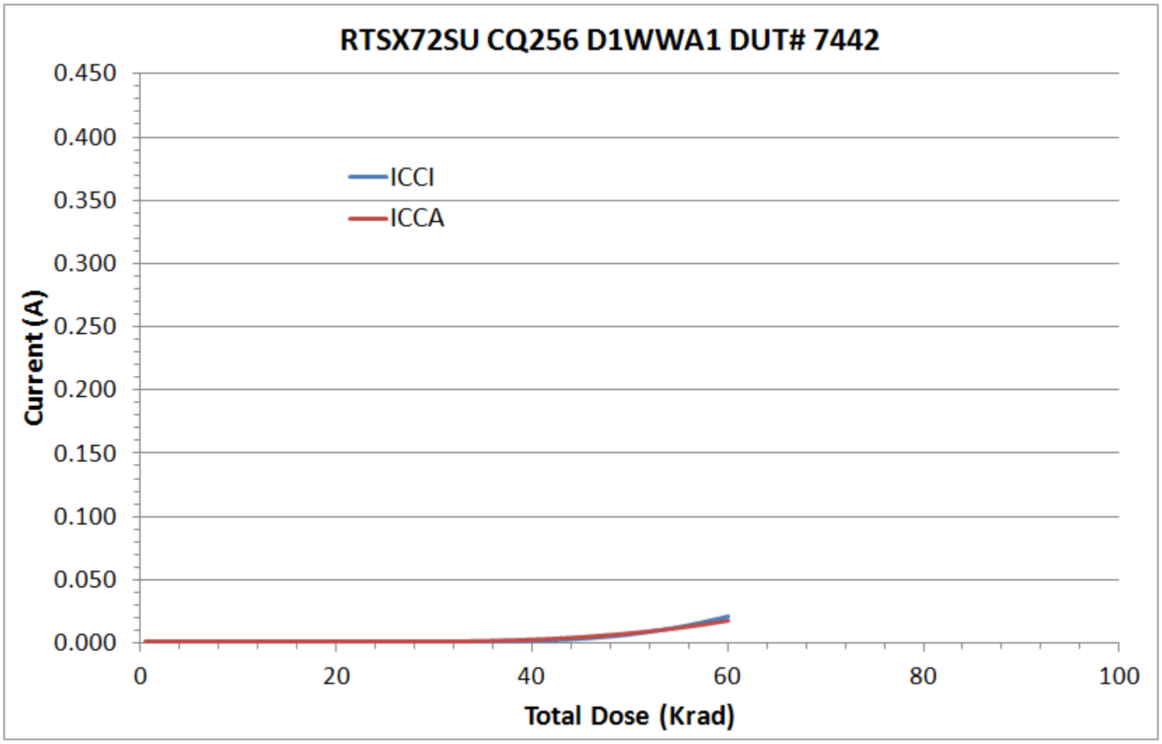


Figure 4 DUT 7442 Influx ICCA and ICCI

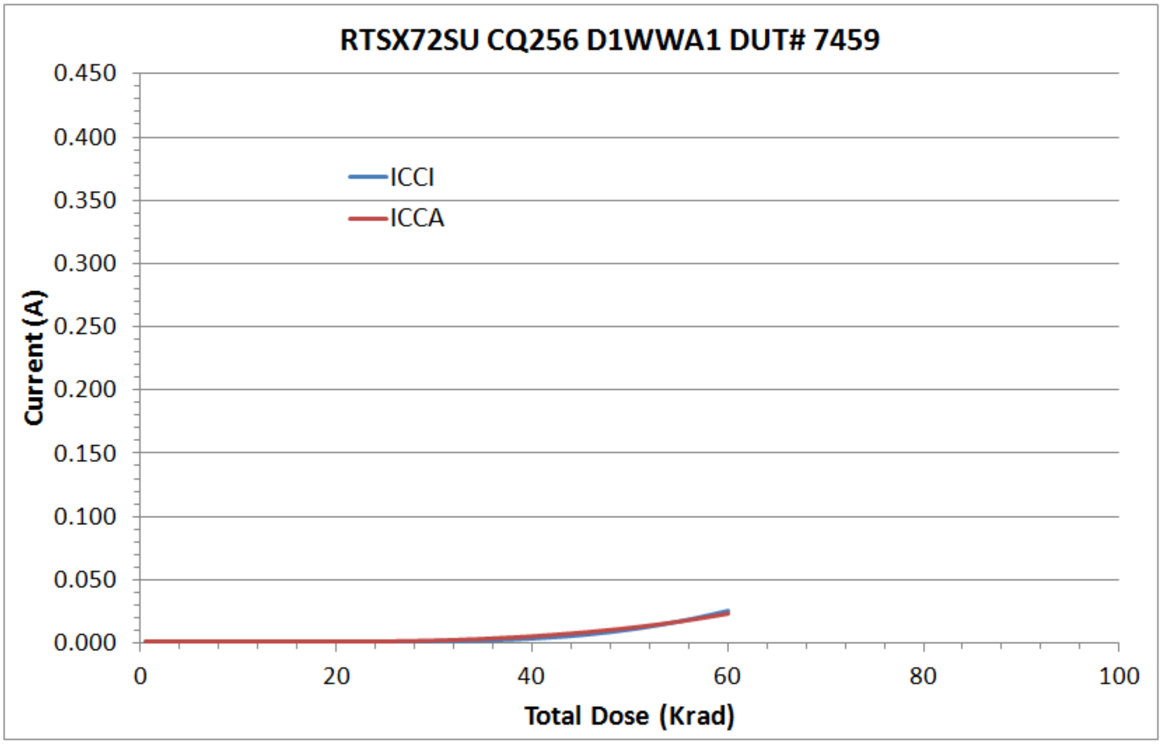


Figure 5 DUT 7459 Influx ICCA and ICCI

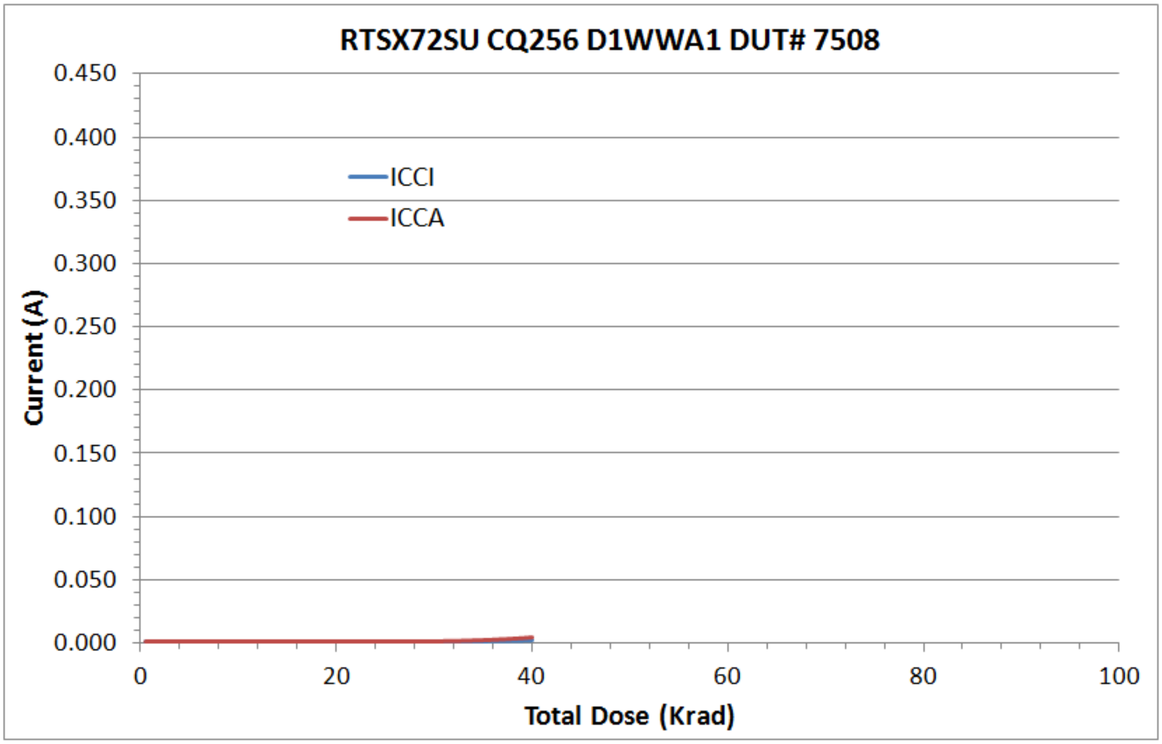


Figure 6 DUT 7508 Influx ICCA and ICCI

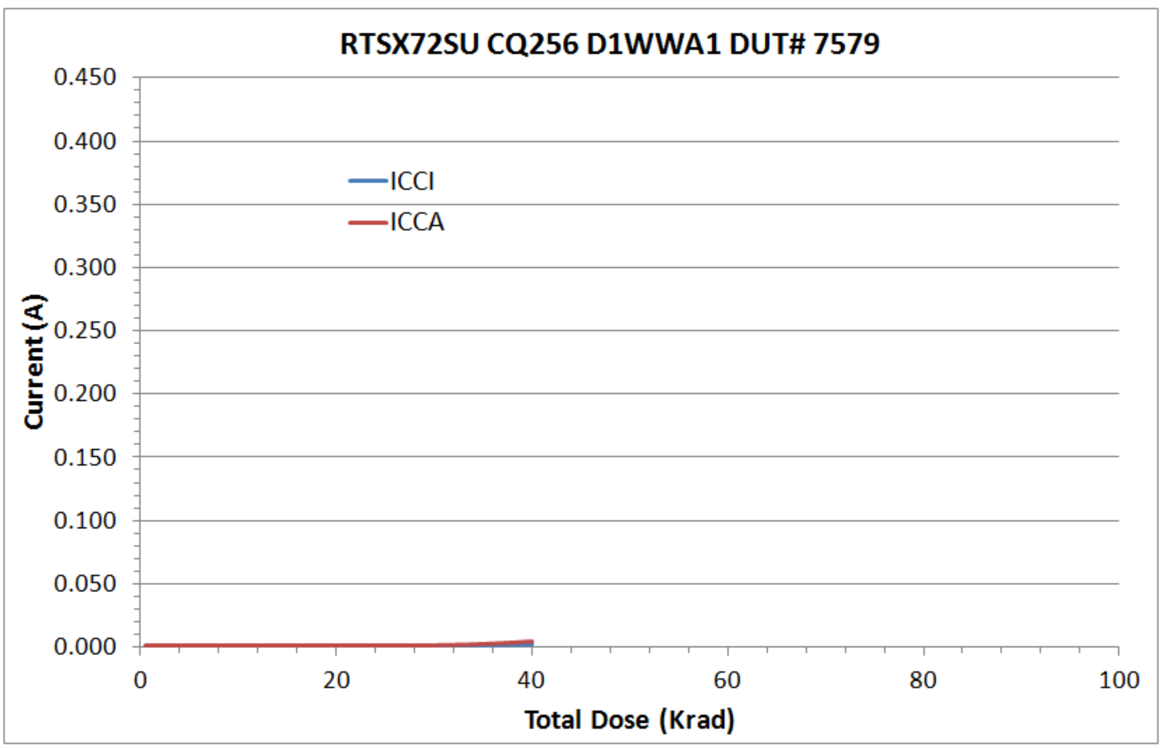


Figure 7 DUT 7579 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds. All data is within the specification limits. The post-annealing shift in every case is very small.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	7422 (100 krad)				7437 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1090	1165	1545	1490	1095	1215	1550	1475
DAH/QA0H	1440	1460	1435	1445	1445	1465	1445	1420
ENCNTRH/YO0	1470	1460	2030	1425	1460	1455	1995	1435
IDII0/IDIO0	1450	1350	1420	1435	1460	1460	1430	1400
IDII1/IDIO1	1515	1515	1450	1455	1510	1500	1450	1450
IDII2/IDIO2	1335	1495	1415	1420	1495	1500	1450	1430
IDII3/IDIO3	1520	1390	1430	1425	1515	1395	1430	1420
IDII4/IDIO4	1480	1440	1455	1415	1465	1440	1455	1415
IDII5/IDIO5	1300	1310	1425	1565	1415	1325	1520	1435
IDII6/IDIO6	1390	1425	1440	1400	1390	1425	1455	1405
IDII7/IDIO7	1490	1480	1420	1425	1460	1495	1420	1420

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	7442 (60 krad)				7459 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1110	1235	1550	1500	1125	1235	1495	1545
DAH/QA0H	1460	1500	1455	1455	1455	1495	1420	1500
ENCNTRH/YO0	1475	1450	2005	1430	1480	1490	2015	1925
IDII0/IDIO0	1370	1420	1445	1430	1390	1495	1440	1470
IDII1/IDIO1	1465	1460	1455	1440	1435	1515	1455	1450
IDII2/IDIO2	1505	1500	1425	1420	1505	1455	1450	1450
IDII3/IDIO3	1530	1535	1440	1420	1520	1500	1440	1425
IDII4/IDIO4	1470	1460	1440	1430	1475	1480	1460	1465
IDII5/IDIO5	1395	1345	1435	1565	1415	1375	1525	1575
IDII6/IDIO6	1465	1460	1425	1405	1415	1470	1425	1445
IDII7/IDIO7	1500	1525	1430	1425	1500	1480	1430	1425

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	7508 (40 krad)				7579 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1105	1195	1555	1550	1160	1225	1520	1550
DAH/QA0H	1445	1475	1440	1485	1450	1510	1450	1505
ENCNTRH/YO0	1475	1490	2025	1960	1490	1470	1960	1915
IDII0/IDIO0	1370	1490	1440	1445	1375	1480	1440	1455
IDII1/IDIO1	1515	1480	1450	1465	1505	1460	1460	1460
IDII2/IDIO2	1415	1505	1445	1425	1370	1495	1430	1430
IDII3/IDIO3	1525	1530	1435	1440	1550	1530	1440	1435
IDII4/IDIO4	1465	1455	1455	1405	1475	1395	1460	1460
IDII5/IDIO5	1390	1335	1425	1455	1385	1375	1455	1575
IDII6/IDIO6	1410	1460	1450	1455	1410	1460	1430	1450
IDII7/IDIO7	1475	1515	1440	1525	1510	1510	1525	1435

E. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	7422 (100 krad)		7437 (100 krad)		7442 (60 krad)		7459 (60 krad)		7508 (40 krad)		7579 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	10	10	10	10	10	10	10	10	10	10	10	10
12 mA	115	115	114	113	117	116	117	115	117	115	115	115
20 mA	193	192	189	189	195	193	194	192	193	193	192	192
50 mA	484	483	477	475	490	487	489	483	488	486	485	483
100 mA	992	989	977	975	1001	998	1001	990	999	995	993	989

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	7422 (100 krad)		7437 (100 krad)		7442 (60 krad)		7459 (60 krad)		7508 (40 krad)		7579 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4979	4971	4979	4965	4980	4975	4980	4977	4979	4977	4979	4977
8 mA	4850	4839	4850	4833	4850	4845	4851	4848	4850	4847	4851	4848
20 mA	4623	4609	4623	4601	4623	4616	4624	4620	4622	4618	4624	4620
50 mA	4011	3985	4008	3971	4013	4001	4014	4007	4010	4002	4013	4007
100 mA	2647	2560	2624	2493	2669	2631	2666	2637	2646	2623	2658	2638

F. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion. The user can take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (μs)	Post-Anneal (μs)	Degradation (%)
7422	100 krad	1.37	1.48	8.42%
7437	100 krad	1.38	1.50	9.09%
7442	60 krad	1.35	1.37	1.48%
7459	60 krad	1.35	1.36	0.74%
7508	40 krad	1.36	1.36	0.00%
7579	40 krad	1.38	1.38	0.00%

G. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

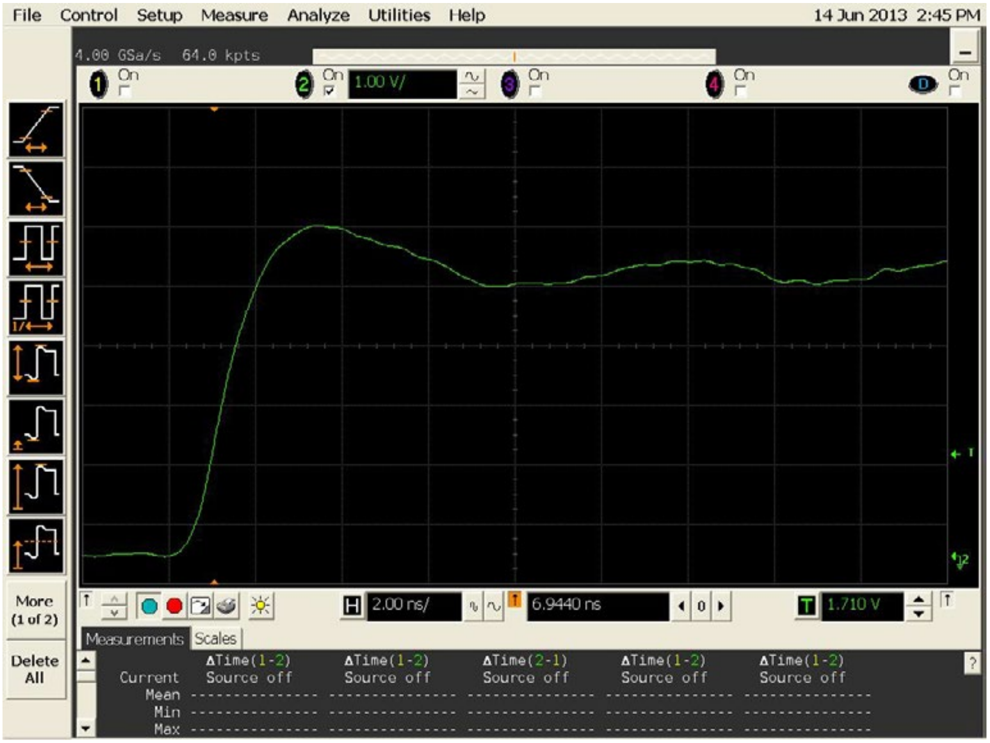


Figure 9a DUT 7422 Pre-Irradiation Rising Edge

Figure 9b DUT 7422 Post-Annealing Rising Edge

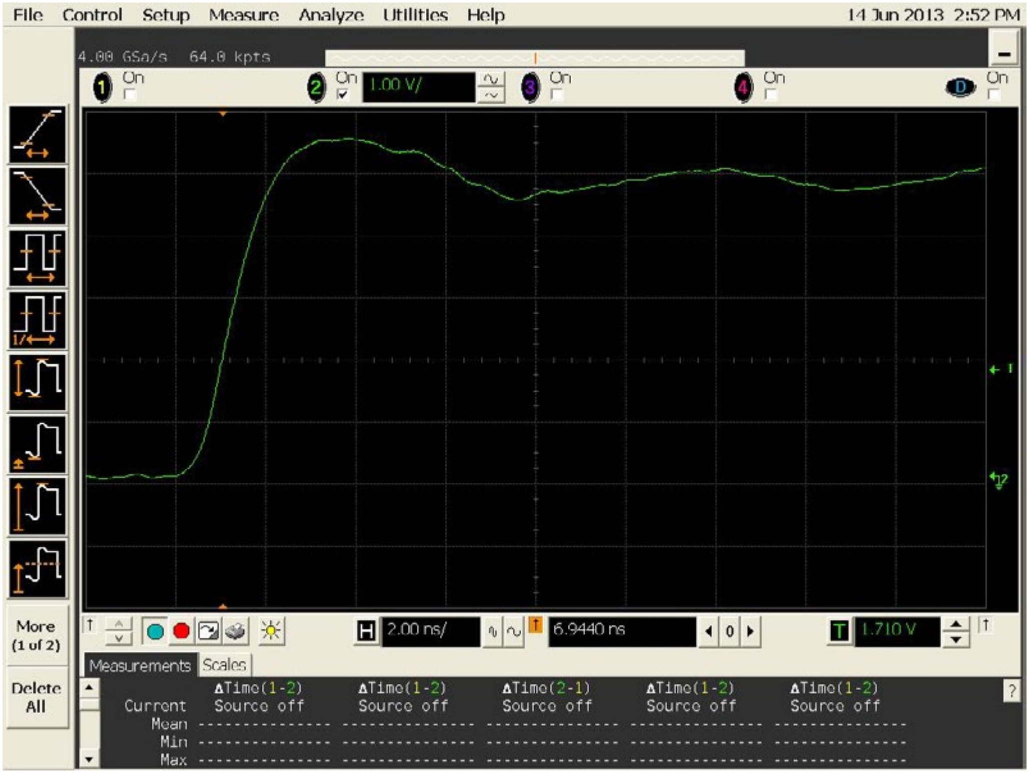


Figure 10a DUT 7437 Pre-Irradiation Rising Edge

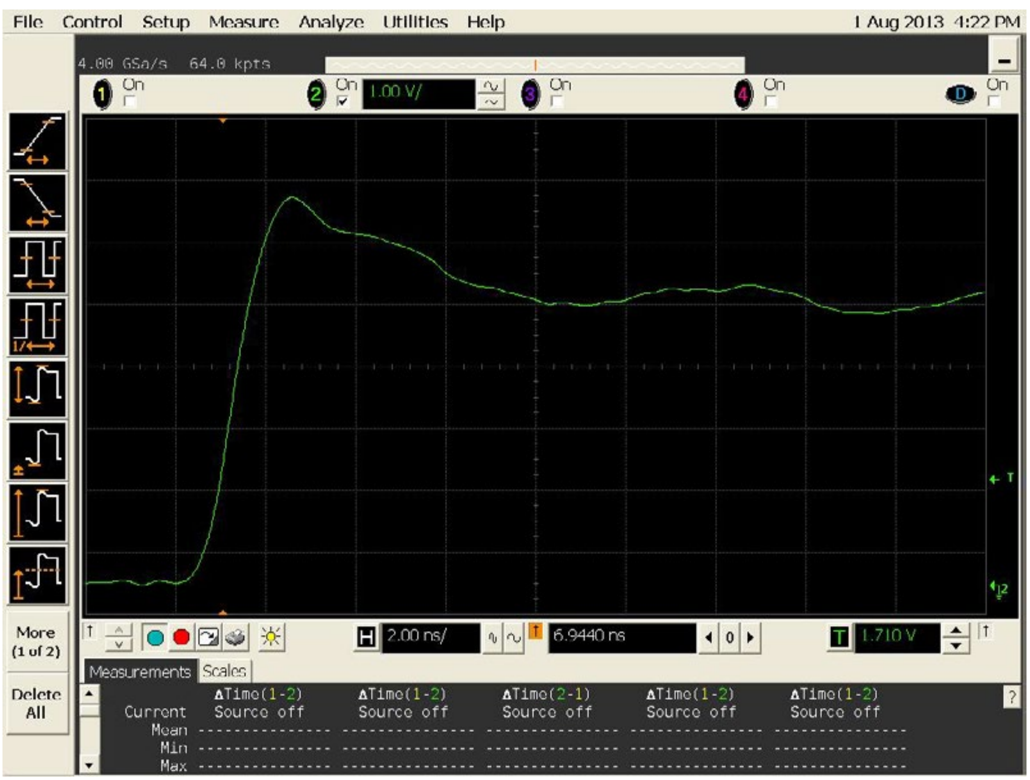


Figure 10b DUT 7437 Post-Annealing Rising Edge

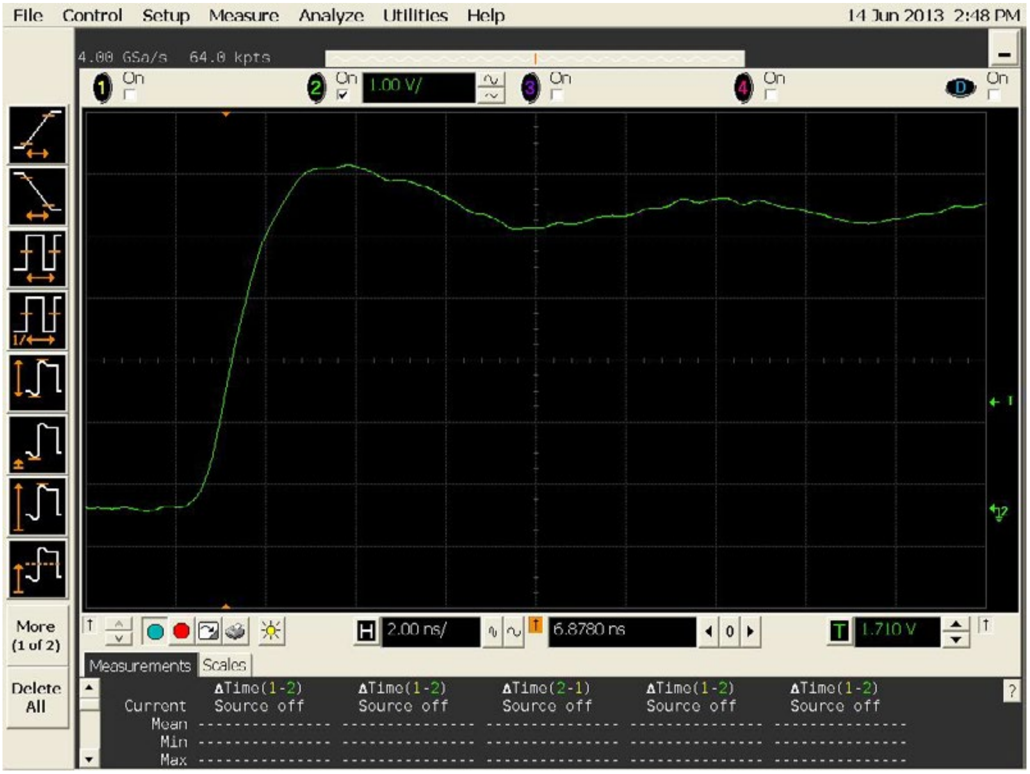


Figure 11a DUT 7442 Pre-Radiation Rising Edge

Figure 11b DUT 7442 Post-Annealing Rising edge

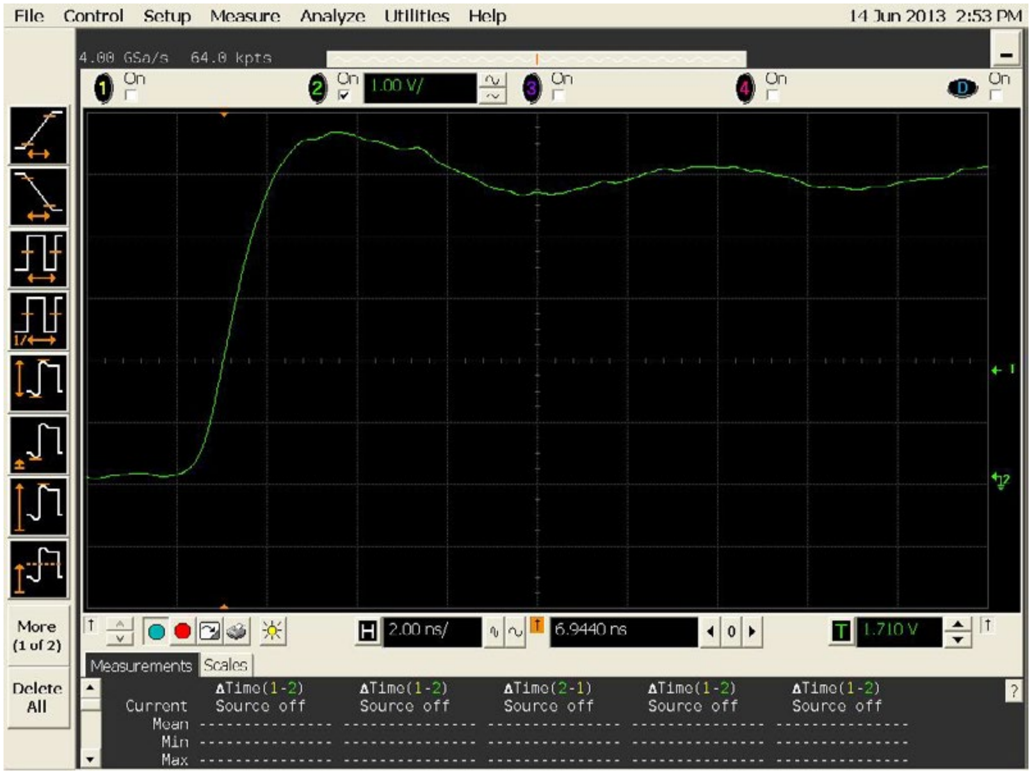


Figure 12a DUT 7459 Pre-Irradiation Rising Edge

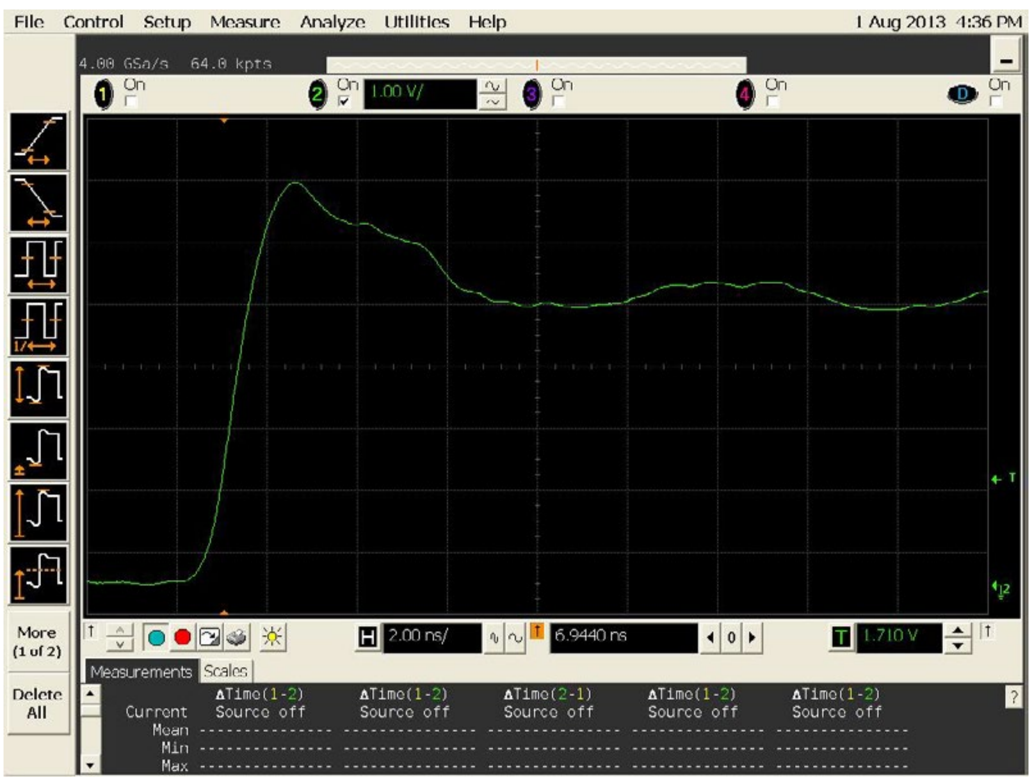


Figure 12b DUT 7459 Post-Annealing Rising Edge

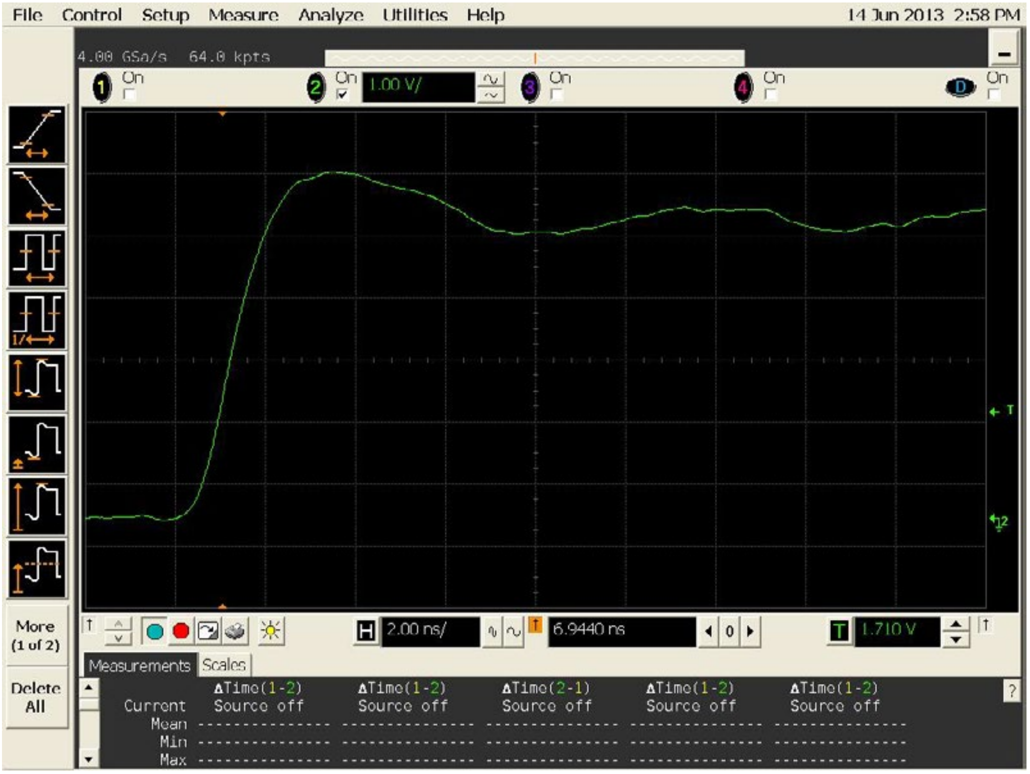


Figure 13a DUT 7508 Pre-Irradiation Rising Edge

Figure 13b DUT 7508 Post-Annealing Rising Edge

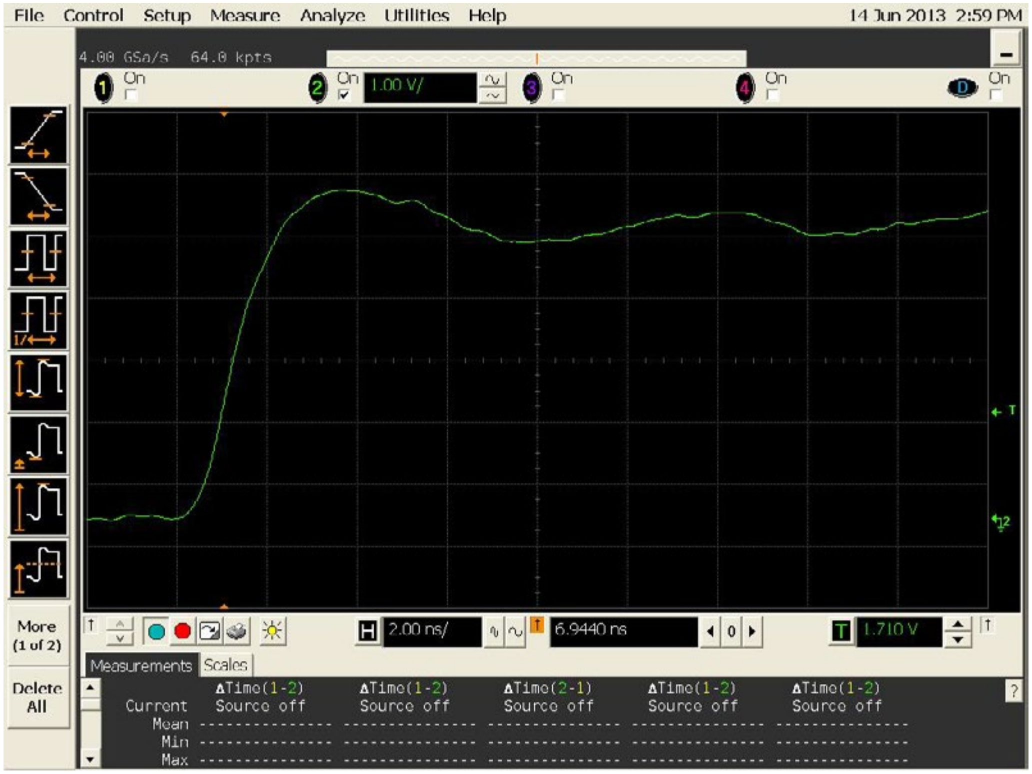


Figure 14a DUT 7579 Pre-Irradiation Rising Edge

Figure 14b DUT 7579 Post-Annealing Rising Edge

Figure 15a DUT 7422 Pre-Radiation Falling Edge

Figure 15b DUT 7422 Post-Annealing Falling Edge

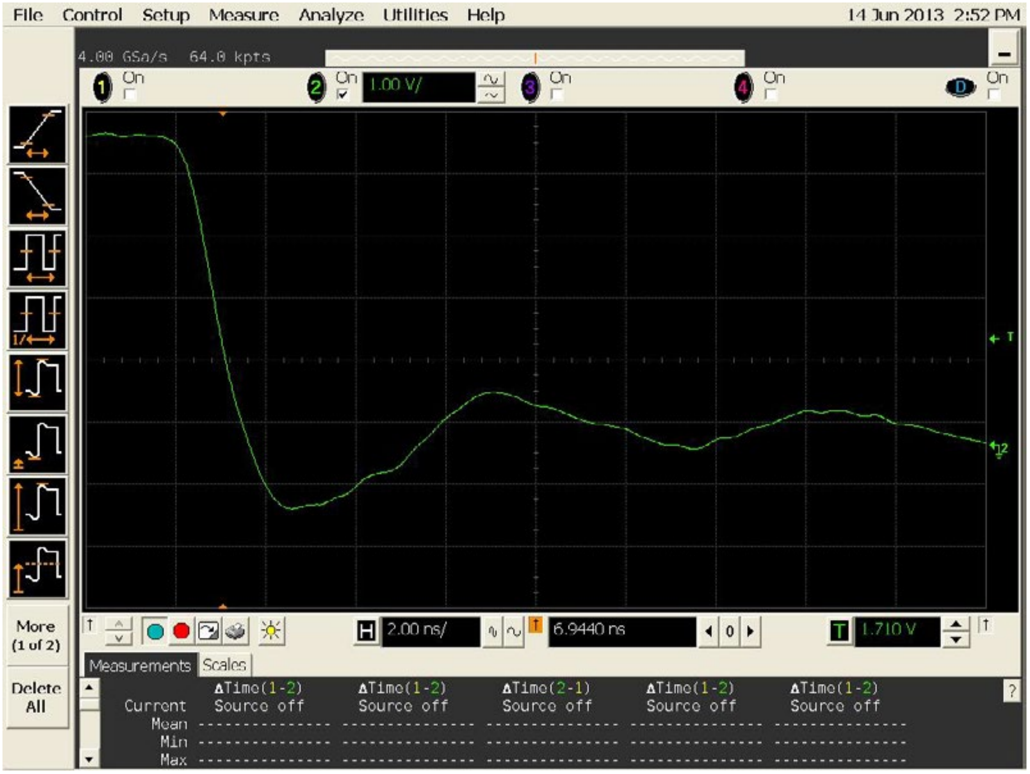


Figure 16a DUT 7437 Pre-Irradiation Falling Edge

Figure 16b DUT 7437 Post-Annealing Falling Edge

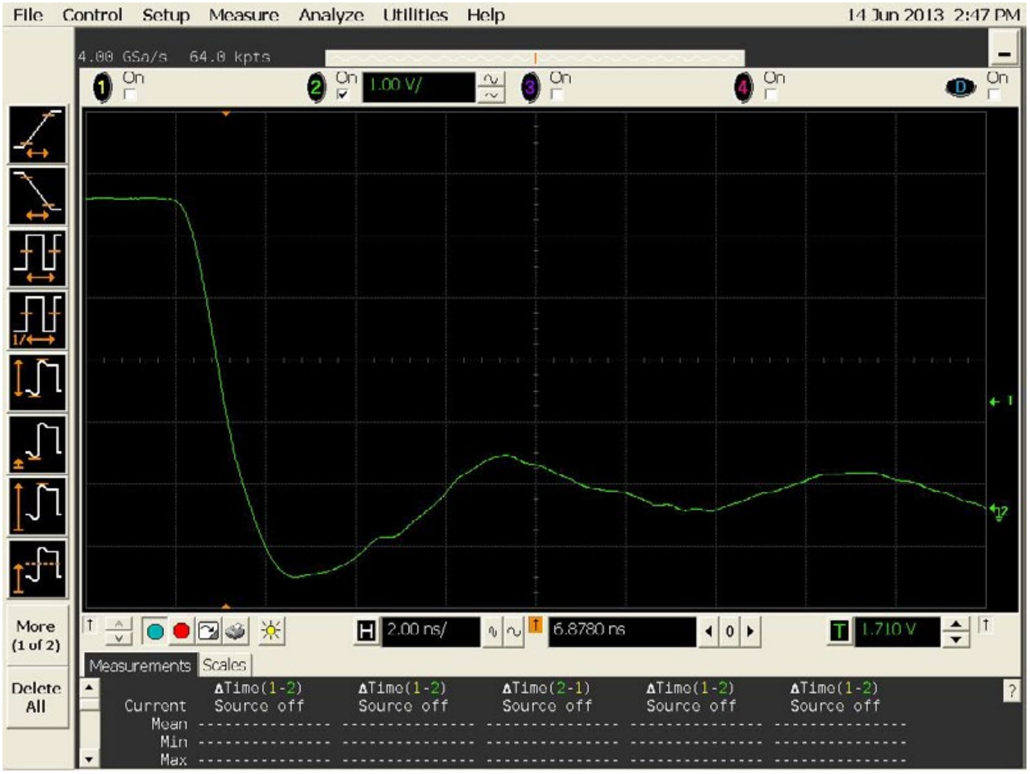


Figure 17a DUT 7442 Pre-Irradiation Falling Edge

Figure 17b DUT 7442 Post-Annealing Falling Edge

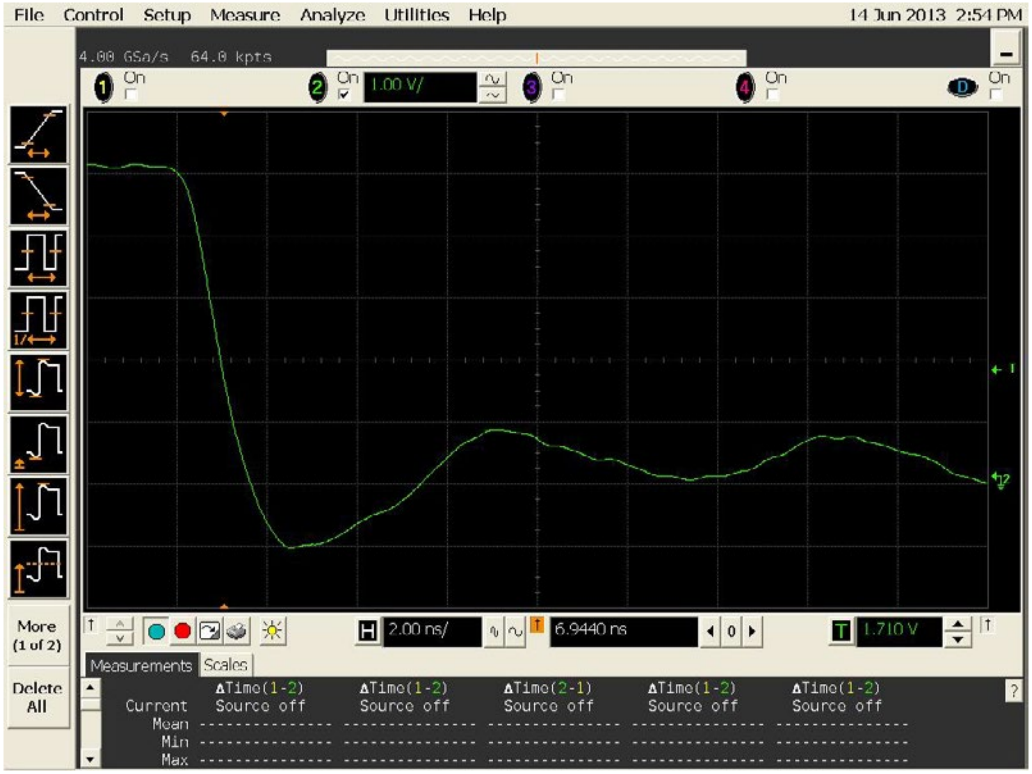


Figure 18a DUT 7459 Pre-Irradiation Falling Edge

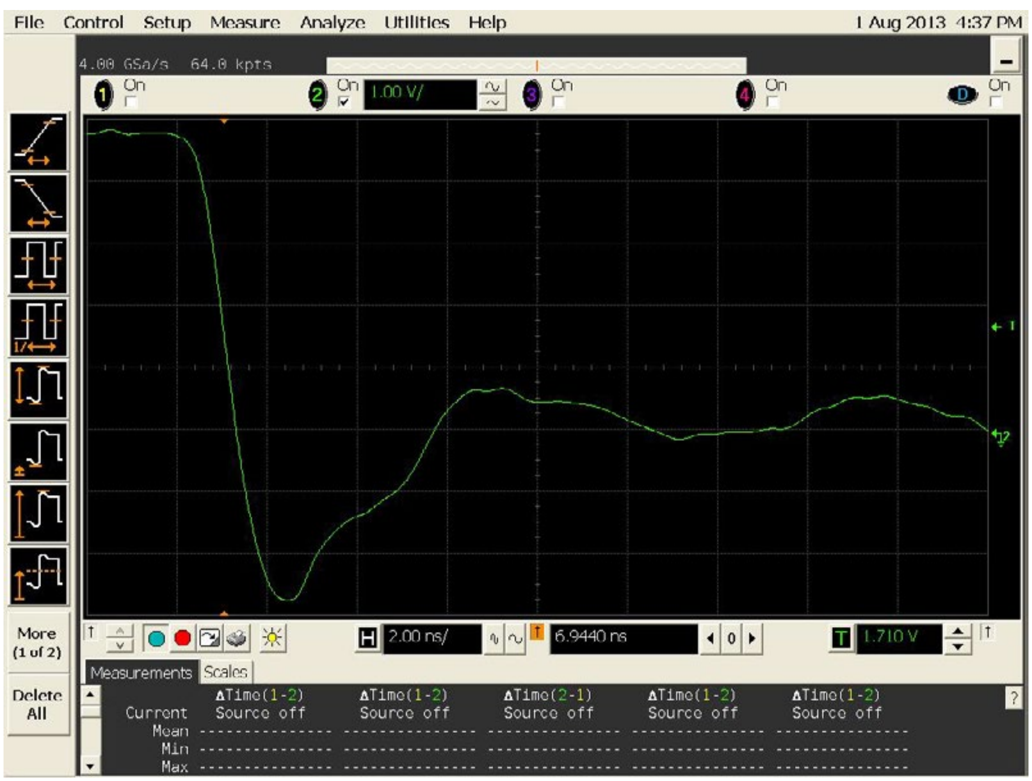


Figure 18b DUT 7459 Post-Annealing Falling Edge

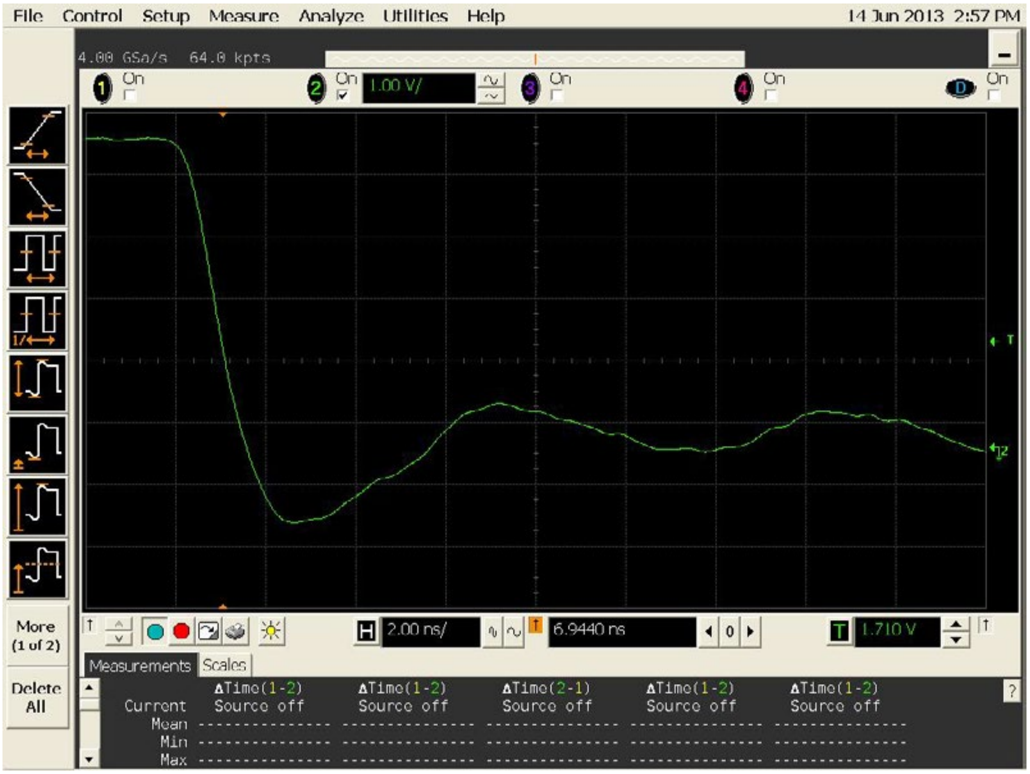


Figure 19a DUT 7508 Pre-Irradiation Falling Edge

Figure 19b DUT 7508 Post-Annealing Falling Edge

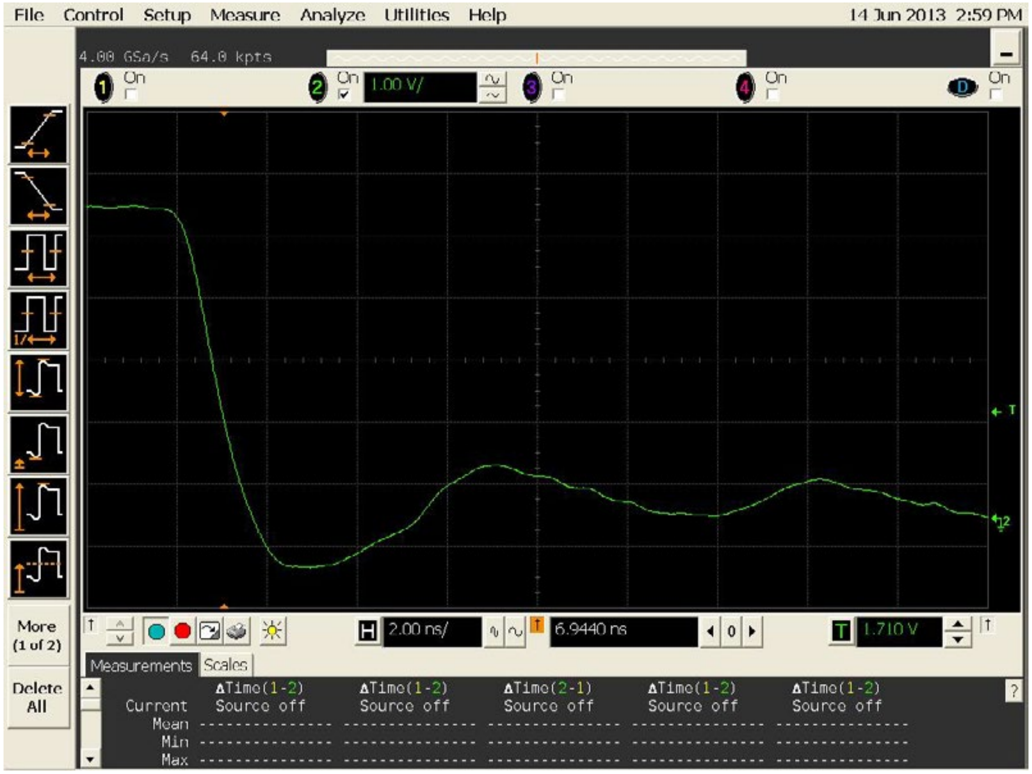


Figure 20a DUT 7579 Pre-Irradiation Falling Edge

Figure 20b DUT 7579 Post-Annealing Falling Edge

Appendix A: DUT Bias

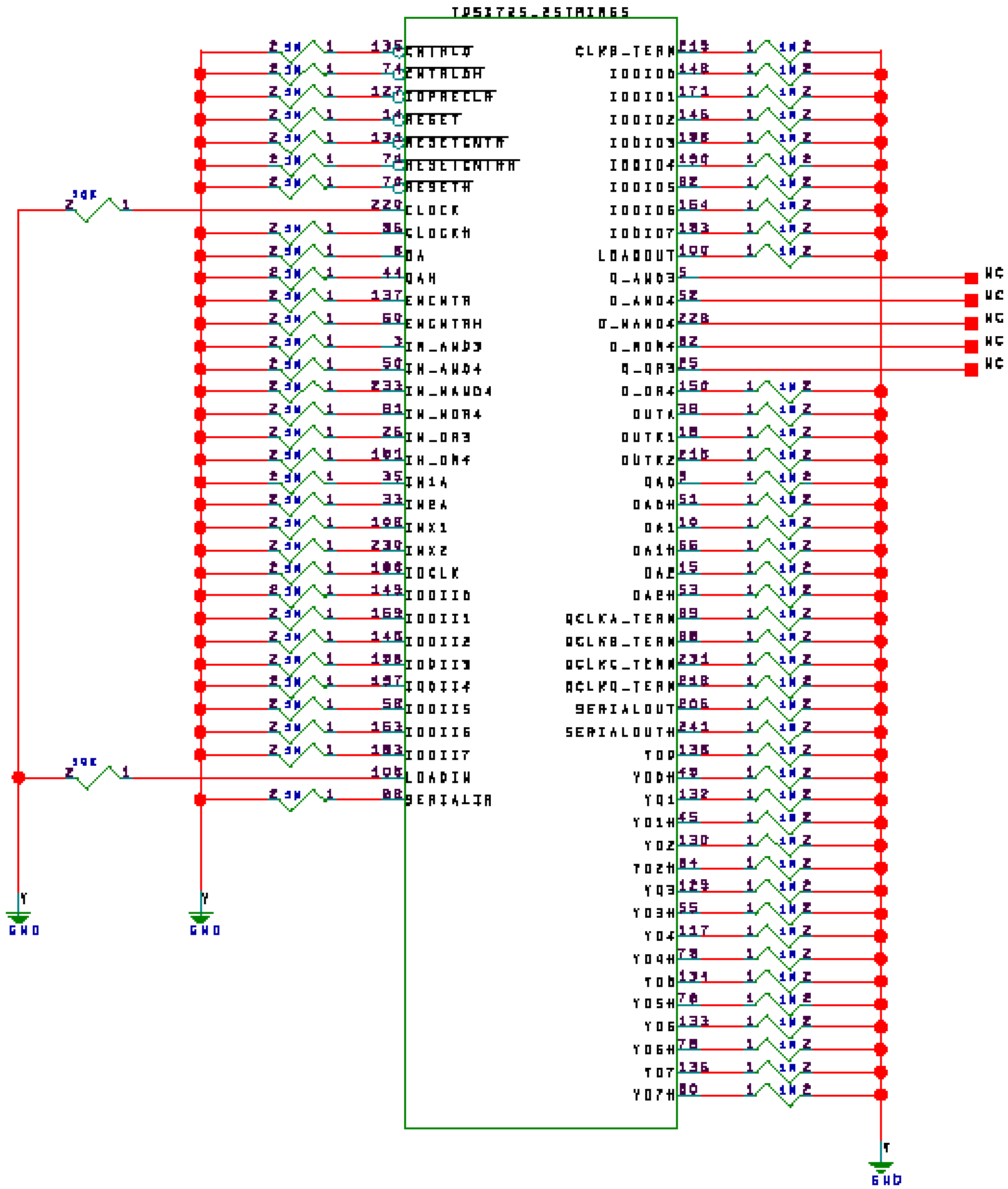


Figure A1 I/O Bias During Irradiation

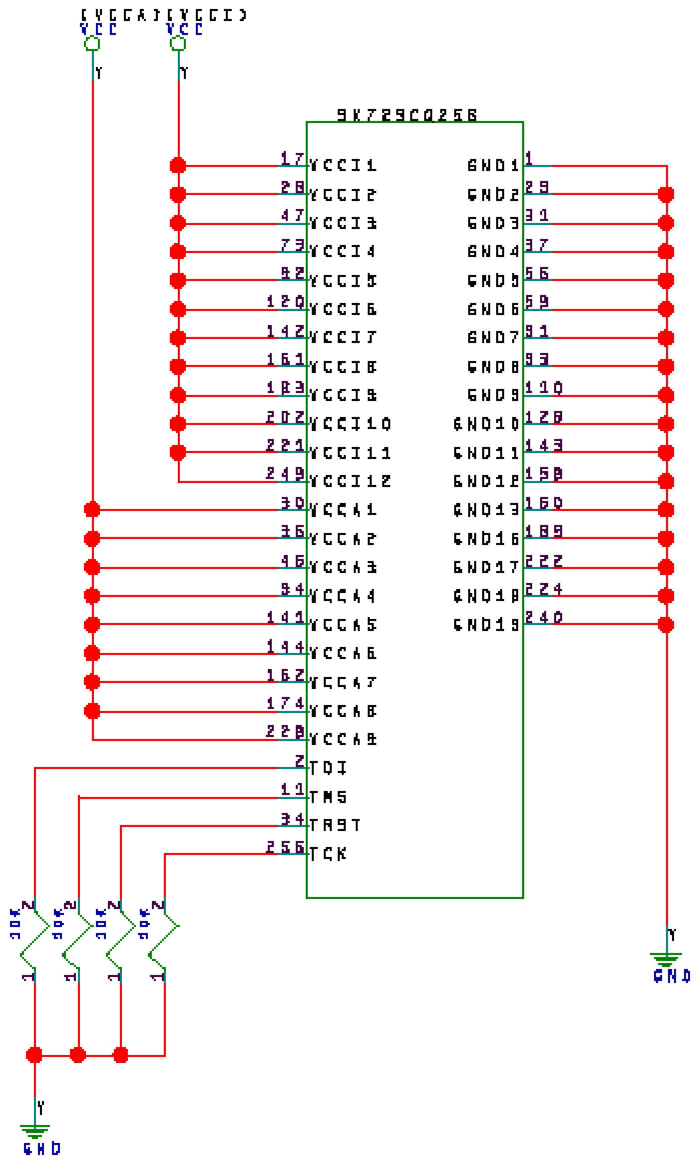
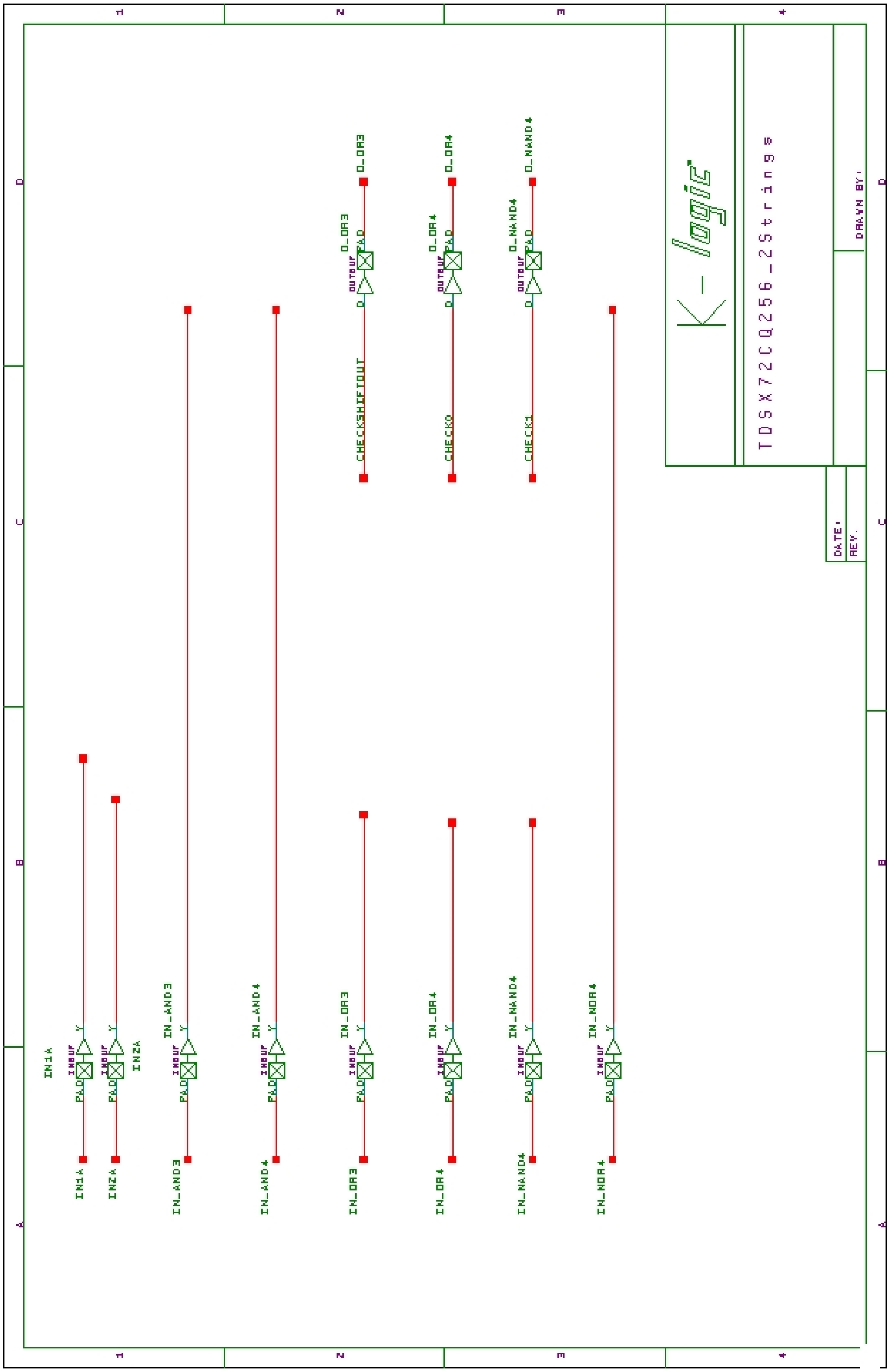
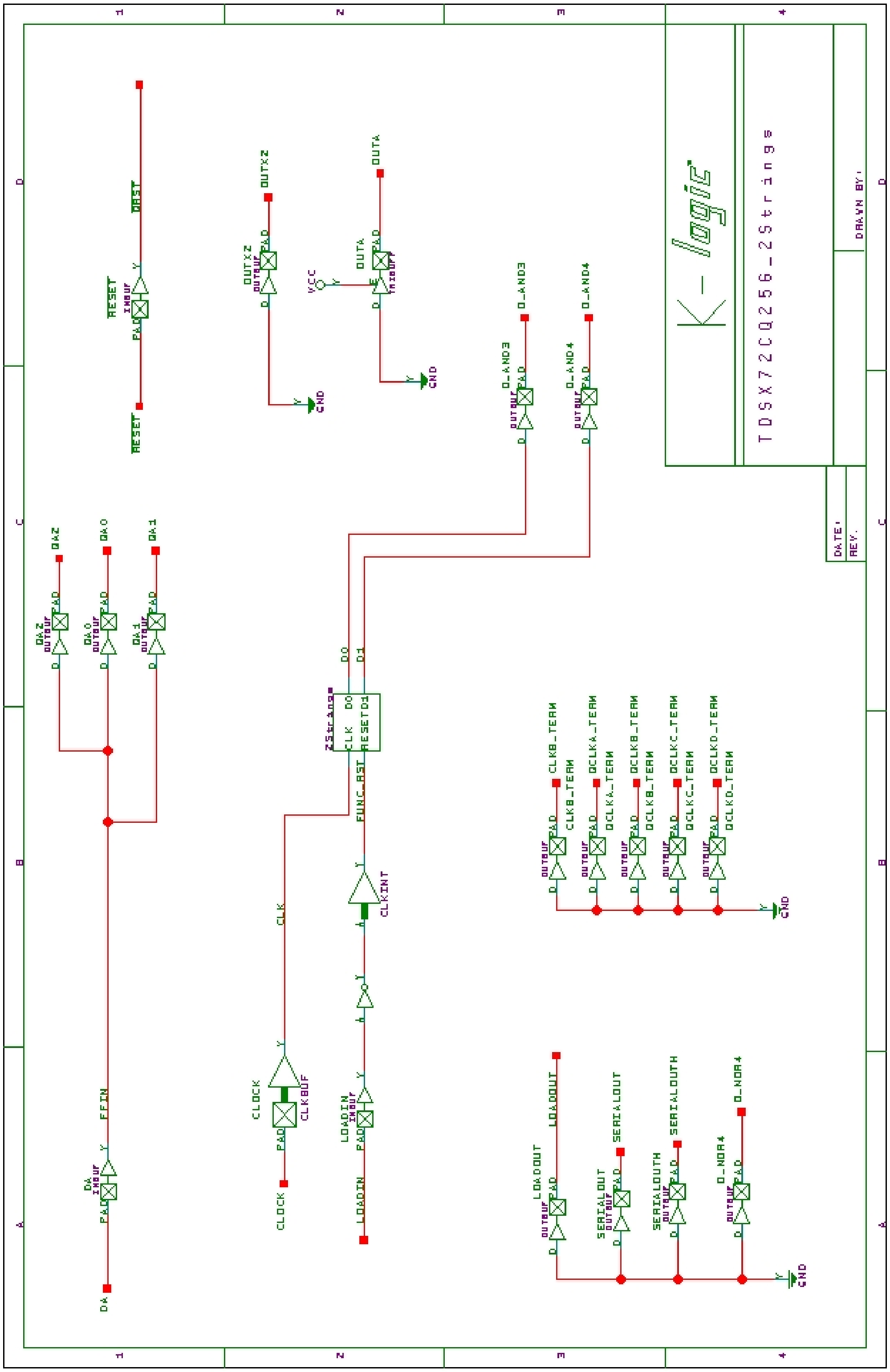


Figure A2 Power Supply, Ground and Special Pins Bias During Irradiation

Appendix B: DUT Design Schematics

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D_AND4
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QA1
2Strings
CLK
D0
D1
RESET
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
INBUF
OUTBUF
PAD
FFIN
DA
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QCLKB_TERM
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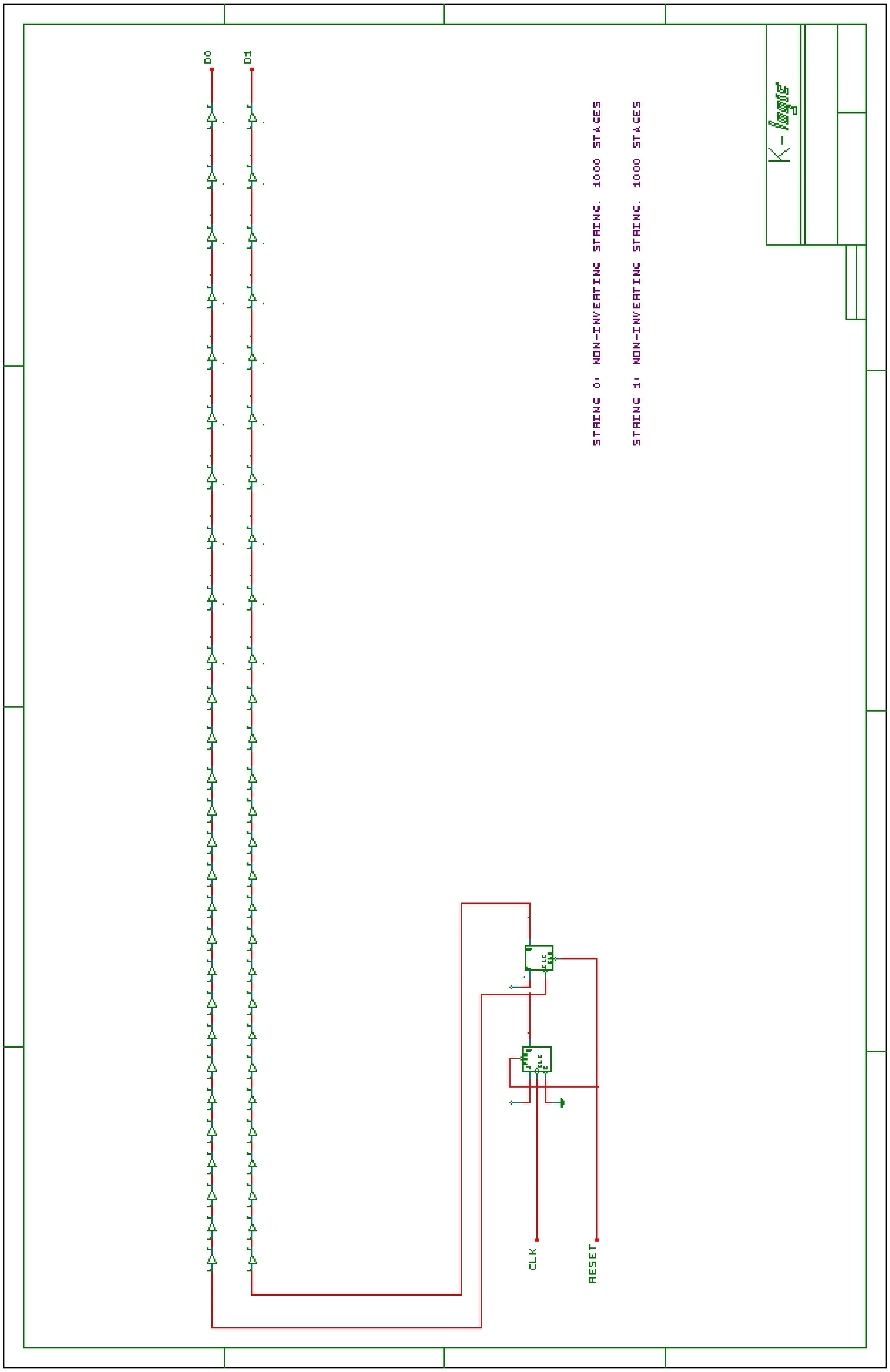
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D1
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STRING 1: NON-INVERTING STRING, 1000 STAGES
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RESET


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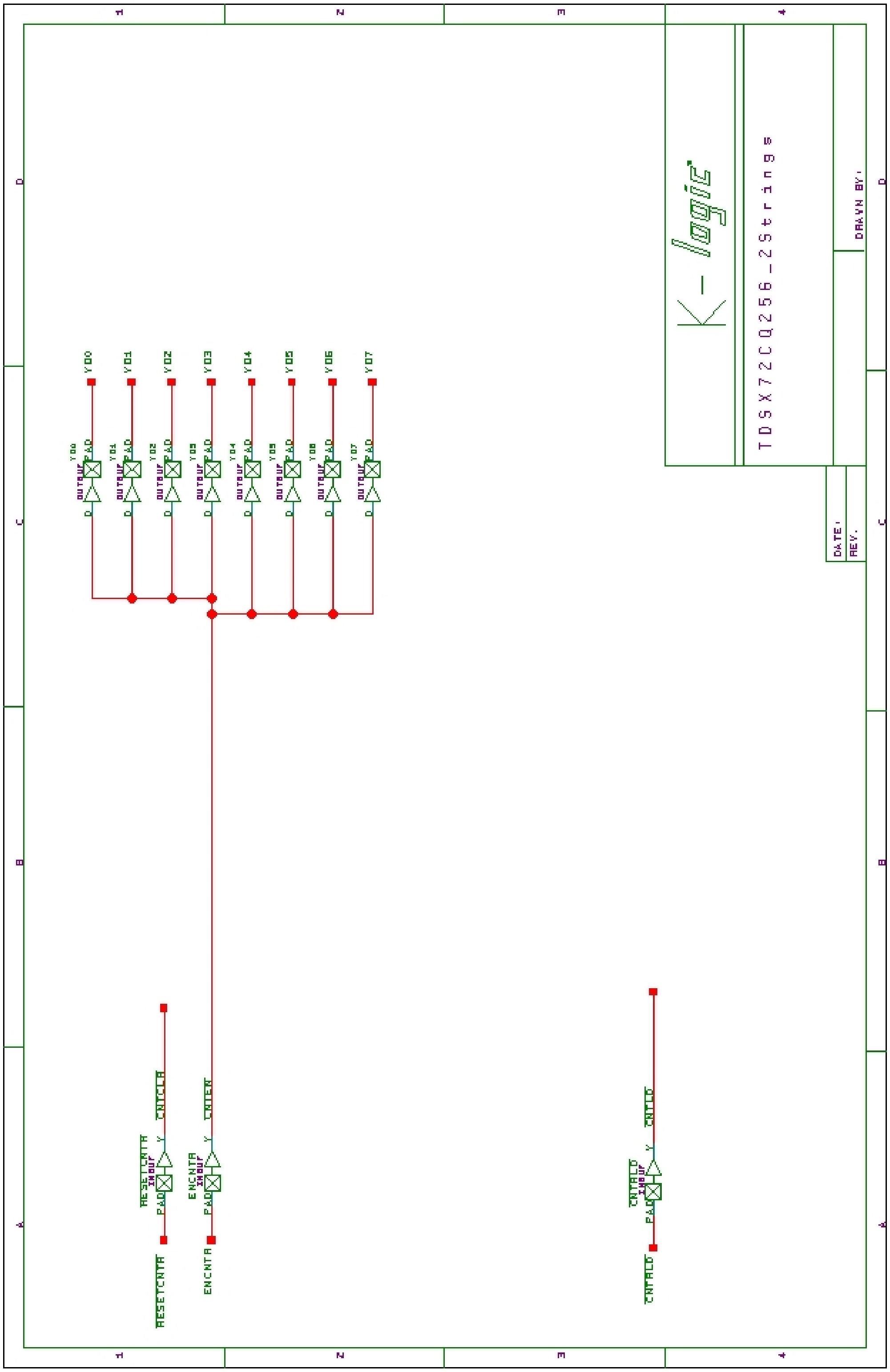
REV.



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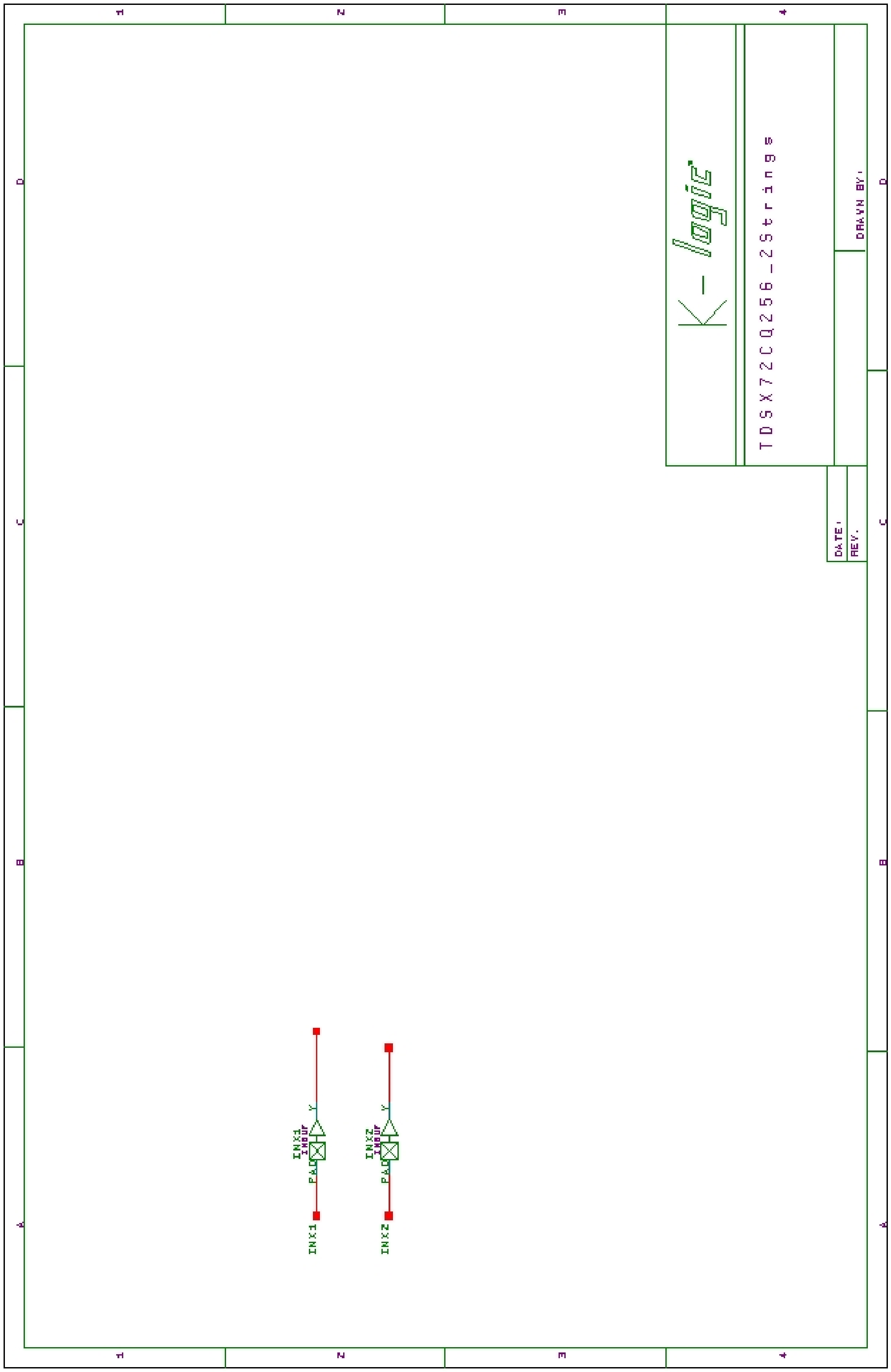
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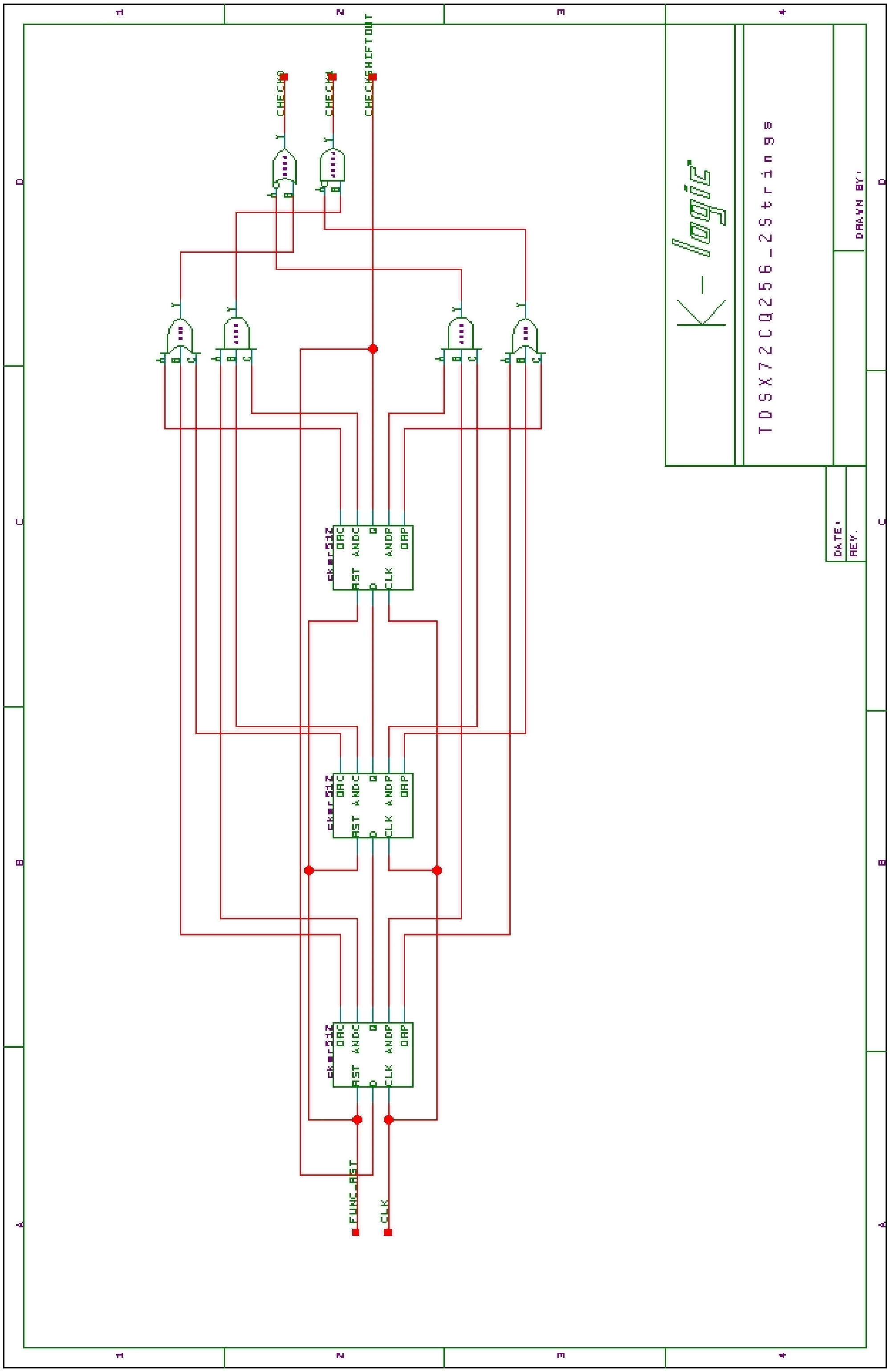
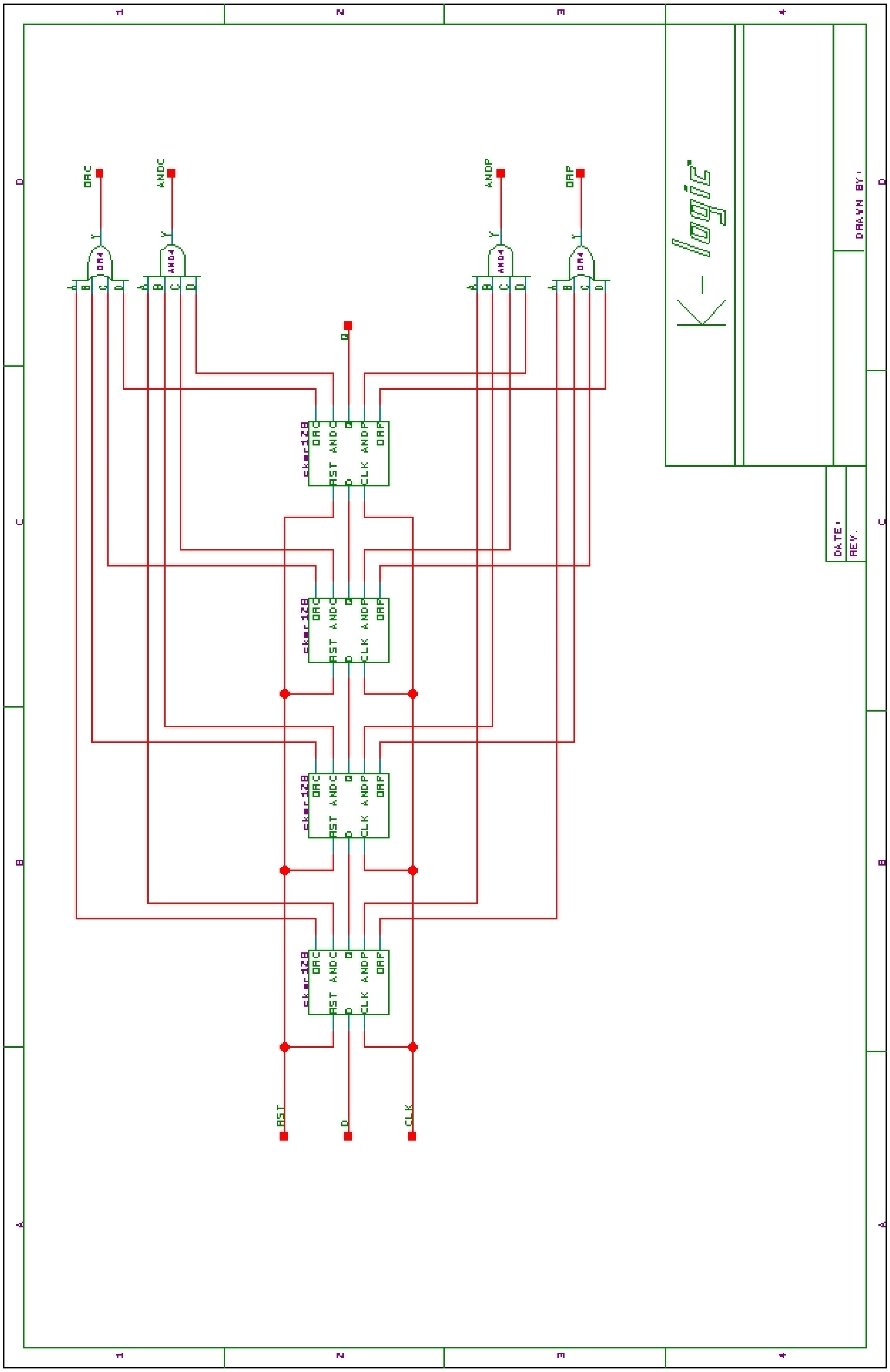
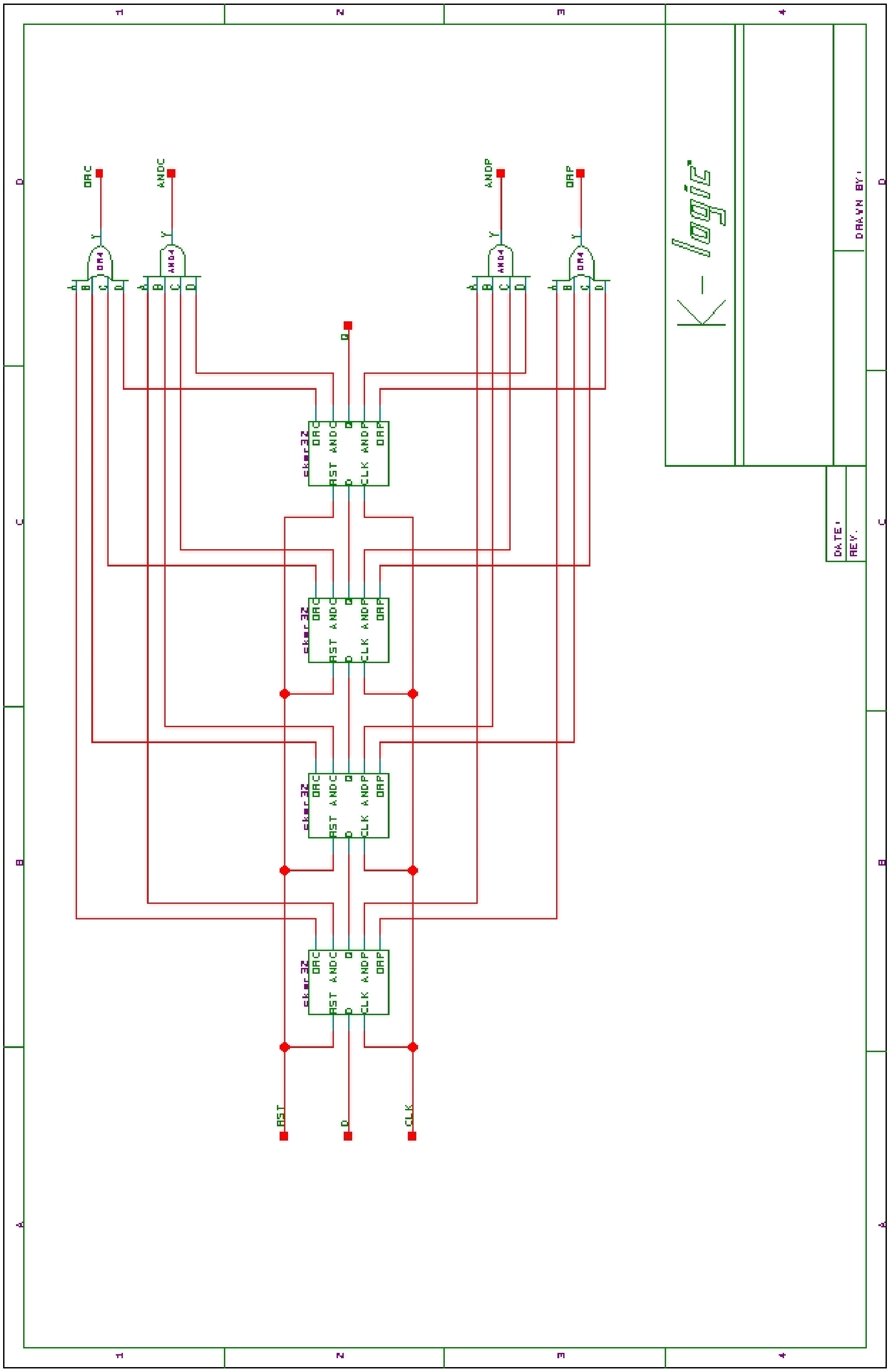
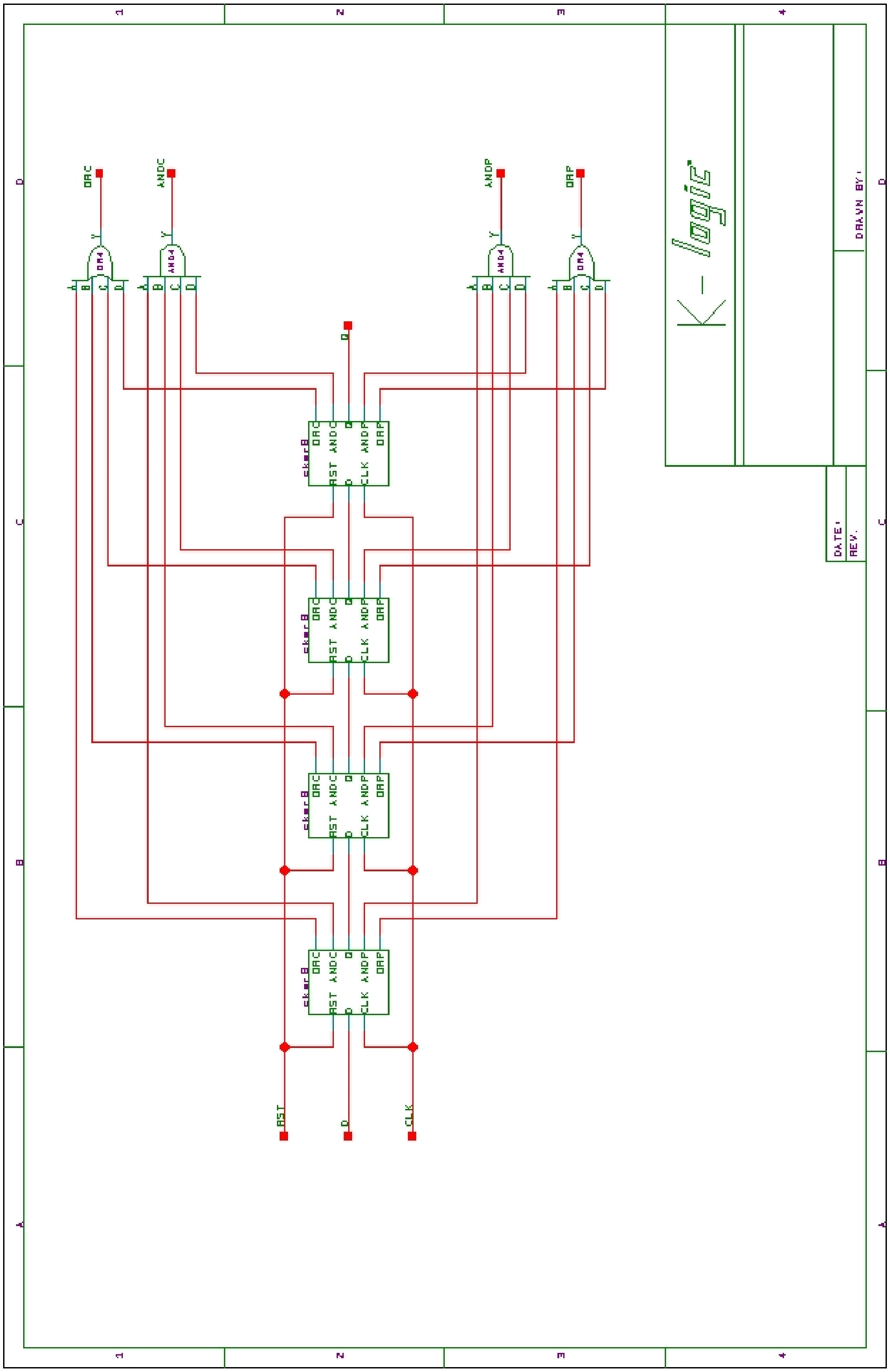
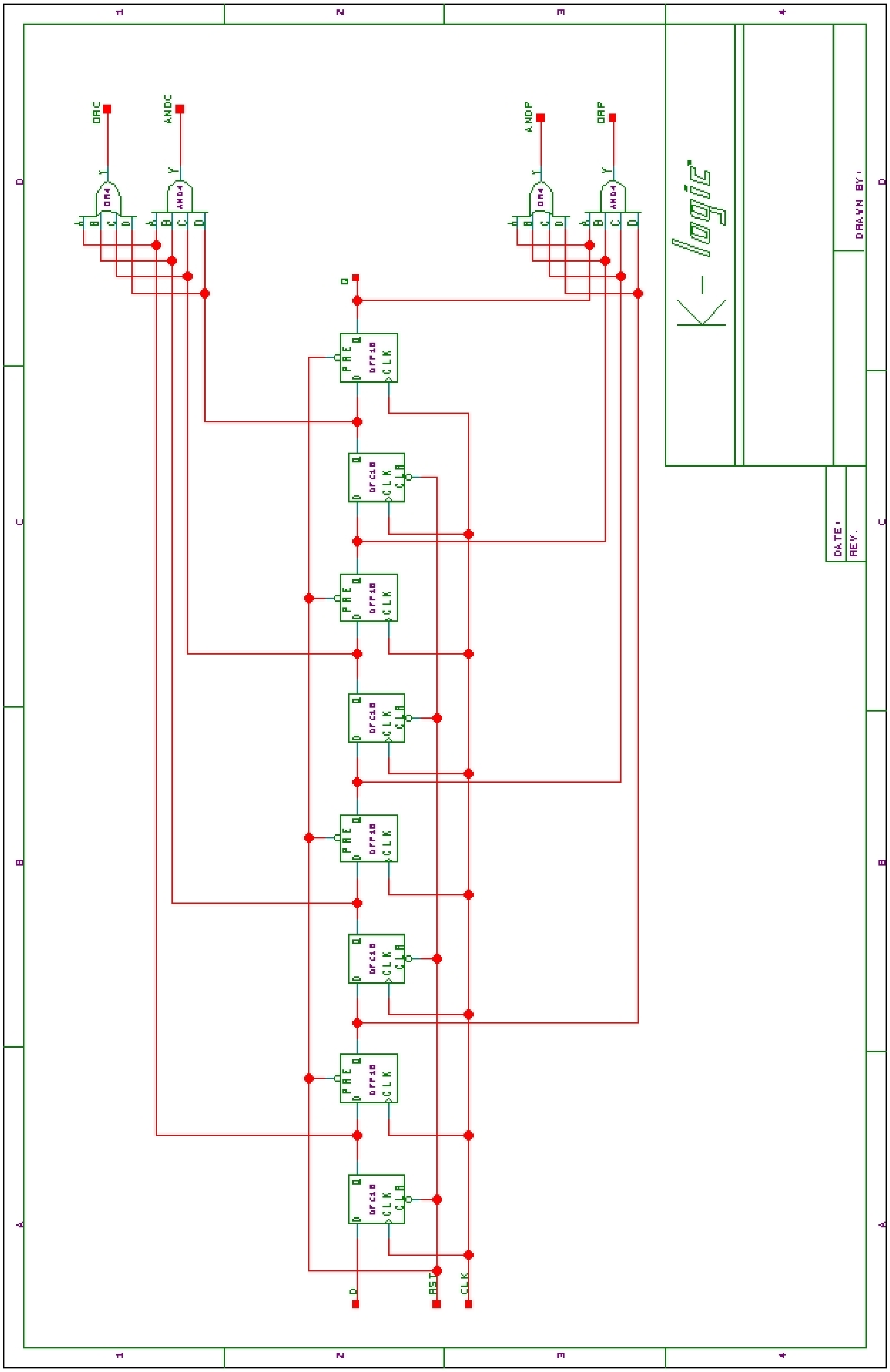
INX1
INX2

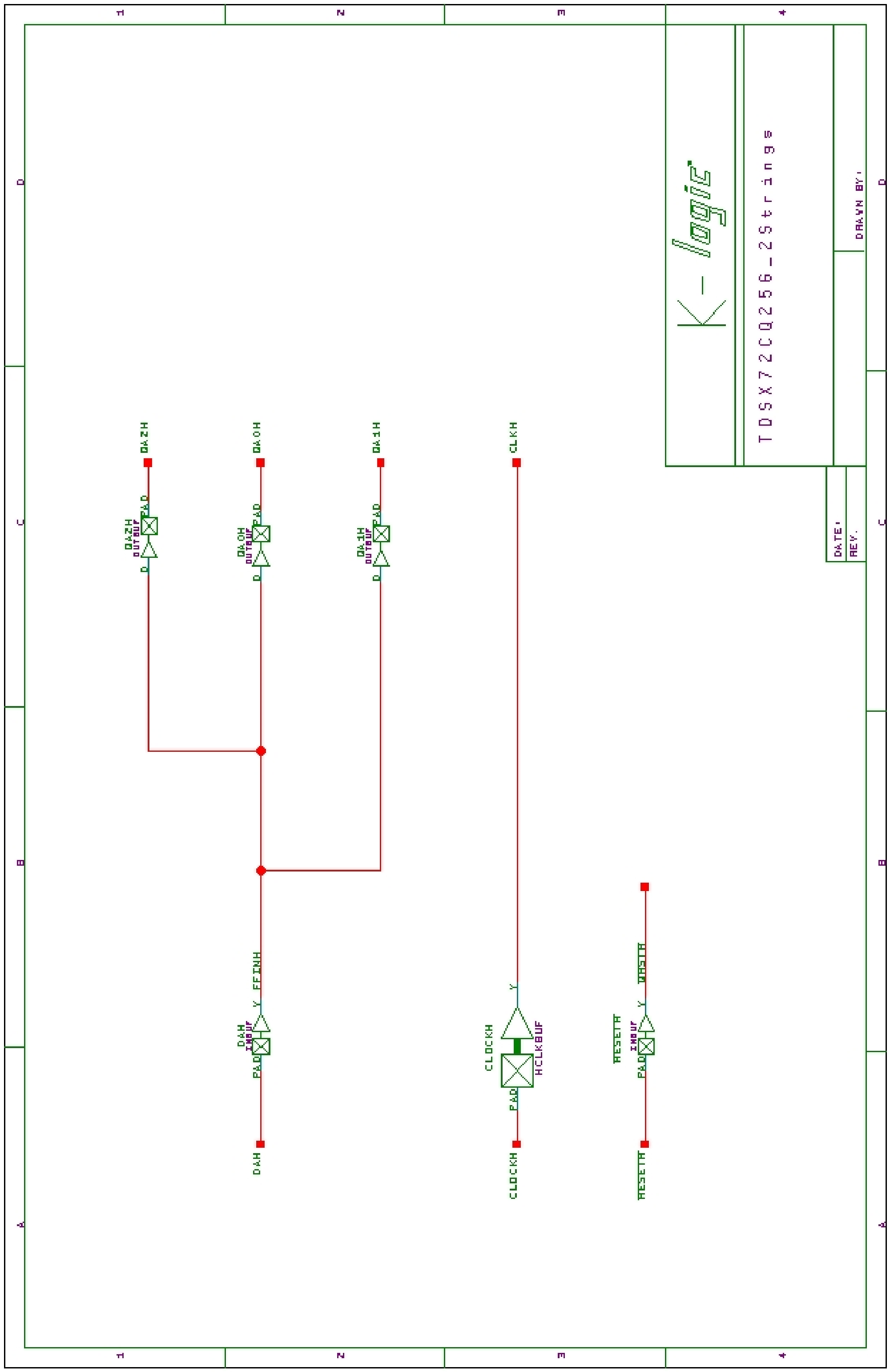

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
ORC
ANDC
ANDP
ORP
RST
D
Q
CLK
K - logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DRAWN BY:
DATE:
REV.

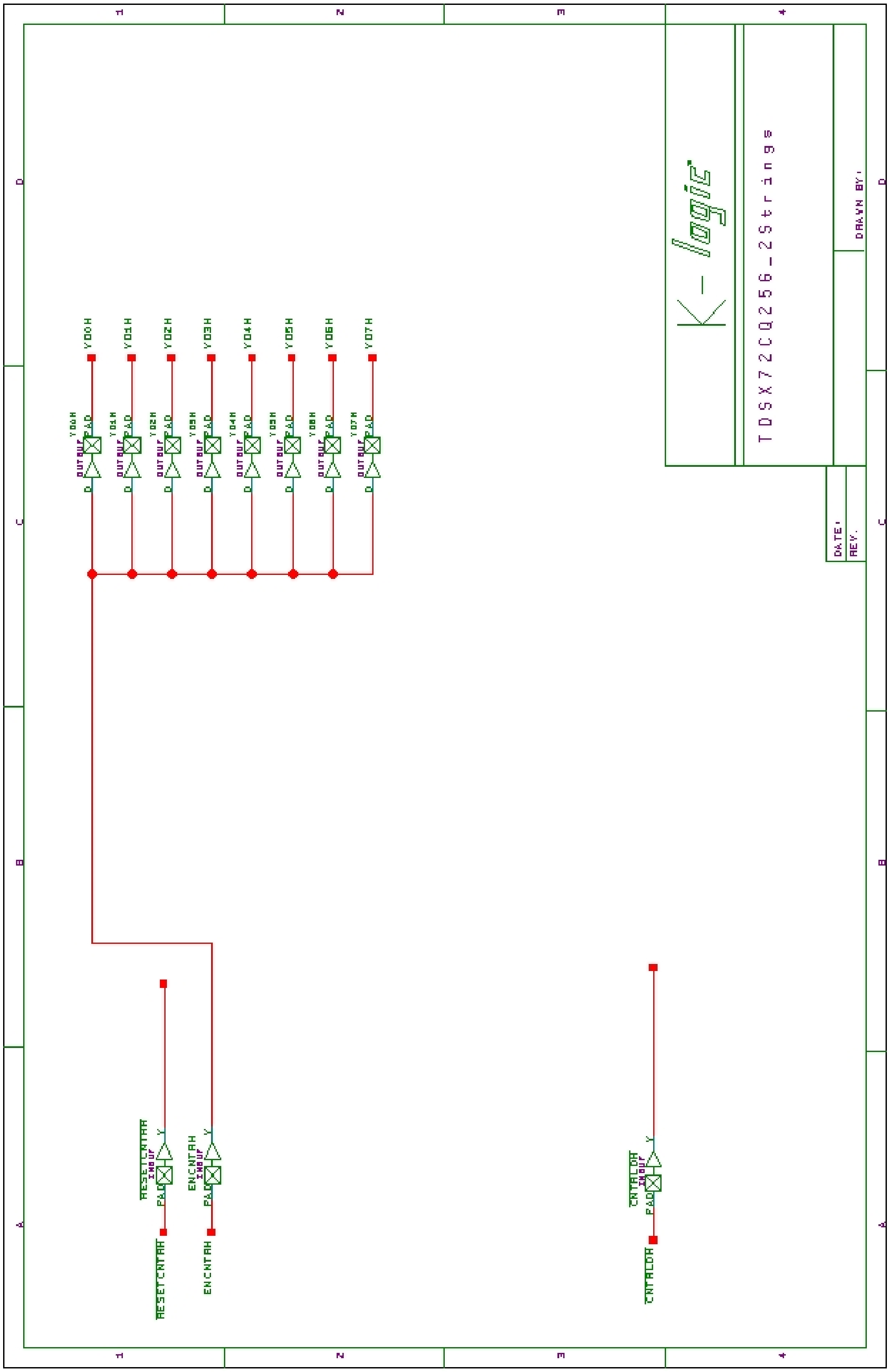

ORC
ANDC
ANDP
ORP
OR4
AND4
A
B
C
D
Y
Q
ckmr32
RST
CLK
K - logic
DRAWN BY:
DATE:
REV.
1
2
3
4

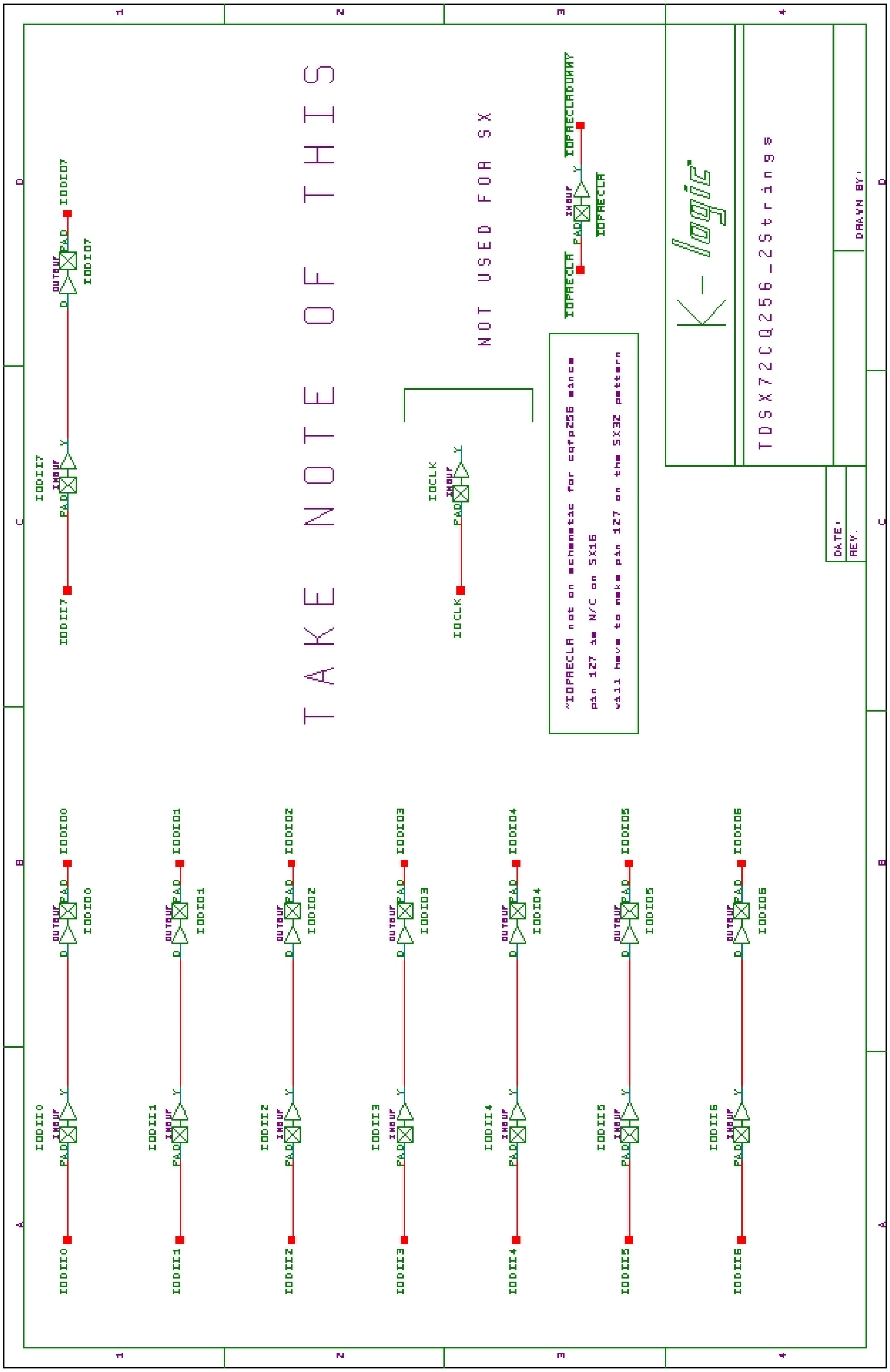

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
DATE:
REV.
DRAWN BY:

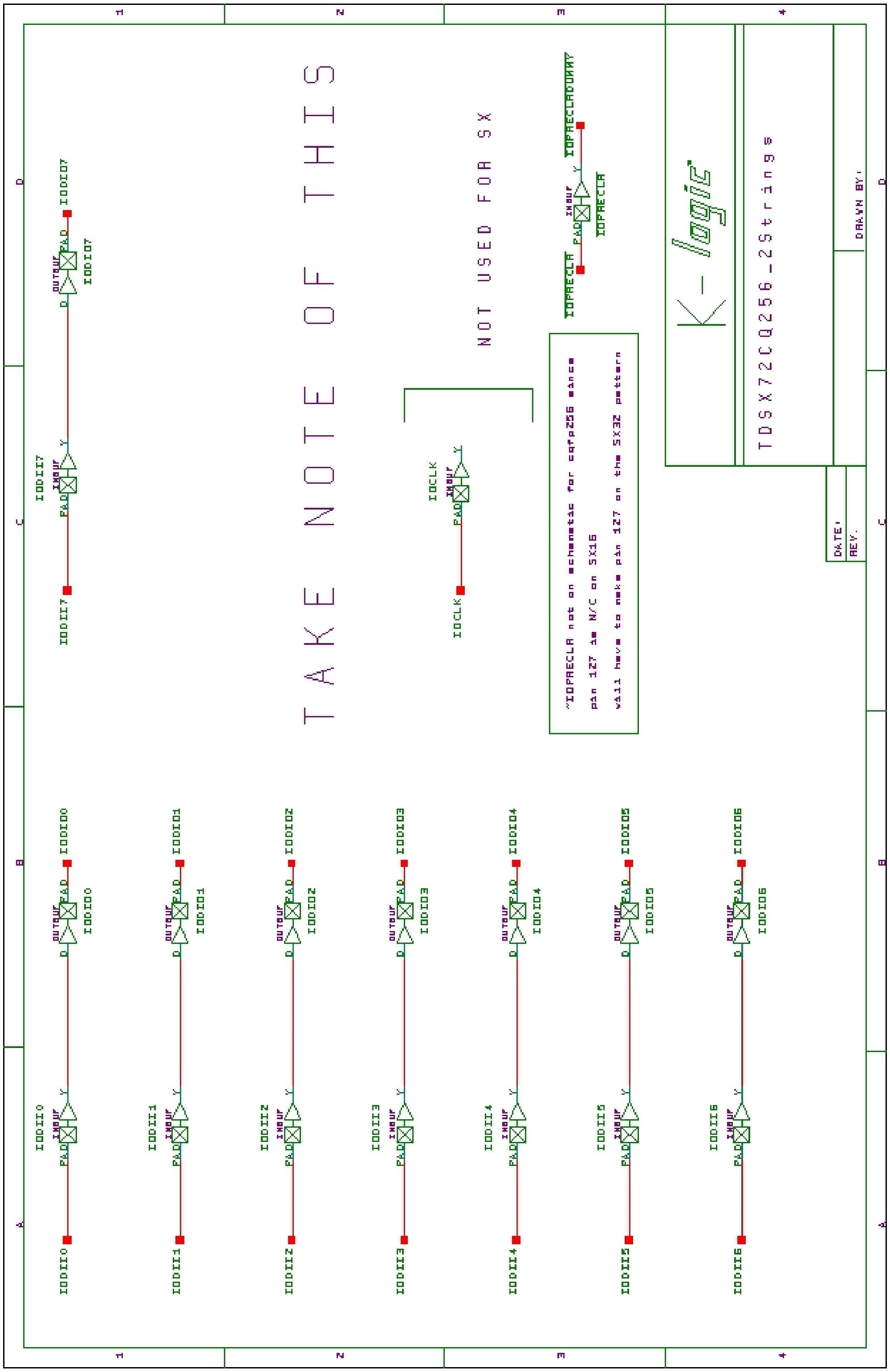

ORC
ANDC
ANDP
ORP
Q
D
RST
CLK
K-logic
DRAWN BY:
DATE:
REV.

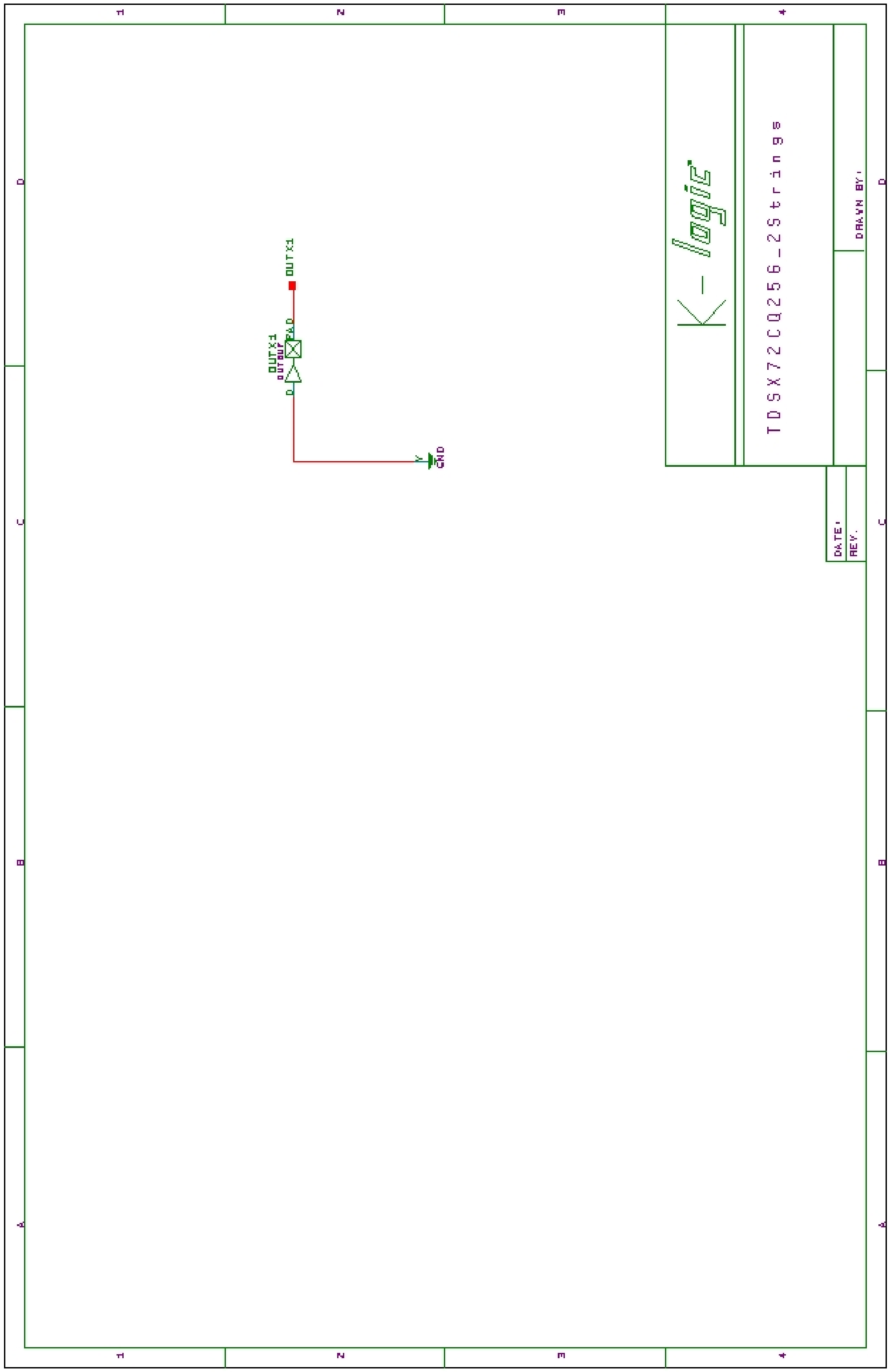


TDSX72CQ256_2Strings
DA2H
DA0H
DA1H
CLKH
DAH
CLOCKH
RESETH
OUTBUF
INBUF
HCLKBUF
FFINH
DATE:
REV.
DRAWN BY:


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLDH


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRDUMMY
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODII7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6
IODIO7
INBUF
OUTBUF
PAD


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
K - logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


OUTX1
PAD
OUTBUF
D
Y
GND
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

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