Power Measurements on IGLOO2 Evaluation Kit

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Purpose

This application note describes the steps to use the IGLOO®2 field programmable gate array (FPGA) evaluation kit to measure power and understand the results. The aspects and measurement methods that are discussed in this application note can be applied to any user-specific design project.

Introduction

IGLOO2 FPGA has a low power advantage among other devices in its class. When designing for low power, designers often consider factors such as operating temperature, activity factor, device variables and so on. In case of any uncertainty about power performance, the IGLOO2 evaluation kit can be used to program the design onto the device and measure actual power. FPGA-power measurement is far from trivial. In part, measuring FPGA power can be complicated because there are typically several power nodes connected to common voltage rails as is the case on the IGLOO2 Evaluation Kit. A “how-to” understanding of the IGLOO2 Evaluation Kit and use of the Libero® System-on-Chip (SoC) software is required to make this process easy.

The economical IGLOO2 FPGA Evaluation Kit features the 12000 logic element M2GL010T-1FGG484 device and RJ45 for 10/100/1000 Ethernet, one Full-Duplex SERDES Lane through sub miniature version A (SMA) connectors.The IGLOO2 memory management system is supported by 512 MB of on board mobile LPDDR, 64 MB SPI flash, USB-UART connections as well as I^2C, SPI and GPIO headers. The kit includes a 12 volt (V) power supply but can also be powered through the PCIe edge connector and a FlashPro4 JTAG programmer for programming and debugging. The kit allows for development and testing of PCIe Gen2 x1 lane designs, as well as testing of the FPGA transceiver’s signal quality using full-duplex SERDES SMA pairs. Test points and circuitry are provided to allow power measurements.

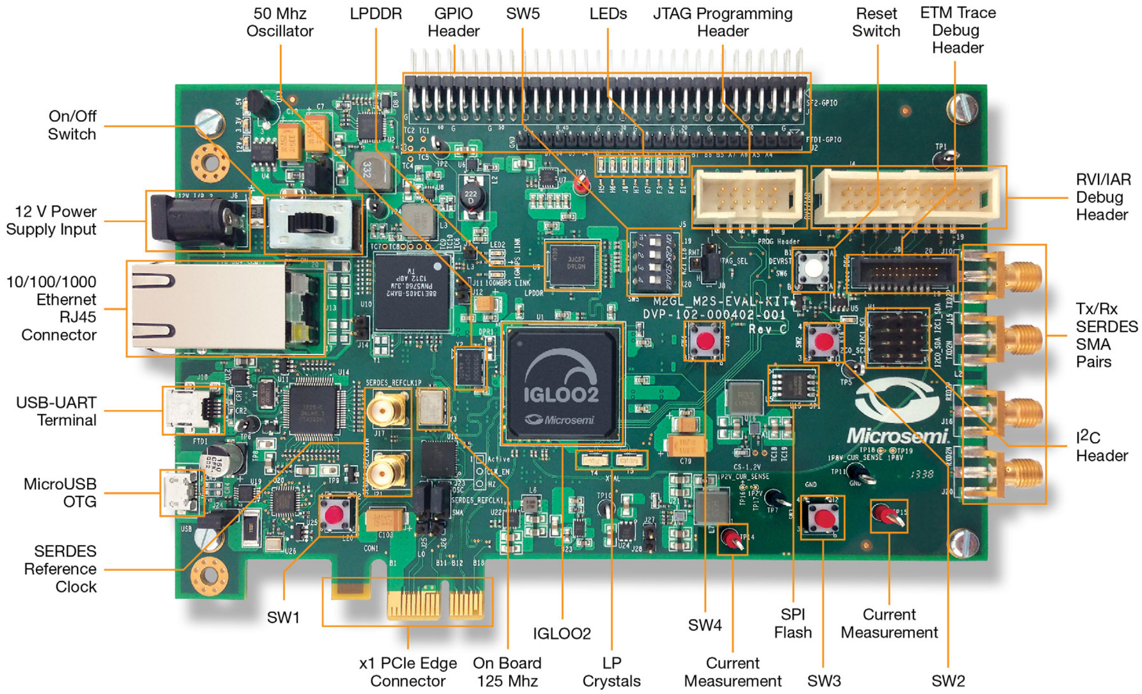

Figure 1 **• IGLOO2 Evaluation Kit**

Microsemi® Libero SoC software is a comprehensive software toolset for designing with Microsemi FPGA and SoC FPGAs. The Libero SoC software supports Microsemi's IGLOO2, SmartFusion2, SmartFusion, IGLOO, ProASIC3, and Fusion families, managing the entire design flow from design entry, synthesis, and simulation, through place-and-route, timing, and power analysis, with enhanced integration of the embedded design flow. The integrated power management guidance to properly optimize power of the devices based on the criteria of the design is specific to SmartFusion2 and IGLOO2.

The following terminology is used to understand the power consumption:

- **Standby/Static Power Consumption**: Power being consumed by a programmed device when idle with no activity.
- **Dynamic Power Consumption**: Incremental power consumed by non-zero activity within a programmed device.

These terms are important concepts as several designs might be required to thoroughly highlight and understand the key power components of the device. The Libero SoC software realizes the necessary components within a design. Libero produces the needed programming of the device to control and power-down the unused portions of the device.

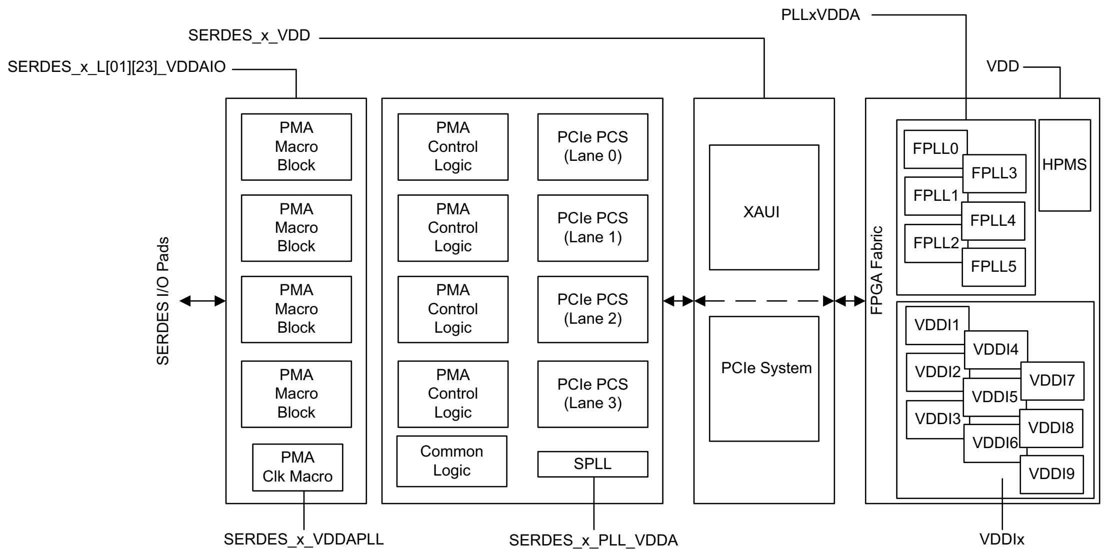

***Figure 2* • IGLOO2 Device Power Distribution**

Figure 2 depicts the power supply scheme of the IGLOO2 device. It specifically highlights the FPGA Core, fabric PLLs, and dedicated SERDES power supplies. Table 1 references the power distribution network on the IGLOO2 Evaluation Kit and highlights connections to the board for the purpose of understanding the various shared supplies. PCB connections that reference a plane are connected together with other supplies requiring the same voltage. Consequentially, specific power characteristics of the supplies must be derived with the other supply elements. Whereas PCB connections noted as node have individual power connections that permit direct power measurements from the board.

***Table 1* • IGLOO2 Power Supply Connections**

M2GL010T **Power Supply Name**	**Supply Value**	**PCB Connection**
SERDES_0_L[01][23]_VDDAIO	1.2 V	Plane
SERDES_0_VDD (Note 1)	1.2 V	Plane
PLLxVDDA	3.3 V	Node
VDD	1.2 V	Plane
SERDES_0_VDDAPLL	2.5 V	Node
SERDES_0_PLL_VDDA	3.3 V	Node
VDDI	Various	Plane
Note 1: SERDES_0_VDD is connected to Core VDD within the device package.		

Refer to the *IGLOO2 Evaluation Kit User Guide* for more details.

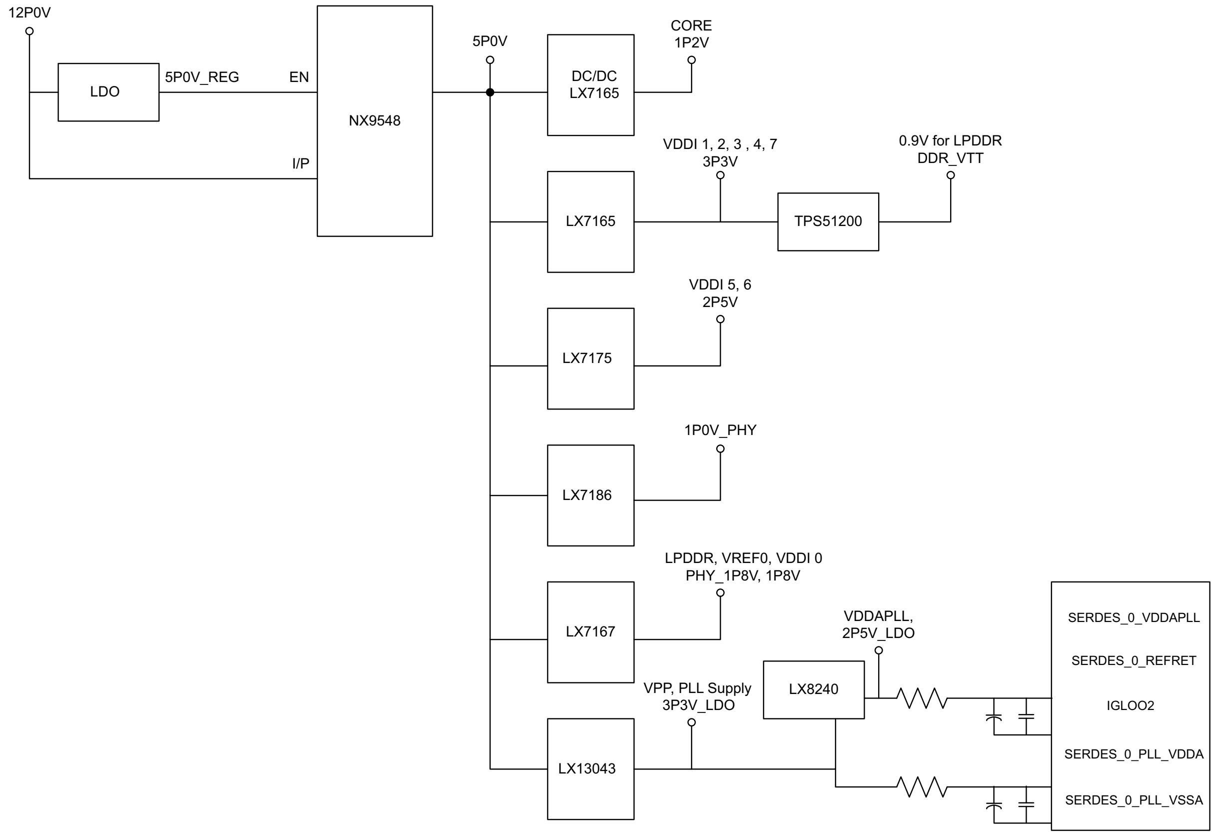

***Figure 3* • IGLOO2 Evaluation Kit Power Distribution Network**

References

Refer to Table 2 for detailed information.

***Table 2* • References**

Document	Description
IGLOO2 FPGA Datasheet	This datasheet contains IGLOO2 DC and switching charact eristics.
IGLOO2 FPGA High Speed Serial Interfaces User Guide	IGLOO2 devices integrate hard high-speed serial interfaces (PCIe, XAUI/XGXS, SERDES) for accessing external bulk memories. This document describes the IGLOO2 high-speed serial interfaces.

Table 2 • **References (continued)**

Document	Description
IGLOO2 Clocking Resources User Guide	IGLOO2 clocking resources include oscillators, FPGA fabric global network, and clock conditioning circuitry (CCCs) with dedicated phase-locked loops (PLLs). These clocking Libero SoC software resources provide flexible clocking schemes to the on-chip hard IP blocks—HPMS, fabric DDR (FDDR) subsystem, and high-speed serial interfaces (PCIe, XAUI/XGXS, SERDES)—and logic implemented in the FPGA fabric.
IGLOO2 Low Power Design User Guide	In addition to low static power consumption during normal operation, IGLOO2 devices support an ultra-low-power Static mode (Flash*Freeze mode) with power consumption less than 1 mW. Flash*Freeze mode retains all the SRAM and register data which enables fast recovery to Active mode. This document describes the IGLOO2 Flash*Freeze mode entry and exit mechanisms.
IGLOO2 Security and Reliability User Guide	The IGLOO2 device family incorporates essentially all the security features that made third generation Microsemi SoC devices the gold standard for security in the PLD industry. Also included are unique design and data security features and use models new to the PLD industry. IGLOO2 flash-based FPGA fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. This document describes the IGLOO2 security features and error detection and correction (EDAC) capabilities.
IGLOO2 Evaluation Kit User Guide	Details of the IGLOO2 Evaluation Kit functions and Libero SoC Software operating instructions including PCB schematics and design layout information.

Description of Test Methodologies

This application note discusses the purposed designs that can be applied to your designs. The measurement methods discussed can be applied to any design targeted to the IGLOO2 Evaluation Kit.

The following methods provide guidance to understand the instrumentation of the IGLOO2 Evaluation Kit to measure design power. The defined methods shows the details of how to make the measurement and interpret the results. All methods require a standard digital voltage meter (DVM). A high resolution DVM such as a Fluke Model 289 or equivalent is known to produce reliable measurements using the defined methods and strongly recommended to be used.

Measurement Methods

Method A

Core

There are three power supply types as follows:

- Core VDD(VDD)
- SERDES(SERDES_x_VDD)
- SERDES_x_L[01][23]_VDDAIO

The IGLOO2 Evaluation Kit includes capabilities to measure power. The board is equipped with active circuitry including test points and current sensing resistors surrounding the 1.2 V rail supplying the FPGA core and SERDES. VDD, SERDES_0_VDD, and SERDES_0_L[01][23]_VDDAIO are connected together to the 1.2 V supply on the IGLOO2 Evaluation Kit.

Figure 4 highlights the 1.2 V power measurement circuitry. The circuitry permits easy access the test points for greater than 10 mA measurements of the 1.2 V rail.

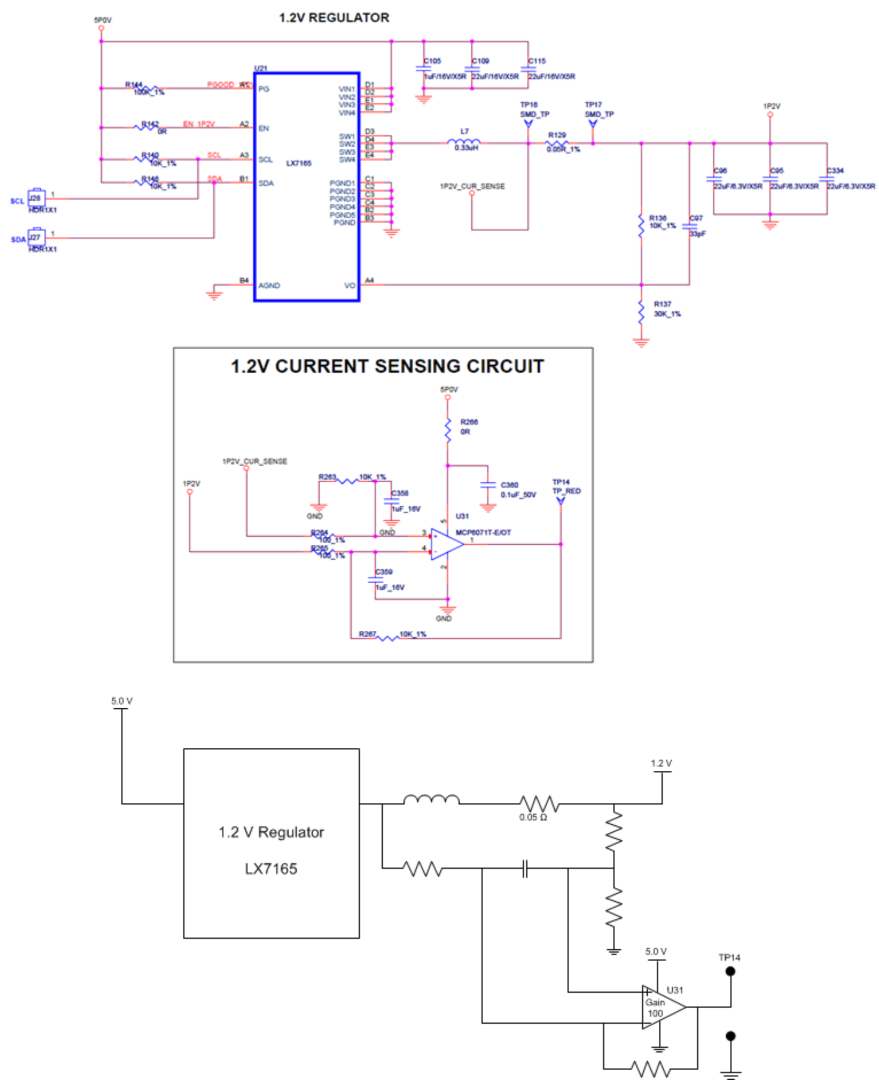

***Figure 4* • Current Sensing Circuit**

As shown in the Figure 4, R129 is a 0.05Ω sense resistor. There is an on-board op-amp with a gain of 100 that amplifies the voltage drop across this resistor and exposes it on Test Point 14 (TP14) for easy probing. Connect the positive lead of high accuracy digital voltmeter (DVM) to TP14 and the negative lead to TP7 (which is located close-by) the resulting voltage measurement indicates the voltage drop across R129.

The core power can be calculated using following equation.

$$\text{CoreCurrent (mA)} = \text{Measured Voltage (mV)} / 5 \text{ (Scaling Factor)}$$

$$\text{CorePower (mW)} = 1.2 * \text{CoreCurrent}$$

EQ 1

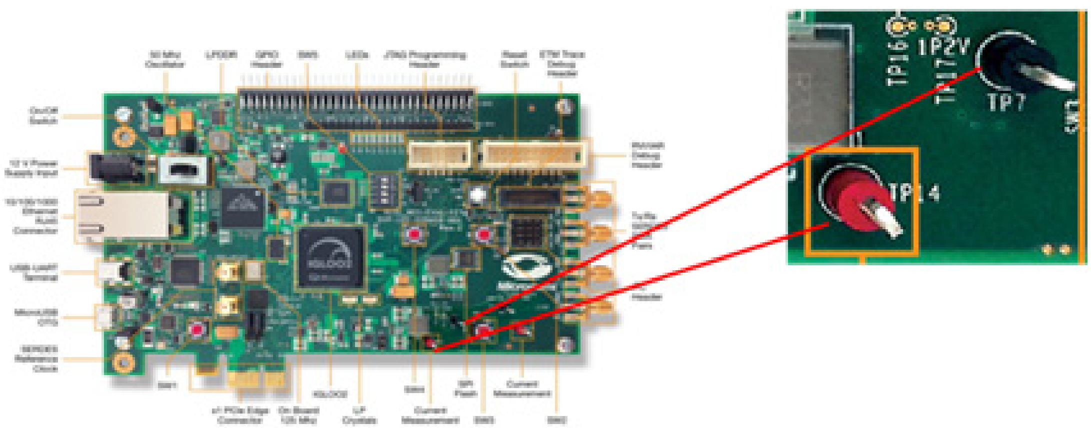

***Figure 5* • 1.2 V Measurement Test Point**

Since the 1.2 V voltage supply is shared between the FPGA core and portions of the SERDES blocks, two designs can be used to separate the power components. One design including a SERDES and one without a SERDES instantiation is useful to measure and derive the power requirements. The Libero software will correctly program all aspects of the two designs accordingly which accurately represents the power components of the device. A comparison of the power consumption of the 1.2 V board supply sub-divides the individual power components of the FPGA core and SERDES.

Notes about SERDES Power Measurements

1. Designs including SERDES should be RX terminated. Lane 1 is recommended on the IGLOO2 Evaluation Kits as Lane1 connects the RX and TX on the board which provides proper termination. Other lanes can be used but you should be aware that un-terminated RX draws slightly more power. Lane 0 can be terminated by using a PCIe slot, Lane 2 requires coaxial cables to connect the RX and TX together to provide termination and Lane 3 is terminated although not directly looped together.

   Un-terminated lanes are subject to higher than expected power consumption.
2. EPCS modes expose user access to EPCS_PWRDN pins on the SERDESIF. This permits you to control the power-up and down of each SERDES lane. However, this only controls a small section of the SERDES I/O power. The PWRDN pins are not available in any other protocol-based modes (such as PCIe or XAUI). In EPCS mode, pin EPCS_PWRDN[] is used to put only the PMA Rx and Tx macros into low power mode. Other internal registers define the state of power to other circuitry within the SERDES block, that is, whether CDR PLL is to be reset or kept in frequency lock mode. This provides users a trade off between lower power and shorter wake up time.
3. If a lane is totally unused, the Libero SoC software configures the lane to completely power down/disable the SERDES to achieve maximum power saving and is the recommended method for power management of the SERDES lanes.

Method B

Standby Power

Inserted in series between power rail outputs and the FPGA supply input pins is a small precision resistor which creates a small voltage drop which, by Ohm's Law, is proportional to the flowing current. Measuring this voltage gives you the current being supplied to FPGA.

For very low-power measurements such as standby power, the direct voltage measurement across the series resistor is recommended to be used. This method directly measures voltage across the 1.2 V sense resistor using a recommended precision DVM that can read sub-milli-volts.

Test points TP16 and TP17 can be used to directly measure voltage across the 1.2 V sense resistor. These testpoints are found directly adjacent to TP7.

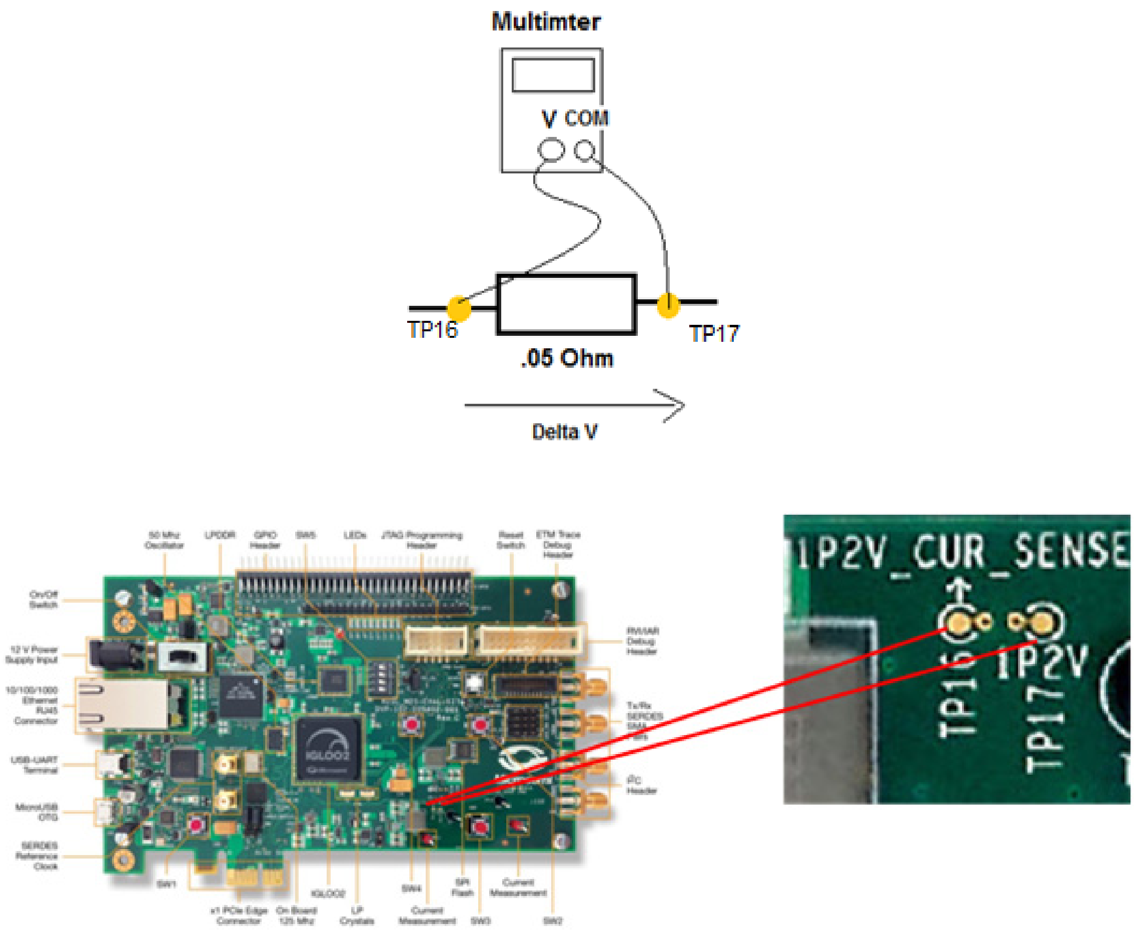

***Figure 6* • Measuring across sense resistor**

The voltage measured across sense resistor can be converted to power using the following equation:

$$\text{Power (mW)} = (\text{Voltage measured in milli Volts}/0.05) * 1.2 \quad \text{EQ 2}$$

Method C

SERDES_[0:1]_L[01,23]_VDDAPLL

Several in-series resistors are on the board to measure power of dedicated power supplies used by the SERDESIF block. There are two dedicated power connections for the SERDESIF_0 block which supply the SERDES TX/CDR PLL. The SERDES_0_L01_VDDAPLL and SERDES_0_L23_VDDAPLL provide power to LANE[0:1] and LANE[2:3] respectively from 2.5 V. They are used in conjunction with the reference clock provided to the IGLOO2 SERDESIF block either from the dedicated REFCLK input pins or from the FPGA fabric.

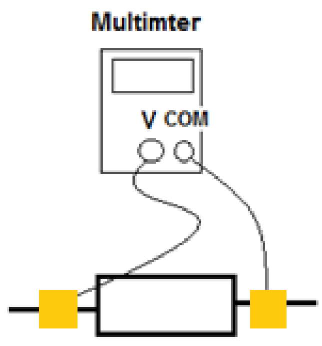

***Figure 7* • Probing of Series Resistor Voltage**

Measure the voltage across the respective 20-ohm series resistor (R234 or R233) and convert the voltage measured across resistor to power, use the following equation:

SERDES_[0:1]_L[01,23]_VDDAPLL Power (mW) = (Voltage measured in milli Volts/20) * 2.5

EQ 3

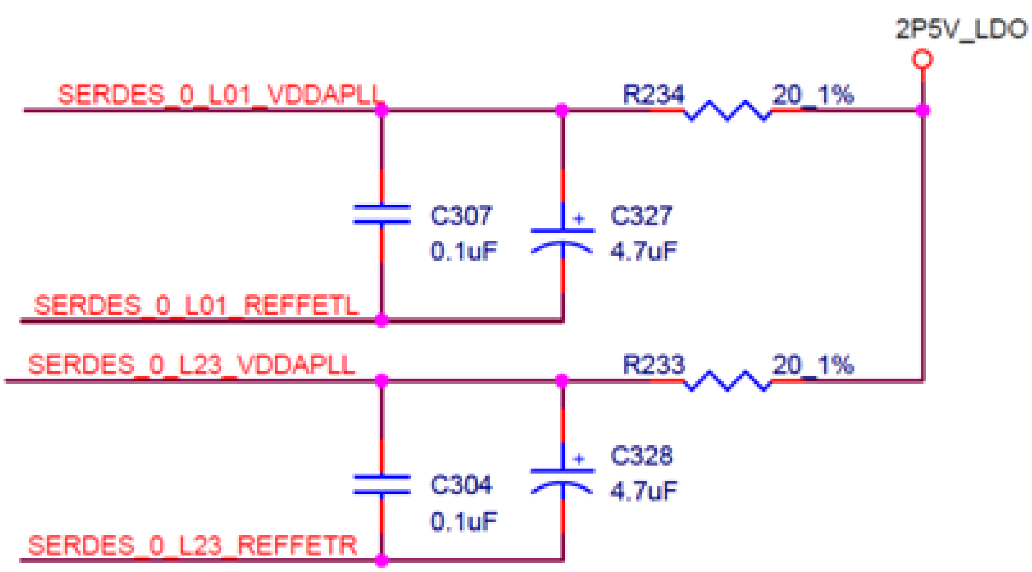

***Figure 8* • SERDESIF CDR/TX PLL Power Connections**

As shown in the Figure 8, R233 and R234 can be located on the bottom side of the board.

As shown in the layout plot Figure 9, R233 and R234 can be probed with the DVM to measure the voltage.

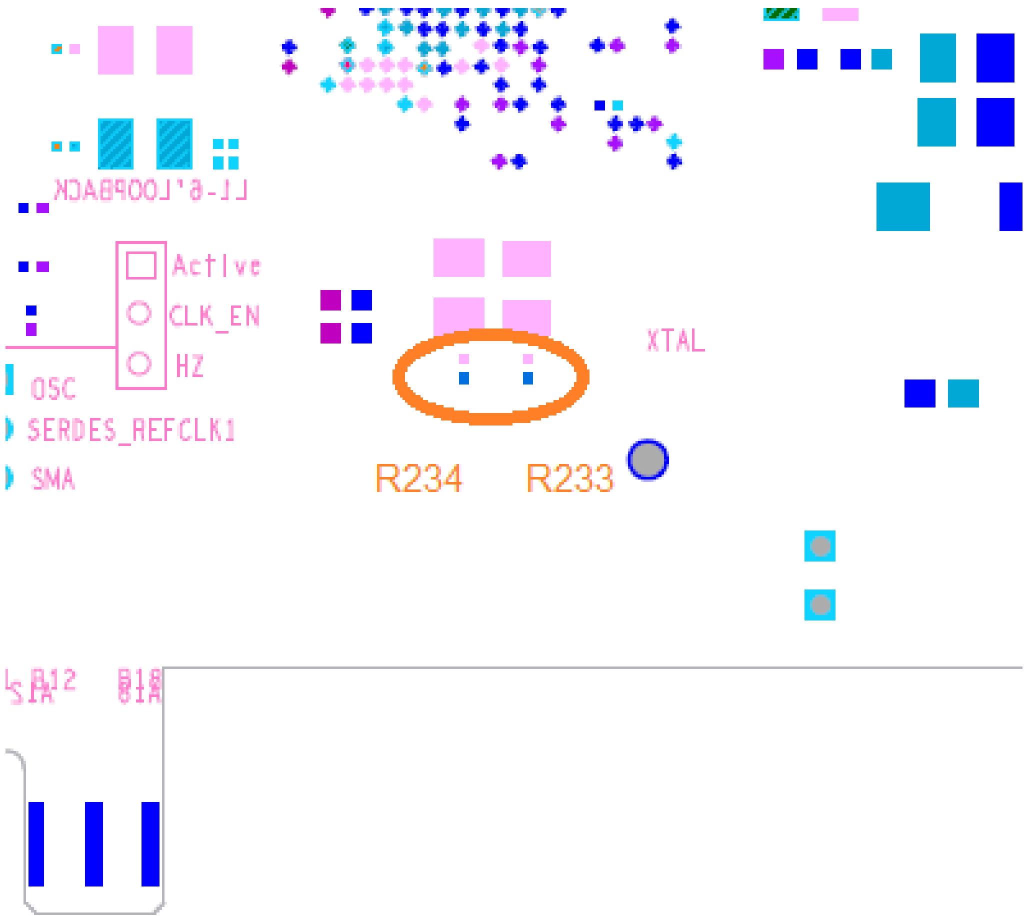

Figure 9 **• Bottom Side Location of Series Resistors for SERDES_VDDAPLL Power Supply (R233 and R234)**

Method D

SPLL

The SPLL is used by the SERDESIF to achieve interface timing for the PCIe and XAUI modes. This PLL is only powered in these two modes.

An in-series resistor is on the board and can be used to measure power-to-power supplies dedicated to the SPLL. The SPLL is only used for PCIe or XAUI protocol support. It is not used for EPCS modes.

Measure the voltage across the respective 50-ohm series resistor (R221) and convert the voltage measured across resistor to power, use the following equation:

$$\text{SPLL Power (mW)} = (\text{Voltage measured in milli Volts}/50) * 3.3$$

EQ 4

Refer to Figure 6 on page 8 for measuring across sense resistor.

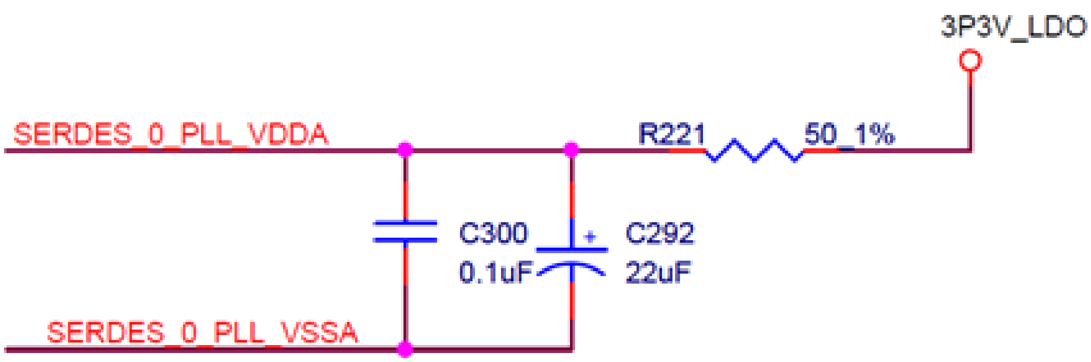

Figure 10 **• SPLL Power Supply Connection**

As shown in Figure 10, R221 is located on the bottom side of the board.

In the layout plot as shown in Figure 11, R221 can be probed with the DVM to measure the voltage across it.

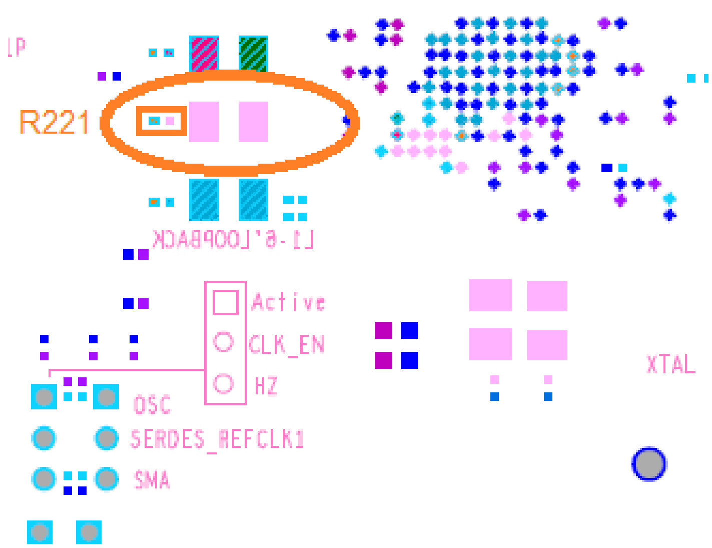

Figure 11 **• Bottom Side Location of Series Resistor for SPLL Power Supply (R221)**

Method E

FPLL

In-series resistors are on the board and can be used to measure power to power supplies dedicated to the FPLLs. FPLLs have several dedicated power supply connections and require the user to find the correct supply connection for the targeted FPLL.

Measure the voltage across the respective 100-ohm series resistor and convert the voltage measured across resistor to power, use the following equation:

FPLL Power (mW) = (Voltage measured in milli Volta/100) * 3.3

EQ 5

Refer to Figure 6 on page 8 for measuring across sense resistor.

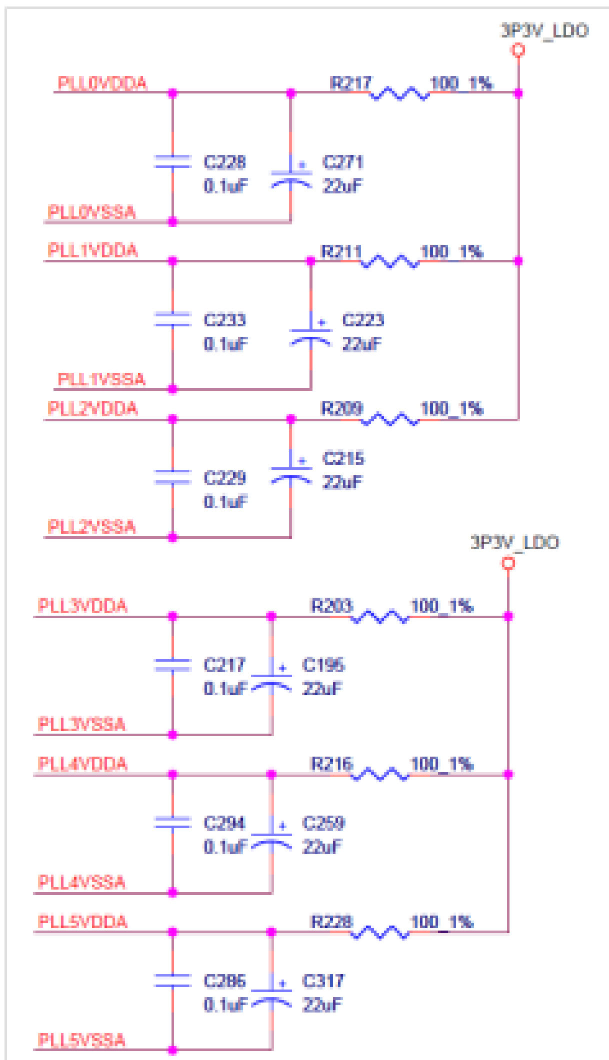

***Figure 12* • FPLL Power Supply Connections**

As shown in the Figure 12, the series resistors for the FPLL power supplies can be located on the bottom side of the board.

As shown in the layout plot Figure 13, the series resistors for the FPLL power supplies can be probed with the DVM to measure the voltage across them.

Figure 13 • **Bottom Side Location of Series Resistor for FPLL Power Supplies**

Method Summary

The steps above have been provided to correctly measure and understand the power distribution on the IGLOO2 Evaluation Kit. The Table 3 highlights the measurement method used for specific device power supplies for the IGLOO2 Evaluation Board.

Table 3 **• Measurement Method per Power Supply**

Power Supply	Measurement Method
Core VCC	A
Standby Power	B
EPCS SERDES Power	A, C
PCIE & XAUI Power	A, C, D
FPLL	E

Conclusion

Power is a key advantage of the IGLOO2 family of devices. A general understanding of how to measure and verify design results on standard hardware allows for early adoption and acceptance of the device. The power estimation tool is a very good way to obtain an estimate. However, actual measured results provide confidence and the results can be extended to investigate and reduce the power consumption on the user's system.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 2 (May 2014)	Added Figure 4 which was missing (SAR 56942).	6
Revision 1 (January 2014)	Initial release.	NA

Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.

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