Radiation Characterization & Mitigation Techniques

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Agenda

- RT ProASIC3 FPGAs Overview
- Total Ionizing Dose (TID) Effects in Flash FPGAs
- Temperature Effects in Flash FPGAs
- TID Experiments in High Temperature
- Summary
RT ProASIC3 FPGAs Overview

- 130-nm Flash Technology from UMC
- Reprogrammable
- Retain configuration in heavy ion radiation, unlike SRAM FPGAs
- Up to 75,264 VersaTiles
- Flexible core power supply 1.2 to 1.5 V
- Ultra low power in Flash*Freeze mode
- Qualified to MIL-STD-883B
- QML-Q qualification planned for 2014

Any 3-Input Combinatorial Function

D Flip-Flop With Enable and Set or Reset

## RT ProASIC3 Resources

<table>
<thead>
<tr>
<th></th>
<th>RT3PE600L</th>
<th>RT3PE3000L</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Gates</td>
<td>600K</td>
<td>3M</td>
</tr>
<tr>
<td>Tiles</td>
<td>13,824</td>
<td>75,264</td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>108K</td>
<td>504K</td>
</tr>
<tr>
<td>Flash (ROM) bits</td>
<td>1K</td>
<td>1K</td>
</tr>
<tr>
<td>PLLs</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Globals</td>
<td>18</td>
<td>18</td>
</tr>
<tr>
<td>Maximum IO</td>
<td>270</td>
<td>620</td>
</tr>
<tr>
<td>Packages (Availability)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CQFP</td>
<td>256 (NOW)</td>
<td>256 (NOW)</td>
</tr>
<tr>
<td>CCGA/LGA</td>
<td>484 (NOW)</td>
<td>484 (NOW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>896 (NOW)</td>
</tr>
<tr>
<td>STATUS</td>
<td>Mil Std 883 Class B Qualification Complete</td>
<td></td>
</tr>
</tbody>
</table>

- Prototype with low-cost commercial ProASIC3 devices today
  - Identical silicon, identical timing
    - Plastic FG484 and FG896 match Ceramic CG484 and CG896 footprint
    - RT-PROTO versions are available NOW

Flash Transistor Overview

- Floating gate holds switch transistor in “on” or “off” state
- Switch transistor connects routing tracks and logic modules
- Charge on floating gate controls $V_T$ of switch transistor
- Sense transistor allows programming and monitoring of charge on floating gate
Post-Irradiation $V_T$ Shift in MOS

- Historical data shows that $V_T$ shift recovers with room temp annealing
- Microsemi experiments are intended to show the effects of high temperature exposure during irradiation on $V_T$ shift

![Graph showing the time dependence of the room temperature annealing of $\Delta V_{mg}$ in three oxide layers with different oxide processing. The solid curves are tunneling model fits to the data for “hard” and “soft” samples from Texas Instruments Corp. (TI) and a “soft” sample from Sandia National Laboratories (SNL). (From Oldham et al. [145], © 1986 IEEE. Reprinted with permission.)](image-url)
TID Effects in Flash FPGAs

Only Flash Cells and Configuration Circuitry Affected by TID
TID Effects in Flash FPGAs (cont.)

- TID only affects Flash cells and configuration circuitry
  - TID affects the amount of charge deposited on the floating gate of the Flash cells, resulting in transistor threshold voltage ($V_T$) shift
  - $V_T$ shift of High Voltage (HV) pass transistors degrades propagation delay
    - HV pass transistors are used to implement connection between logic modules and routing tracks
    - These transistors have large $V_T$ shift because of thick oxide to pass high voltages during programming

\[ \Rightarrow \text{TID degrades propagation delay through the pass transistors} \]

- TID does not affect the embedded Flash ROM (FROM) as there is no passing of logic levels in the FROM
  - FROM only switches states between logic 0 and 1

- TID does not affect SRAM, PLL, I/O and I/O bank
Temperature Effects in Flash FPGAs

- Temperature affects Flash data retention
  - Data retention is limited by leakage current through the oxide
    - Higher temperature causes higher leakage
  - Leakage can flip a programmed cell to an erased cell causing verify errors
  - Leakage can also cause tail bits – cells which erase faster than normal cells causing verify errors

<table>
<thead>
<tr>
<th>Tj (°C)</th>
<th>HTR Lifetime (yrs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>102.7</td>
</tr>
<tr>
<td>85</td>
<td>43.8</td>
</tr>
<tr>
<td>100</td>
<td>20.0</td>
</tr>
<tr>
<td>105</td>
<td>15.6</td>
</tr>
<tr>
<td>110</td>
<td>12.3</td>
</tr>
<tr>
<td>115</td>
<td>9.7</td>
</tr>
<tr>
<td>120</td>
<td>7.7</td>
</tr>
<tr>
<td>125</td>
<td>6.2</td>
</tr>
<tr>
<td>130</td>
<td>5.0</td>
</tr>
<tr>
<td>135</td>
<td>4.0</td>
</tr>
<tr>
<td>140</td>
<td>3.3</td>
</tr>
<tr>
<td>145</td>
<td>2.7</td>
</tr>
<tr>
<td>150</td>
<td>2.2</td>
</tr>
</tbody>
</table>

RT ProASIC3 High-Temperature Data Retention (HTR) Lifetime
TID Experiments in High Temperature

- **Experiment Goals**
  - Show reliability of Flash cells under TID and other stressful factors of space environments such as high temperature
  - Collecting more life test data on RT ProASIC3 FPGAs

- **Experiment Setup**
  - Used Gamma ray chamber with one step irradiation to 30 Krad, up to 60 Krad
  - Measured every Flash cell’s $V_T$ before and after irradiation
    - $V_T$ is defined at 20 µA
  - Collected data until after 1000 device hours
Experiment Results

- **Test conditions**

RT3PE3000L TID + High Temp Retention

<table>
<thead>
<tr>
<th>Thermal</th>
<th>Electrical</th>
<th>Sample Size</th>
<th>Status</th>
<th>TID Dose</th>
<th>Reference</th>
<th>Fab lot#</th>
<th>Package</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>150°C</td>
<td>Unbiased</td>
<td>6</td>
<td>1000h done</td>
<td>30 Krads</td>
<td>HTS data</td>
<td>QHR8G</td>
<td>CG896</td>
<td>2nd lot test</td>
</tr>
<tr>
<td>125°C</td>
<td>Unbiased</td>
<td>4</td>
<td>500h done</td>
<td>0~60 Krads</td>
<td>-</td>
<td>QJA2G</td>
<td>CG484</td>
<td>1st lot test dose varied</td>
</tr>
<tr>
<td>125°C</td>
<td>Biased</td>
<td>3</td>
<td>500h done</td>
<td>30~50 Krads</td>
<td>HTOL data</td>
<td>QJA2G</td>
<td>CG484</td>
<td>1st lot test dose varied</td>
</tr>
</tbody>
</table>

- **Results**
  - No tail bits observed in unbiased condition for 1000 hours
  - No tail bits observed in biased or un-biased condition for 500 hours
  - No tail bits on control samples which were exposed to high temperature but not irradiated
Results for Unbiased Condition at 150°C

- Devices exposed to 30Krad unbiased had very slight shift in $V_T$ after 1680 hours at 150°C

RT3PE3000L-CG896 Vt Distribution
Unbiased at 150C after TID 30krads QHR8G #5365

Results for Biased Condition at 125°C

- Devices exposed to 30Krad biased had very slight shift in $V_T$ after 500 hours at 125°C

![Graph showing cumulative probability and distribution of $V_T$ at various times and conditions.](image-url)
Results for Unbiased Condition at 125°C

- Devices exposed to 30Krad unbiased had very slight shift in $V_T$ after 500 hours at 125°C
Results for Unbiased at 125°C (Not Irradiated)

- Devices with no TID had no $V_T$ shift after 500 hours at 125°C
Summary

- RT ProASIC3 FPGAs have been tested extensively for TID and High Temperature Effects
  - The longest runners went through 1680 device hours at 150 C
- Irradiated devices had slow $V_T$ shift and small impact on Flash cell data retention
- Devices, which were not irradiated, had no $V_T$ shift and no impact on Flash cell data retention
- No tail bits, thus no defects, were observed
- Proven reliability of Microsemi Flash FPGAs under TID and high temperature
- Microsemi continues investing in the product family and collecting more life test data
Thank You