IGLOO2 FPGA DSP FIR Filter -
Libero SoC v11.7

DG0504 Demo Guide
## Contents

1 Preface ................................................................. 5  
  1.1 Purpose ............................................................ 5  
  1.2 Intended Audience ................................................ 5  
  1.3 References ........................................................ 5  

2 IGLOO2 FPGA DSP FIR Filter ........................................ 6  
  2.1 Introduction ....................................................... 6  
  2.2 Design Requirements ............................................. 7  
  2.3 Demo Design ....................................................... 7  
    2.3.1 Introduction .................................................... 7  
    2.3.2 Demo Design Description .................................... 8  
       2.3.2.1 Data Handle .............................................. 8  
       2.3.2.2 Filter Control .......................................... 8  
       2.3.2.3 TPSRAM IP ............................................... 9  
       2.3.2.4 CoreUART ............................................... 9  
       2.3.2.5 CoreFIR .................................................. 9  
       2.3.2.6 CoreFFT .................................................. 9  
       2.3.2.7 SYSRESET ............................................... 10  
       2.3.2.8 OSC ..................................................... 10  
       2.3.2.9 CCC ..................................................... 10  
  2.4 Setting Up the Demo Design .................................... 10  
  2.5 Programming the Demo Design .................................. 14  
    2.5.1 Setting Up the Device ...................................... 14  
    2.5.2 Programming the Device ................................... 14  
    2.5.3 DSP FIR Demo GUI .......................................... 16  
  2.6 Running the Demo Design ....................................... 17  
  2.7 Conclusion ....................................................... 29  

3 Appendix: SmartDesign Implementation ............................. 30  

4 Appendix: Resource Usage Summary ................................ 31  

5 Appendix: Coefficient Text File Format ............................ 32  

6 Revision History ................................................... 33  

7 Product Support ..................................................... 34  
  7.1 Customer Service ................................................ 34  
  7.2 Customer Technical Support Center ................................ 34  
  7.3 Technical Support ................................................ 34  
  7.4 Website ............................................................ 34  
  7.5 Contacting the Customer Technical Support Center ........... 34  
    7.5.1 Email ....................................................... 34  
    7.5.2 My Cases ................................................... 34  
    7.5.3 Outside the U.S. ............................................ 35  
  7.6 ITAR Technical Support .......................................... 35  

Revision 6
# Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1</td>
<td>Top-Level Diagram of DSP FIR Filter Demo</td>
<td>6</td>
</tr>
<tr>
<td>Figure 2</td>
<td>Demo Design Files Top-Level Structure</td>
<td>7</td>
</tr>
<tr>
<td>Figure 3</td>
<td>DSP FIR Filter Demo Design Block Diagram</td>
<td>8</td>
</tr>
<tr>
<td>Figure 4</td>
<td>IGLOO2 Evaluation Kit DSP FIR Filter Demo Setup</td>
<td>11</td>
</tr>
<tr>
<td>Figure 5</td>
<td>USB to UART Bridge Drivers</td>
<td>12</td>
</tr>
<tr>
<td>Figure 6</td>
<td>FlashPro - New Project</td>
<td>13</td>
</tr>
<tr>
<td>Figure 7</td>
<td>FlashPro Project Configuration</td>
<td>14</td>
</tr>
<tr>
<td>Figure 8</td>
<td>FlashPro Project RUN Passed</td>
<td>15</td>
</tr>
<tr>
<td>Figure 9</td>
<td>DSP FIR Demo Window</td>
<td>16</td>
</tr>
<tr>
<td>Figure 10</td>
<td>Serial Port Configuration</td>
<td>17</td>
</tr>
<tr>
<td>Figure 11</td>
<td>Filter Generation - 1</td>
<td>18</td>
</tr>
<tr>
<td>Figure 12</td>
<td>Filter Generation - 2</td>
<td>19</td>
</tr>
<tr>
<td>Figure 13</td>
<td>Filter Response and Filter Coefficient Plot</td>
<td>20</td>
</tr>
<tr>
<td>Figure 14</td>
<td>Signal Generation</td>
<td>21</td>
</tr>
<tr>
<td>Figure 15</td>
<td>Input Signal and Input Signal FFT Plot</td>
<td>22</td>
</tr>
<tr>
<td>Figure 16</td>
<td>DSP FIR Filter Demo - Start</td>
<td>23</td>
</tr>
<tr>
<td>Figure 17</td>
<td>Filtered Signal: Time and Frequency Plot</td>
<td>24</td>
</tr>
<tr>
<td>Figure 18</td>
<td>Filtered Signal: GUI Options</td>
<td>25</td>
</tr>
<tr>
<td>Figure 19</td>
<td>Text Viewer</td>
<td>26</td>
</tr>
<tr>
<td>Figure 20</td>
<td>Text Viewer: Filter Coefficient Values</td>
<td>27</td>
</tr>
<tr>
<td>Figure 21</td>
<td>Text Viewer: Coefficients Save Options</td>
<td>28</td>
</tr>
<tr>
<td>Figure 22</td>
<td>FIR Filter Demo: Exit</td>
<td>29</td>
</tr>
<tr>
<td>Figure 23</td>
<td>DSP FIR Filter SmartDesign</td>
<td>30</td>
</tr>
<tr>
<td>Figure 24</td>
<td>Coefficient File Example – 9 Taps, Decimal Values</td>
<td>32</td>
</tr>
</tbody>
</table>
Tables

Table 1. Design Requirements .............................................................. 7
Table 2. TPSRAM Configuration for Data Buffers .................................... 9
Table 3. IGLOO2 FPGA Evaluation Kit Jumper Settings .............................. 10
Table 4. DSP FIR Filter Demo SmartDesign Blocks and Description ............... 30
Table 5. DSP FIR Filter Demo Resource Usage Summary ............................ 31
Table 6. MACC Blocks Usage Summary .................................................. 31
Table 7. RAM1Kx18 Blocks Usage Summary ............................................ 31
1  Preface

1.1  Purpose

This demo is for IGLOO®2 field programmable gate array (FPGA) devices. It provides instructions on how to use the corresponding reference design.

1.2  Intended Audience

This demo guide is intended for:

• FPGA designers
• System-level designers

1.3  References

The following documents are referred in this demo guide:

• UG0451: IGLOO2 FPGA and SmartFusion2 SoC FPGA Programming User Guide
• UG0450: SmartFusion2 SoC FPGA and IGLOO2 FPGA System Controller User Guide
• UG0448: IGLOO2 FPGA High Performance Memory Subsystem User Guide

Refer to the following web page for a complete and up-to-date listing of IGLOO2 device documentation: http://www.microsemi.com/products/fpga-soc/fpga/igloo2docs.
2.1 Introduction

The IGLOO2 FPGA devices integrate a fourth generation flash-based FPGA fabric architecture, which includes embedded mathblocks optimized specifically for digital signal processing (DSP) applications such as, finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) functions.

This demo shows a DSP FIR filter application using the IGLOO2 device. In this DSP FIR filter application, the host interface and the FIR filter are implemented in the fabric for low-pass, high-pass, band-pass, and band-reject filtering operations. A user-friendly graphical user interface (GUI) generates the filter coefficients, input signals (pass-band frequency and stop-band frequency), and also plots the input or output waveforms, and the required spectrum. Microsemi CoreFIR filter IP is used to suppress the unwanted frequency components, and CoreFFT IP is used to generate the output spectrum to verify the filtering operation.

Figure 1 shows the top-level diagram for the DSP FIR filter demo.

**Figure 1** • Top-Level Diagram of DSP FIR Filter Demo
2.2 Design Requirements

Table 1 lists the hardware and software requirements.

Table 1 • Design Requirements

<table>
<thead>
<tr>
<th>Design Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hardware Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>IGLOO2 Evaluation Kit:</td>
<td></td>
</tr>
<tr>
<td>• FlashPro4 programmer</td>
<td>Rev C or later</td>
</tr>
<tr>
<td>• USB A to Mini-B cable</td>
<td></td>
</tr>
<tr>
<td>Host PC or Laptop</td>
<td>Windows 7 64-bit Operating System</td>
</tr>
<tr>
<td><strong>Software Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>Libero® system-on-chip (SoC)</td>
<td>v11.7</td>
</tr>
<tr>
<td>FlashPro Programming Software</td>
<td>v11.7</td>
</tr>
<tr>
<td>Host PC Drivers</td>
<td>USB to UART drivers</td>
</tr>
<tr>
<td>Framework</td>
<td>Microsoft .NET Framework 4 Client for launching demo GUI</td>
</tr>
</tbody>
</table>

2.3 Demo Design

2.3.1 Introduction

The design files are available for download from the following path in the Microsemi website:

http://soc.microsemi.com/download/rsc/?f=m2gl_dg0504_dsp_fir_filter_liberov11p7_df

The design files include:

• Design Files
• GUI
• Programming file
• Readme.txt file

Figure 2 shows the top-level structure of the design files. Refer to the Readme.txt file provided in the demo file folder for the complete directory structure.

Figure 2 • Demo Design Files Top-Level Structure

```
<download_folder>
  IGL2_FIR_FILTER_DF
    DesignFiles
    GUI
    ProgrammingFiles
    Readme.txt
```
2.3.2 Demo Design Description

This demo design uses the following blocks:

- Data Handle (user RTL)
- Filter Control (user RTL)
- TPSRAM IP (IPcore)
- CoreUART (IPcore)
- CoreFIR (IPcore)
- CoreFFT (IPcore)
- SYSRESET (IPcore)
- OSC (IPcore)
- CCC (IPcore)

Figure 3 shows the detailed block diagram of the demo design.

**Figure 3 • DSP FIR Filter Demo Design Block Diagram**

2.3.2.1 Data Handle

Data handle consists of the Core UART IP and the UART interface finite state machine handling the control operations between the host PC (GUI interface) and the fabric logic. Control operations include the loading of filter coefficients, filter input data to the corresponding input data buffer, coefficient buffers, and send and receive data from the Host PC GUI.

2.3.2.2 Filter Control

Controls the FIR filter and the FFT operations. It loads the filtered data to the corresponding output buffer and moves the FFT output data to the corresponding output data buffer.
2.3.2.3 TPSRAM IP

TPSRAM IP uses the following configurations:

- Filter coefficient buffer
- Input signal data buffer
- Output signal buffer
- Output signal FFT real data buffer
- Output signal FFT imaginary data buffer

Table 2 • TPSRAM Configuration for Data Buffers

<table>
<thead>
<tr>
<th>Buffer</th>
<th>Write Port</th>
<th>Read Port</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Depth</td>
<td>Width</td>
</tr>
<tr>
<td>Filter Coefficients</td>
<td>64</td>
<td>8</td>
</tr>
<tr>
<td>FIR Input Signal</td>
<td>2048</td>
<td>8</td>
</tr>
<tr>
<td>FIR Output Signal</td>
<td>1024</td>
<td>16</td>
</tr>
<tr>
<td>FFT Output Real Signal</td>
<td>256</td>
<td>16</td>
</tr>
<tr>
<td>FFT Output Imaginary Signal</td>
<td>256</td>
<td>16</td>
</tr>
</tbody>
</table>

2.3.2.4 CoreUART

The Core UART IP is used to transfer the data between the host PC (GUI) and IGLOO2. The Core UART configuration is as follows:

- Version: 5.5.101
- TxFIFO: Disable TxFIFO
- RxFIFO: Disable RxFIFO
- RxLegacyMode: Disable
- Baud rate: 115200
- Number of bits: 8
- Stop bits: 1
- Parity: None

2.3.2.5 CoreFIR

The Core FIR IP is used in the Reloadable coefficient mode to support Low-pass, High-pass, Band-pass, and Band-reject filters. The Core FIR IP configuration is as follows:

- Version: 8.6.101
- Filter Type: Single rate fully enumerated
- Number of Taps: 31
- Coefficients Type: Reloadable
- Coefficients Bit Width: 16 (signed)
- Data Bit Width: 16 (signed)
- Filter Structure: Transposed with symmetry

2.3.2.6 CoreFFT

The Core FFT IP is used for generating the frequency spectrum of the filtered data. Core FFT IP configuration is as follows:

- Version: 6.4.105
- FFT Architecture: In place
- FFT Type: Forward
- FFT Scaling: Conditional
- FFT Transform Size: 256
- Width: 16
2.3.2.7 SYSRESET
The SYSRESET IP provides the power on reset signal.

2.3.2.8 OSC
The OSC IP is configured as an RC oscillator to provide the 50 MHz signal to the clock conditioning circuit (CCC).

2.3.2.9 CCC
The CCC IP is configured to provide a 150 MHz clock signal. For detailed smart design implementation and resource usage summary, refer to "Appendix: SmartDesign Implementation" on page 30.

2.4 Setting Up the Demo Design
The following steps describe how to setup the hardware demo:

1. Connect the jumpers on the IGLOO2 Evaluation Kit board, as shown in Table 3.

Table 3 • IGLOO2 FPGA Evaluation Kit Jumper Settings

<table>
<thead>
<tr>
<th>Jumper</th>
<th>Pin (From)</th>
<th>Pin (To)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>J22</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J23</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J24</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J8</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
<tr>
<td>J3</td>
<td>1</td>
<td>2</td>
<td>Default</td>
</tr>
</tbody>
</table>

CAUTION: While making the jumper connections, the power supply switch SW7 must be switched OFF.

2. Connect the Power supply to the J6 connector, switch ON the power supply switch, SW7.
3. Connect the FlashPro4 programmer to the J5 connector of the IGLOO2 Evaluation Kit board.
4. Connect the host PC USB port to the J18 USB connector on the IGLOO2 Evaluation Kit board using the USB Mini-B cable.
Figure 4 shows the board setup for running the DSP FIR Filter demo on the IGLOO2 Evaluation Kit.

Figure 4 • IGLOO2 Evaluation Kit DSP FIR Filter Demo Setup
5. Ensure that the USB to UART bridge drivers are automatically detected. This can be verified in the Device Manager of the host PC. The FTDI USB to UART converter enumerates four COM ports. For USB 2.0, note down the USB Serial Converter D COM port number to use it in the IGL2_FIR_Filter.exe. Figure 5 shows the USB 2.0 Serial port properties and the connected COM10 and USB Serial Converter D.

*Figure 5 • USB to UART Bridge Drivers*

6. If the USB to UART bridge drivers are not installed, download and install the drivers from www.microsemi.com/documents/CDM_2.08.24_WHQL_Certified.zip.
2.5 Programming the Demo Design

The following steps describe how to program the demo design:

1. Download the demo design from: http://soc.microsemi.com/download/rsc/?f=m2gl_dg0504_dsp_fir_filter_liberov11p7_df
2. Switch ON the power supply switch, SW7.
3. Launch the FlashPro software.
4. Click New Project.
5. In the New Project window, enter the project name as IGL2_FIR_FILTER.

Figure 6 • FlashPro - New Project

6. Click Browse and navigate to the location where you want to save the project.
7. Select Single device as the Programming mode.
8. Click OK to save the project.
2.5.1 Setting Up the Device

The following steps describe how to configure the device:

1. Click **Configure Device** on the FlashPro GUI.
2. Click **Browse** and navigate to the location where the `IGL2_FIR_FILTER.stp` file is located and select the file. The default location of the programming file is: `<download_folder>/VGL2_FIR_FILTER_DF\ProgrammingFiles\VGL2_FIR_FILTER.stp`.
3. Click **Open**. The required programming file is selected and is ready to be programmed in the device.
4. Select **Advanced** as Mode and **PROGRAM** as Action.

2.5.2 Programming the Device

*Figure 7 • FlashPro Project Configuration*
5. Click **PROGRAM** to start programming the device. Wait until **Programmer Status** is changed to **RUN PASSED**.

*Figure 8 • FlashPro Project RUN Passed*
2.5.3 DSP FIR Demo GUI

The DSP FIR demo is provided with a user-friendly GUI that runs on the host PC which communicates with the IGLOO2 Evaluation Kit. The UART is used as the underlying communication protocol between the host PC and IGLOO2 Evaluation Kit.

Figure 9 shows the DSP FIR demo GUI.

Figure 9 • DSP FIR Demo Window

The DSP FIR demo window consists of the following tabs:

- **Input Parameters**: Configures the serial COM port, filter generation, and signal generation.
- **Filter Input**: Plots the input signal and its frequency spectrum
- **Filter Output**: Plots the output signal and its frequency spectrum
- **Text Viewer**: Shows the coefficients, input signal, output signal, and FFT data values

Click Help for more information on the GUI.
2.6 Running the Demo Design

The following steps describe how to run the demo design:

1. Launch the DSP FIR Demo GUI executable file available in the design files. 
   (`IGL2_FIR_FILTER_DFGUI/IGL2_FIR_Filter.exe`). The FIR Filter Demo window is displayed, as shown in Figure 10.

   **Figure 10** • Serial Port Configuration

   ![Serial Port Configuration](image)

2. **Serial Port Configuration**: The COM port number is automatically detected and the baud rate is fixed at 115200. Click **Connect**. Refer to Figure 10.
3. **Filter Generation:** Two options are provided for generating the filter coefficients:
   - Generate the coefficients using MATLAB or any similar tool and save it as a text file (Refer to "Appendix: Coefficient Text File Format" on page 32 for the format of the text file). The GUI can be used to browse and load this file. Refer to Figure 11.

*Figure 11 • Filter Generation - 1*
• Generate the Filter coefficients using the GUI. The following parameters are required to generate filter coefficients:
  • **Filter Type**: Low-pass (Low-pass/High-pass/Band-pass/Band-reject filter)
  • **Filter Window**: Blackman (Blackman/Hamming window)
  • **Low Cut-off Frequency**: Disabled for Low-pass filter required (high cut-off frequency is disabled for high-pass filter)
  • **High Cut-off Frequency**: 20 MHz
  • **Filter Taps**: 31 (Fixed)
    Press Generate Filter to generate the filter coefficients.

*Figure 12• Filter Generation - 2*
4. The successful after-generation graphs of the filter coefficients, filter response, and the filter coefficient plots, are displayed. Refer to Figure 13.

*Figure 13*  Filter Response and Filter Coefficient Plot
The following parameters are required to generate Signal Generation:

- **Sampling Frequency**: 150 MHz (Fixed)
- **Number of Samples**: 1024 (Fixed)
- **Input Frequency 1**: Enter the signal frequency in the Pass-band region. For example, 1 MHz to High cut-off frequency
- **Input Frequency 2**: Enter the signal frequency in the Stop-band region. For example, High cut-off frequency to Sampling frequency/2

5. Click **Generate Signal**, as shown in **Figure 14**.

**Figure 14** • Signal Generation
6. Input signal and frequency spectrum of the specified signal are displayed, as shown in Figure 15.

*Figure 15* • Input Signal and Input Signal FFT Plot
7. To configure the input frequencies and coefficients, click **Start**, as shown in Figure 16. It sends the input data (1K samples) and filter coefficients to the IGLOO2 device for processing the filtering operation.

*Figure 16 • DSP FIR Filter Demo - Start*
After completing the filter operation by the IGLOO2 device, the GUI plots the filtered data and the FFT data on the filter output window, as shown in Figure 17. Since Low-pass filter option was selected, the High frequency component is suppressed while the Low frequency signal is preserved. This can be observed in the frequency spectrum of the output signal.

Figure 17 • Filtered Signal: Time and Frequency Plot
8. Right-click on the window, it shows different options, as shown in Figure 18. The data can be copied, saved, and exported to the CSV plot for analysis purpose. Page setup, print, show point values, zoom, and set scale are set to default.

*Figure 18 • Filtered Signal: GUI Options*
9. The filter coefficients, input signal, output signal, and FFT output data values can be viewed in the Text viewer. Click Text Viewer and click the corresponding View, as shown in Figure 19.

Figure 19 • Text Viewer
The values can be observed, as shown in Figure 20.

Figure 20 • Text Viewer: Filter Coefficient Values
10. To save the coefficients as a text file, right-click Filter Coefficients window, it shows different options, as shown in Figure 21. Click Save and select OK to save the text file.

*Figure 21 • Text Viewer: Coefficients Save Options*
11. Click Exit to stop the demo, as shown in Figure 22.

*Figure 22 • FIR Filter Demo: Exit*

### 2.7 Conclusion

This demo shows the features of the IGLOO2 device including mathblocks and LSRAMS for DSP specific applications. Also provides information about how to use the Microsemi DSP IP cores (CoreFIR, and CoreFFT). This FIR Filter GUI-based demo is very easy to use and provides several options to understand and implement the DSP filters on the IGLOO2 device.
Appendix: SmartDesign Implementation

DSP FIR filter SmartDesign is shown in Figure 23.

*Figure 23 • DSP FIR Filter SmartDesign*

Table 4 shows SmartDesign blocks in DSP FIR Filter.

*Table 4 • DSP FIR Filter Demo SmartDesign Blocks and Description*

<table>
<thead>
<tr>
<th>S.No</th>
<th>Block Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DATA_HANDLE_0</td>
<td>Handles the communication between the host PC and the IGLOO2 Evaluation Kit board.</td>
</tr>
<tr>
<td>2</td>
<td>FILTERCONTROL_FSM_0</td>
<td>Control logic to generate the control signals for the FIR and FFT operations.</td>
</tr>
<tr>
<td>3</td>
<td>Coef_Buff</td>
<td>IP for the filter coefficient buffer.</td>
</tr>
<tr>
<td>4</td>
<td>FIR_IN_Buff</td>
<td>IP for the FIR input signal data buffer.</td>
</tr>
<tr>
<td></td>
<td>FIR_Out_Buff</td>
<td>IP for the FIR output signal buffer.</td>
</tr>
<tr>
<td></td>
<td>FFT_Re_Buff</td>
<td>IP for the FFT output imaginary data buffer.</td>
</tr>
<tr>
<td></td>
<td>FFT_Im_Buff</td>
<td>IP for the FFT output real data buffer.</td>
</tr>
<tr>
<td>5</td>
<td>COREFIR_0</td>
<td>COREFIR IP</td>
</tr>
<tr>
<td>6</td>
<td>COREFFT_0</td>
<td>COREFFT IP</td>
</tr>
<tr>
<td>7</td>
<td>SYSRESET_0</td>
<td>Reset IP</td>
</tr>
<tr>
<td>8</td>
<td>OSC_0</td>
<td>Oscillator IP</td>
</tr>
<tr>
<td>9</td>
<td>FCCC_0</td>
<td>Clock Conditioning circuit IP</td>
</tr>
</tbody>
</table>
Table 5 shows DSP FIR filter resource usage summary.

**Device**: IGLOO2 device

**Die**: M2GL010

**Package**: 484 FBGA

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>2867</td>
<td>12084</td>
<td>23.73</td>
</tr>
<tr>
<td>DFF</td>
<td>3747</td>
<td>12084</td>
<td>31.01</td>
</tr>
<tr>
<td>RAM64x18</td>
<td>0</td>
<td>22</td>
<td>0.00</td>
</tr>
<tr>
<td>RAM1Kx18</td>
<td>12</td>
<td>21</td>
<td>57.14</td>
</tr>
<tr>
<td>MACC</td>
<td>20</td>
<td>22</td>
<td>90.91</td>
</tr>
</tbody>
</table>

Table 6 shows MACC blocks usage summary.

<table>
<thead>
<tr>
<th>CoreFIR</th>
<th>CoreFFT</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>04</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 7 shows RAM1Kx18 blocks usage summary.

<table>
<thead>
<tr>
<th>CoreFIR</th>
<th>CoreFFT</th>
<th>Fabric Buffers</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>7</td>
<td>5</td>
<td>12</td>
</tr>
</tbody>
</table>
The FIR filter coefficients can be loaded from an ASCII text file (*.txt). Create the coefficient file using a text editor. The format of the text file must be, as shown in Figure 24. The coefficient values must be entered as integer numbers. For a symmetric or anti-symmetric filter, only half of the coefficients must be listed in the file (this applies to the fully enumerated type only). Only one coefficient value per line is permitted. An extra empty line must be placed after the last coefficient of the last set.

*Figure 24*  Coefficient File Example – 9 Taps, Decimal Values

```
coefficient_set_1
5
6
10
25
63
-1
-11
-32
-63
```
## Revision History

The following table shows important changes made in this document for each revision.

<table>
<thead>
<tr>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 6</td>
<td>Updated the document for Libero v11.7 software release (SAR 78044).</td>
</tr>
<tr>
<td>(April 2016)</td>
<td></td>
</tr>
<tr>
<td>Revision 5</td>
<td>Updated the document for Libero v11.6 software release (SAR 72354).</td>
</tr>
<tr>
<td>(October 2015)</td>
<td></td>
</tr>
<tr>
<td>Revision 4</td>
<td>Updated the document for Libero v11.5 software release (SAR 63927).</td>
</tr>
<tr>
<td>(January 2015)</td>
<td></td>
</tr>
<tr>
<td>Revision 3</td>
<td>Updated the document for Libero v11.4 software release (SAR 59681).</td>
</tr>
<tr>
<td>(August 2014)</td>
<td></td>
</tr>
<tr>
<td>Revision 2</td>
<td>Updated the document for Libero v11.3 software release (SAR 56265).</td>
</tr>
<tr>
<td>(June 2014)</td>
<td>Figure 3 on page 8 was updated.</td>
</tr>
<tr>
<td>Revision 1</td>
<td>Initial release</td>
</tr>
<tr>
<td>(January 2014)</td>
<td></td>
</tr>
</tbody>
</table>
Product Support

7 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

7.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

- From North America, call 800.262.1060
- From the rest of the world, call 650.318.4460
- Fax, from anywhere in the world, 408.643.6913

7.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

7.3 Technical Support


7.4 Website


7.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

7.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

7.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to My Cases.
7.5.3 **Outside the U.S.**

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit About Us for sales office listings and corporate contacts.

7.6 **ITAR Technical Support**

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select Yes in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.