AC402
Application Note
Design Migration in IGLOO2 Devices in FG484 Package

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 2.0

In revision 2.0 of this application note, published in December 2017, a note was added under Table 8, page 9 to describe the usage of VREF5 pins.

1.2 Revision 1.0

Updated the document to include M2GL090 device (SAR 54319).

1.3 Revision 0

Revision 0 was the first publication of this document.

2 Design Migration in IGLOO2 Devices in FG484 Package

This document describes how to migrate designs within the IGLOO®2 FPGA device family between the M2GL025, M2GL050, and M2GL090 devices within the FG484 package. It addresses restrictions and specifications that need to be considered when moving a design between the M2GL025, M2GL050, and M2GL090 devices. This includes pin compatibility between the devices, design and device resources evaluation, I/O banks, standards, and so on. It also describes the software flow behavior during the migration.

2.1 Design Migration

IGLOO2 family devices are architecturally compatible with each other. Key areas need more attention while migrating a design from one device to another. Following are the specific points discussed in this document:

2.1.1 Design and Device Evaluation

One of the initial tasks while migrating a design should be to compare the available resources between the two devices. The device resources can be of the following three categories:

Necessary design timing analysis and simulations should be performed while migrating designs from one device to another.

Each of the following sections focuses on the different aspects of the design and device evaluation categories.

2.1.1.1 High Performance Memory Subsystem

The following table provides a high-level summary of the differences between the M2GL025, M2GL050, and M2GL090 high performance memory subsystem (HPMS) blocks. Based on the different HPMS resources and features, migration from one device to another can be planned to avoid any resource conflicts or issues. Fabric Resources

Table 1 • **HPMS Features Per Package or Device**

	FG484 Package		
Feature	**M2GL025 and M2GL025T**	**M2GL050 and M2GL050T**	**M2GL090 and M2GL090T**
Fabric interfaces (FIC)	1 (FIC_0)	2 (FIC_0 and FIC_1)	1 (FIC_0)
Memory subsystem DDR (MDDR)	X18[1]	X18[2]	X18[1]
eNVM (K bytes)	256	256	512
eSRAM (K bytes)	64	64	64

Table 1 • **HPMS Features Per Package or Device *(continued)***

Feature	FG484 Package		
	M2GL025 and M2GL025T	**M2GL050 and M2GL050T**	**M2GL090 and M2GL090T**
eSRAM (non-SECDED) (K bytes)	80	80	80
SPI, HPDMA, PDMA	1	1	1
DDR supports x18, x16, x9, and x8 modes DDR supports x18 and x16 modes			

The following table gives a high-level summary of the differences between the M2GL025, M2GL050, and M2GL090 fabric resources. Based on the differences, effective logic count, RAM size, and number of I/Os, migration can be evaluated and planned from one device to another to avoid any resource conflicts or issues.

Table 2 • **Summary of the Fabric Features Supported Per Device**

Fabric Features (Logic, DSP, and Memory)		FG484 Package		
		M2GL025 and M2GL025T	**M2GL050 and M2GL050T**	**M2GL090 and M2GL090T**
Logic/DSP	Logic modules (4-Input LUT)	27,696	56,340	86,316
	Mathblocks	34	72	84
	PLLs and CCCs	6	6	6
Fabric memory	LSRAM 18 K blocks	31	69	109
	uSRAM 1 K blocks	34	72	112
User I/Os	MSIO (3.3 V max)	157	105	157
	MSIOD (2.5 V max)	40	40	40
	DDRIO (2.5 V max)	70	122	70
	Total user I/Os per package	267	267	267

2.1.1.2 SERDES

IGLOO2 “T” devices have up to four 5 Gbps high speed serial interfaces (SERDES) transceivers.

The high-speed serial features are same between the M2GL025T and M2GL050T devices in the FG484 package. The M2GL090T device, on the other hand, has one extra PCIe endpoint compared to the M2GL025T and M2GL050T devices as shown in the following table.

Table 3 • **High-Speed Serial Support per Device**

Feature	FG484 Package		
	M2GL025T	**M2GL050T**	**M2GL090T**
5G SERDES lanes (SERDES_IF_0)	4	4	4
PCIe endpoints	1	1	2

2.1.1.3 On-Chip Oscillators

The following table shows the summary of IGLOO2 on-chip oscillators that are the primary sources for generating free-running clocks.

Table 4 • **On-Chip Oscillator Support per Device**

	FG484 Package		
Feature	**M2GL025**	**M2GL050**	**M2GL090**
1 MHz RC oscillator	1	1	1
50 MHz RC oscillator	1	1	1
Main crystal oscillator (32 K Hz - 20 MHz)	1	1	1

See, *IGLOO2 FPGA Clocking Resources User Guide* for more information.

2.1.2 I/O Banks and Standards

IGLOO2 I/Os are partitioned into multiple I/O voltage banks. The number of banks depends upon the device. There are seven I/O banks in the M2GL025 device and eight I/O banks in the M2GL050 and M2GL090 devices. The following table shows a summary of organization of the I/O banks between M2GL025, M2GL050, and M2GL090 FPGA devices

Table 5 • **Organization of the I/O Banks in IGLOO2 Devices**

	FG484 Package		
I/O Banks	**M2GL025T**	**M2GL050T**	**M2GL090T**
Bank 0	DDRIO: MDDR or fabric	DDRIO: MDDR or fabric	-
Bank 1	MSIO: fabric	MSIO: fabric	DDRIO: MDDR or fabric
Bank 2	MSIO: HPMS or fabric	-	MSIO: MSS or fabric
Bank 3	MSIO: JTAG	MSIO: HPMS or fabric	MSIO: MSS or fabric
Bank 4	MSIO: fabric	MSIO: JTAG	MSIO: JTAG/SWD
Bank 5	MSIOD: SERDES_0 or fabric	DDRIO: fabric	MSIO: fabric
Bank 6	MSIOD: fabric	MSIOD: SERDES_0 or fabric	MSIOD: SERDES_0 or fabric
Bank 7	MSIO: fabric	MSIOD: fabric	MSIOD: fabric
Bank 8	-	MSIO: fabric	MSIO: fabric

Package pins VDDIx are the bank power supplies where x indicates the bank number. For example, VDDI0 is bank0 power supply. Figure 1, page 5, Figure 2, page 5, and Figure 3 on page 6 show the different I/O bank locations and number of locations per device in the FG484 package.

Figure 1 • **IGLOO2 M2GL025T FG484 I/O Bank Locations**

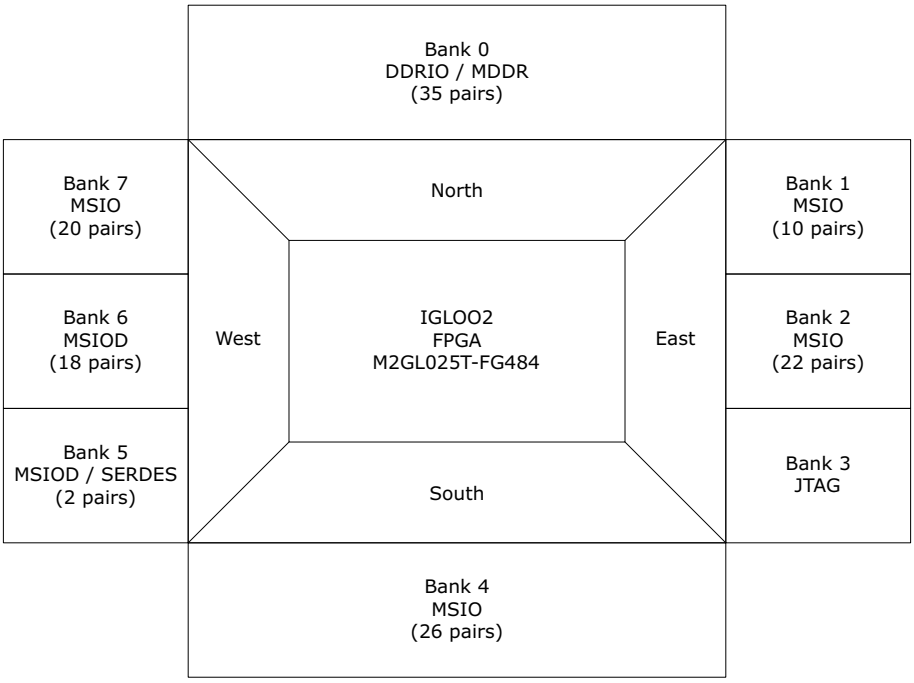


Figure 2 • **IGLOO2 M2GL050T FG484 I/O Bank Locations**

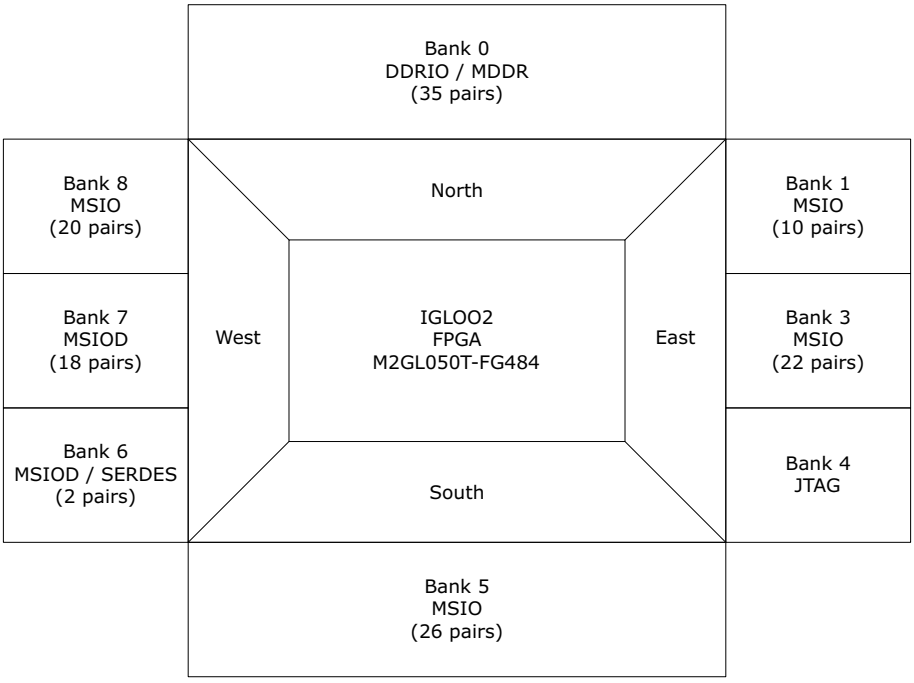
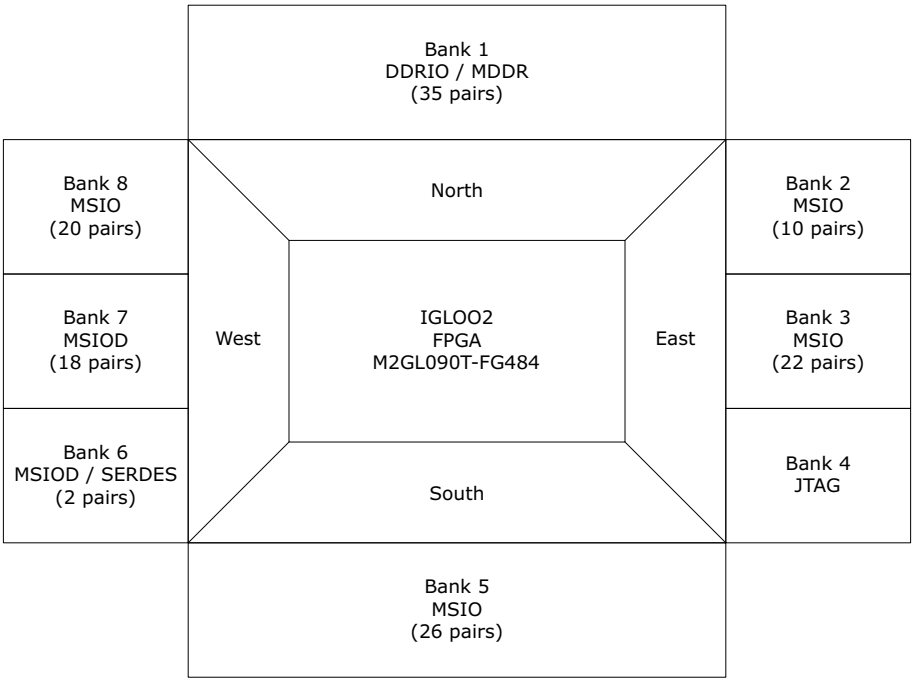


Figure 3 • **IGLOO2 M2GL090T FG484 I/O Bank Locations**



An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltage standards. MSIOD or DDRIO banks support 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltage standards. 3.3 V is not supported for MSIOD or DDRIO I/Os. For more information on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, see the “Supported Voltage Standards” table in the *IGLOO2 FPGA Fabric User Guide*.

2.1.3 Pin Migration and Compatibility

IGLOO2 devices and packaging have been designed to allow footprint compatibility for smoother migration but some of the pins have a reduced compatibility feature set between the M2GL025, M2GL050, and M2GL090 devices in the FG484 package. This section addresses the different aspects of the pin compatibility. The differences can be grouped into the following categories:

- Global Versus Regular Pins, page 6
- Available versus No Connect Pins, page 9
- I/Os Technology Compatibility Per Pin or Bank, page 9
- Even though the VDDI may be the same (for example, MSIO 2.5 V and DDRIO 2.5 V), the attributes and features supported may be different for different I/O types (MSIO versus DDRIO). See, “I/O Programmable Features” section in IGLOO2 FPGA Fabric User Guide for more information on the list of features supported per I/O type., page 12
- Probe Pins, page 12

2.1.3.1 Global Versus Regular Pins

When migrating designs between IGLOO2 devices, different types of pins that are available per device have to be evaluated. The functionality of the same pin can be different among different devices. This section focuses on highlighting and comparing the global pins in one device against the other devices. Therefore, migration can be evaluated and planned from one device to another without any resource conflicts or issues. The following are the scenarios that arise while migrating designs:

- Moving from a device where I/O is a global pin, to a device where the same I/O is a regular pin: In this case, replace the global clock (for example, CLKBUF) with a
regular input buffer (for example, INBUF) and then internally promote the signal to a global resource using a CLKINT or synthesis options.
- Moving from a device where I/O is a regular pin, to a device where the same I/O is a global pin: In this case, replace the regular input buffer (for example, INBUF) with a

global clock (for example, CLKBUF) or keep the regular input buffer (INBUF) and internally promote the signal to a global resource using a CLKINT or synthesis options.

The following table provides a comparison between the global pins available in the M2GL025, M2GL050, and M2GL090 devices. The unused global pins are configured as inputs with pull-up resistors by Libero® System-on-Chip (SoC) software.

For more information, see the “FPGA Fabric Global Network Architecture” chapter in *IGLOO2 FPGA Clocking Resources User Guide*.

Table 6 • **Non-Equivalent Global Pins Comparison Per Device**

	FG484 Package					
Package Pin	**M2GL025**	**Bank No**	**M2GL050**	**Bank No**	**M2GL090**	**Bank No**
A6	DDRIO65NB0/**GB4/CCC_NW1_CLKI2**	0	DDRIO66NB0	0	DDRIO92NB1**/GB4/CCC_NW1_CLKI2**	1
A7	DDRIO62PB0/MDDR_DQ_ECC1	0	DDRIO87PB0/**CCC_NW1_CLKI3**/MDDR_DQ_ECC1	0	DDRIO89PB1/MDDR_DQ_ECC3	1
AA11	MSIO124PB4	4	DDRIO152PB5/**GB3/CCC_SW0_CLKI3**	5	MSIO203PB5	5
AA13	MSIO130PB4/**VCCC_SE0_CLKI**	4	DDRIO162PB5	5	MSIO209PB5**/VCCC_SE0_CLKI**	5
AB11	MSIO124NB4	4	DDRIO152NB5/**GB7/CCC_SW1_CLKI2**	5	MSIO203NB5	5
AB13	MSIO129PB4/**CCC_SW1_CLKI3**	4	DDRIO161PB5/**GB11/VCCC_SE0_CLKI**	5	MSIO208PB5**/CCC_SW1_CLKI3**	5
AB15	**DDRIO**164PB5/VCCC_SE1_CLKI	5	**MSIO**134PB4/VCCC_SE1_CLKI	4	**MSIO213PB5**/VCCC_SE1_CLKI	5
B6	DDRIO65PB0/**GB0/CCC_NW0_CLKI3**	0	DDRIO66PB0	0	DDRIO92PB1**/GB0/CCC_NW0_CLKI3**	1
D9	DDRIO61PB0/**CCC_NW1_CLKI3**	0	DDRIO88PB0	0	DDRIO88PB1**/CCC_NW1_CLKI3**	1
U13	MSIO131PB4/**GB11/VCCC_SE0_CLKI**	4	DDRIO166PB5	5	MSIO210PB5**/GB11/VCCC_SE0_CLKI**	5
V11	MSIO125PB4/**GB3/CCC_SW0_CLKI3**	4	DDRIO156PB5	5	MSIO201PB5**/GB3/CCC_SW0_CLKI3**	5
W11	MSIO125NB4/**GB7/CCC_SW1_CLKI2**	4	DDRIO156NB5	5	MSIO201NB5**/GB7/CCC_SW1_CLKI2**	5
W12	MSIO128PB4	4	DDRIO159PB5/**CCC_SW1_CLKI3**	5	MSIO206PB5	5
Y14	MSIO133PB4/**GB15/VCCC_SE1_CLKI**	4	DDRIO169PB5	5	MSIO212PB5**/GB15/VCCC_SE1_CLKI**	5
Y9	MSIO120NB4/**CCC_SW0_CLKI2**	4	DDRIO148NB5/PROBE_B	5	MSIO196NB5**/CCC_SW0_CLKI2**	5

The following table shows the list of global pins that are similar for the two devices.

Table 7 • **Equivalent Global Pins Per Device**

	FG484 Pin Names					
Package Pin	**M2GL025**	**Bank No**	**M2GL050**	**Bank No**	**M2GL090**	**Bank No**
A14	DDRIO50PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0	DDRIO76PB0/GB12/CCC_NE1_CLKI2/MDDR_DQ12	0	DDRIO77PB1/GB12/CCC_NE1_CLKI2/MDDR_DQ12	1
B13	DDRIO52PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0	DDRIO78PB0/GB8/CCC_NE0_CLKI3/MDDR_DQS1	0	DDRIO79PB1/GB8/CCC_NE0_CLKI3/MDDR_DQS1	1
D12	DDRIO53PB0/CCC_NE0_CLKI2/MDDR_DQ10	0	DDRIO79PB0/CCC_NE0_CLKI2/MDDR_DQ10	0	DDRIO80PB1/MDDR_DQ10/CCC_NE0_CLKI2	1
D14	DDRIO49PB0/CCC_NE1_CLKI3/MDDR_DQ14	0	DDRIO75PB0/CCC_NE1_CLKI3/MDDR_DQ14	0	DDRIO76PB1/CCC_NE1_CLKI3/MDDR_DQ14	1
F8	DDRIO66NB0/CCC_NW0_CLKI2	0	DDRIO92NB0/CCC_NW0_CLKI2	0	DDRIO93NB1/CCC_NW0_CLKI2	1
G19	MSIO28PB1/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C	1	MSIO42PB1/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C	1	MSIO55PB2/GB14/VCCC_SE1_CLKI/MMUART_1_CLK/GPIO_25_B/USB_DATA4_C	2
G22	MSIO26PB1/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B	1	MSIO40PB1/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B	1	MSIO53PB2/CCC_NE1_CLKI1/MMUART_1_RI/GPIO_15_B	2
H1	MSIO96PB7/GB6/CCC_NW1_CLKI1	7	MSIO114PB8/GB6/CCC_NW1_CLKI1	8	MSIO156PB8/GB6/CCC_NW1_CLKI1	8
H20	MSIO27PB1/GB10/VCCC_SE0_CLKI/USB_XCLK_C	1	MSIO41PB1/GB10/VCCC_SE0_CLKI/USB_XCLK_C	1	MSIO54PB2/GB10/VCCC_SE0_CLKI/USB_XCLK_C	2
J1	MSIO98PB7/CCC_NW1_CLKI0	7	MSIO116PB8/CCC_NW1_CLKI0	8	MSIO158PB8/CCC_NW1_CLKI0	8
J20	MSIO25PB1/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B	1	MSIO39PB1/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B	1	MSIO52PB2/CCC_NE0_CLKI1/MMUART_1_CTS/GPIO_13_B	2
J22	MSIO20NB2/GB13/VCCC_SE1_CLKI/GPIO_26_A	2	MSIO20NB3/GB13/VCCC_SE1_CLKI/GPIO_26_A	3	MSIO20NB3/GB13/VCCC_SE1_CLKI/GPIO_26_A	3
J3	MSIO97PB7/GB2/CCC_NW0_CLKI1	7	MSIO115PB8/GB2/CCC_NW0_CLKI1	8	MSIO157PB8/GB2/CCC_NW0_CLKI1	8
K1	MSIOD103PB6/CCC_SW0_CLKI0	6	MSIOD121PB7/CCC_SW0_CLKI0	7	MSIOD178PB7/CCC_SW0_CLKI0	7
K22	MSIO20PB2/GB9/VCCC_SE0_CLKI/GPIO_25_A	2	MSIO20PB3/GB9/VCCC_SE0_CLKI/GPIO_25_A	3	MSIO20PB3/GB9/VCCC_SE0_CLKI/GPIO_25_A	3
K4	MSIOD100PB6/GB5/CCC_SW1_CLKI1	6	MSIOD118PB7/GB5/CCC_SW1_CLKI1	7	MSIOD175PB7/GB5/CCC_SW1_CLKI1	7

Table 7 • **Equivalent Global Pins Per Device *(continued)***

	FG484 Pin Names					
Package Pin	**M2GL025**	**Bank No**	**M2GL050**	**Bank No**	**M2GL090**	**Bank No**
K6	MSIO99PB7/CCC_NW0_CLKI0	7	MSIO117PB8/CCC_NW0_CLKI0	8	MSIO159PB8/CCC_NW0_CLKI0	8
K8	MSIOD101PB6/GB1/CCC_SW0_CLKI1	6	MSIOD119PB7/GB1/CCC_SW0_CLKI1	7	MSIOD176PB7/GB1/CCC_SW0_CLKI1	7
M7	MSIOD102PB6/CCC_SW1_CLKI0	6	MSIOD120PB7/CCC_SW1_CLKI0	7	MSIOD177PB7/CCC_SW1_CLKI0	7
P22	MSIO11PB2/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A	2	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A	3	MSIO11PB3/CCC_NE0_CLKI0/I2C_1_SDA/GPIO_0_A/USB_DATA3_A	3
R22	MSIO11NB2/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A	2	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A	3	MSIO11NB3/CCC_NE1_CLKI0/I2C_1_SCL/GPIO_1_A/USB_DATA4_A	3

Note: See, “Dedicated Global I/O Naming Conventions” section in *IGLOO2 Pin Descriptions*.

2.1.3.2 Available versus No Connect Pins

Few pins have specific functions in one device, and the same pins are set to no connect (NC) in the other device. For example, pin AA20 functions as the VPP pin in the M2GL025 device while it is an NC in the M2GL050 device. Similarly, T11 pin is an NC in the M2GL025 device but it is a VREF5 pin in the M2GL050 device. Table 8, page 9 lists the summary of such pins.

When moving from a device where the I/O is an NC pin, to a device where the I/O has a defined functionality but is not used, follow the recommended methods for connecting the unused I/Os depending on the functionality of that I/O. See, “Unused Pin Configurations” in the *Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA Application Note*.

When moving from a device where the I/O has a defined functionality, to a device where the I/O is an NC, the NC pins can either be driven to any voltage or can be left floating with no effect on the operation of the device. NC indicates that the pin is not connected to circuitry within the device.

Table 8 • **Available versus NC Pins**

	FG484 Pin Names		
Package Pin	**M2GL025**	**M2GL050**	**M2GL090**
T11	NC	VREF5	NC
T12	NC	VREF5	NC
AA20	VPP	NC	VPP
AB20	VPP	NC	VPP

Note: FCG484 package has BANK5 configured as DDRIOs. If the customer wants to connect to the differential signals (for e.g: SSTL18,SSTL15) then VREF5 pin must be connected to the respective voltage. In unused condition the VREF5 can be DNC.

2.1.3.3 I/Os Technology Compatibility Per Pin or Bank

The following table shows the list of I/Os that lead to incompatibility with the different technology support, while migrating between the M2GL025, M2GL050, and M2GL090 devices within the FG484 package.

The difference is the type of I/O technology (MSIO versus DDRIO) that is supported on those regular I/Os.

Table 9 • **I/O Standards Compatibility Per Device or Package Pins**

	FG484 Pin Names					
Package Pin	**M2GL025**	**Bank No**	**M2GL050**	**Bank No**	**M2GL090**	**Bank No**
AA10	MSIO122PB4	4	DDRIO149PB5	5	MSIO198PB5	5
AA12	MSIO127PB4	4	DDRIO157PB5	5	MSIO204PB5	5
AA15	MSIO134NB4	4	DDRIO164NB5	5	MSIO213NB5	5
AA16	MSIO138PB4	4	DDRIO167PB5	5	MSIO222PB5	5
AA17	MSIO138NB4	4	DDRIO167NB5	5	MSIO222NB5	5
AA18	MSIO137NB4	4	DDRIO174NB5	5	MSIO221NB5	5
AB10	MSIO122NB4	4	DDRIO149NB5	5	MSIO198NB5	5
AB14	MSIO129NB4	4	DDRIO161NB5	5	MSIO208NB5	5
AB17	MSIO137PB4	4	DDRIO174PB5	5	MSIO221PB5	5
AB18	MSIO142PB4	4	DDRIO177PB5	5	MSIO230PB5	5
AB19	MSIO142NB4	4	DDRIO177NB5	5	MSIO230NB5	5
T13	MSIO131NB4	4	DDRIO166NB5	5	MSIO210NB5	5
T16	MSIO143NB4	4	DDRIO186NB5	5	MSIO232NB5	5
U10	MSIO123PB4	4	DDRIO154PB5	5	MSIO199PB5	5
U11	MSIO123NB4	4	DDRIO154NB5	5	MSIO199NB5	5
U14	MSIO136PB4	4	DDRIO176PB5	5	MSIO218PB5	5
U15	MSIO136NB4	4	DDRIO176NB5	5	MSIO218NB5	5
U16	MSIO143PB4	4	DDRIO186PB5	5	MSIO232PB5	5
U17	MSIO144NB4	4	DDRIO189NB5	5	MSIO234NB5	5
U18	MSIO146NB4	4	DDRIO190NB5	5	MSIO238NB5	5
V12	MSIO128NB4	4	DDRIO159NB5	5	MSIO206NB5	5
V13	MSIO132PB4	4	DDRIO171PB5	5	MSIO211PB5	5
V14	MSIO132NB4	4	DDRIO171NB5	5	MSIO211NB5	5
V16	MSIO139NB4	4	DDRIO184NB5	5	MSIO224NB5	5
V17	MSIO144PB4	4	DDRIO189PB5	5	MSIO234PB5	5
V18	MSIO146PB4	4	DDRIO190PB5	5	MSIO238PB5	5
W14	MSIO133NB4	4	DDRIO169NB5	5	MSIO212NB5	5
W15	MSIO135NB4	4	DDRIO172NB5	5	MSIO216NB5	5
W16	MSIO139PB4	4	DDRIO184PB5	5	MSIO224PB5	5
W17	MSIO140NB4	4	DDRIO182NB5	5	MSIO226NB5	5
W19	MSIO145NB4	4	DDRIO187NB5	5	MSIO236NB5	5
Y12	MSIO127NB4	4	DDRIO157NB5	5	MSIO204NB5	5
Y13	MSIO130NB4	4	DDRIO162NB5	5	MSIO209NB5	5
Y15	MSIO135PB4	4	DDRIO172PB5	5	MSIO216PB5	5

Table 9 • **I/O Standards Compatibility Per Device or Package Pins *(continued)***

	FG484 Pin Names					
Package Pin	**M2GL025**	**Bank No**	**M2GL050**	**Bank No**	**M2GL090**	**Bank No**
Y17	MSIO140PB4	4	DDRIO182PB5	5	MSIO226PB5	5
Y18	MSIO141PB4	4	DDRIO181PB5	5	MSIO228PB5	5
Y19	MSIO141NB4	4	DDRIO181NB5	5	MSIO228NB5	5
Y20	MSIO145PB4	4	DDRIO187PB5	5	MSIO236PB5	5

The DDRIOs do not support single ended 3.3 V I/O standards and differential LVPECL, LVDS 3.3 V, LVDS 2.5 V, RSDS BLVDS, MLVDS, and Mini-LVDS I/O standards, as shown in the following table. To migrate between M2GL025, M2GL050, and M2GL090 devices successfully, ensure that the correct VDDI power supply is used to power the equivalent banks. Only I/Os with compatible standards can be assigned to the same bank.

Table 10 • **Technology Support Difference Between Different I/O Types**

	I/O Types	
I/O Standards	**MSIO**	**DDRIO**
Single-Ended I/O		
LVTTL 3.3V	Yes	–
LVCMOS 3.3V	Yes	–
PCI	Yes	–
LVCMOS 1.2V	Yes	Yes
LVCMOS 1.5V	Yes	Yes
LVCMOS 1.8V	Yes	Yes
LVCMOS 2.5V	Yes	Yes
Voltage-Referenced I/O		
HSTL 1.5V	Yes	Yes
SSTL 1.8	Yes	Yes
SSTL 2.5	Yes	Yes
SSTL 2.5 V(DDR1)	Yes	Yes
SSTL 1.8 V(DDR2)	Yes	Yes
SSTL 1.5 V (DDR3)	Yes	Yes
Differential I/O		
LVPECL (input only)	Yes	–
LVDS 3.3 V	Yes	–
LVDS 2.5 V	Yes	–
RSDS	Yes	–
BLVDS	Yes	–
MLVDS	Yes	–
Mini-LVDS	Yes	–

Note: Even though the VDDI may be the same (for example, MSIO 2.5 V and DDRIO 2.5 V), the attributes and features supported may be different for different I/O types (MSIO versus DDRIO). See, “I/O

Programmable Features" section in *IGLOO2 FPGA Fabric User Guide* for more information on the list of features supported per I/O type.

2.1.3.4 Probe Pins

Probe pin locations are not compatible between the M2GL025 and M2GL050 devices, and also between the M2GL050 and M2GL090 devices. They are compatible between the M2GL025 and M2GL090 devices. The following table shows the different probe I/O locations per device within the FG484 package. By default, probe pins are reserved for the probe functionality.

Unreserve these pins by clearing the **Reserve Pins for Probes** check box in the **"Device I/O Settings**" under **Project Settings** in Libero SoC software. When the pins are not reserved, the probe I/Os can be used as regular I/Os.

Table 11 • **Probe Pins Per Device**

Package Pin	FG484 Pin Names					
	M2GL025	**Bank No**	**M2GL050**	**Bank No**	**M2GL090**	**Bank No**
W10	MSIO121PB4 /PROBE_A	4	DDRIO151PB5	5	MSIO197PB5/PROBE_A	5
W9	MSIO120PB4	4	DDRIO148PB5 /PROBE_A	5	MSIO196PB5	5
Y9	MSIO120NB4 /CCC_SW0_CLKI2	4	DDRIO148NB5 /PROBE_B	5	MSIO196NB5 /CCC_SW0_CLKI2	5
Y10	MSIO121NB4 /PROBE_B	4	DDRIO151NB5	5	MSIO197NB5/PROBE_B	5

For vertical migration between the devices, one way of maintaining the compatibility is to use the **Reserve Pin** option. Select the **User Reserved** option in the **Package Pins** tab which is a part of the **I/O Editor** in Libero SoC software, on the pins that are not probe pins. When a pin is reserved, that pin is not assigned to any port. For example, if M2GL025 design is migrated to M2GL050 where the probe pins (PROBE_A and PROBE_B) are used in the M2GL050 device, reserve the pins W9 and Y9 in the M2GL025. When the design is moved up to M2GL050, the pins are already probe pins and are reserved for probes by default. That is one way to achieve the design compatibility during the migration of probe pins. Another option is to reserve all four pins and route all these four pins to a connector on the PCB.

2.1.4 Power Supply and Board-Level Considerations

I/O power supply requirements are one of the key aspects to consider for design migrations. Since the migration is within the IGLOO2 family, there is no issue regarding the core voltage (VDD), charge pumps voltage (VPP), and analog sense circuit supply of the eNVM voltage (VPPNVM). The ground pins (VSS) are also equivalent between the M2GL025, M2GL050, and M2GL090 devices. See, *IGLOO2 Pin Descriptions* for more information. The bank supply voltage VDDI pins must be connected appropriately. All the bank supplies that are located on the east-side must be powered even if the associated bank I/Os are not used. See the, "Recommendation for Unused Bank Supplies" connections table in the *Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA Application Note* for more information, in case the specific banks are not used.
An MSIO bank supports 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V voltages and MSIOD and DDRIO banks support 1.2 V, 1.5 V, 1.8 V, or 2.5 V voltages. For more information on user I/O pins (MSIO, MSIOD, and DDRIO) and supported voltage standards, see the "Supported Voltage Standards" table in the *IGLOO2 FPGA Fabric User Guide*.

The banks have dedicated supplies. Therefore, only I/Os with compatible voltage standards can be assigned to the same I/O voltage bank. The correct bank supply must be used during migration between the different devices as per the appropriate voltages (I/O Standards) selected for the bank.

The following table shows the power supply compatibility of different banks per device in the FG484 package.

Table 12 • **Power Supply Compatibility Per Device**

	FG484 Pin Names		
Package Pin	**M2GL025**	**M2GL050**	**M2GL090**
AA19	VDDI4	VDDI5	VDDI5
AB12	VDDI4	VDDI5	VDDI5
B12	VDDI0	VDDI0	VDDI1
B16	VDDI0	VDDI0	VDDI1
B20	VDDI0	VDDI0	VDDI1
B8	VDDI0	VDDI0	VDDI1
C10	VDDI0	VDDI0	VDDI1
C14	VDDI0	VDDI0	VDDI1
C2	VDDI7	VDDI8	VDDI8
C6	VDDI0	VDDI0	VDDI1
D17	VDDI0	VDDI0	VDDI1
E11	VDDI0	VDDI0	VDDI1
E20	VDDI1	VDDI1	VDDI2
F1	VDDI7	VDDI8	VDDI8
F13	VDDI0	VDDI0	VDDI1
F22	VDDI1	VDDI1	VDDI2
F7	VDDI0	VDDI0	VDDI1
F9	VDDI0	VDDI0	VDDI1
G4	VDDI7	VDDI8	VDDI8
H12	VDDI0	VDDI0	VDDI1
H14	VDDI0	VDDI0	VDDI1
H18	VDDI1	VDDI1	VDDI2
J21	VDDI1	VDDI1	VDDI2
J7	VDDI7	VDDI8	VDDI8
K3	VDDI6	VDDI7	VDDI7
L17	VDDI2	VDDI3	VDDI3
L6	VDDI6	VDDI7	VDDI7
M20	VDDI2	VDDI3	VDDI3
N2	VDDI6	VDDI7	VDDI7
P5	VDDI6	VDDI7	VDDI7
R19	VDDI2	VDDI3	VDDI3
T14	VDDI4	VDDI5	VDDI5
T22	VDDI2	VDDI3	VDDI3
U2	VDDI5	VDDI6	VDDI6
V10	VDDI4	VDDI5	VDDI5

Table 12 • **Power Supply Compatibility Per Device *(continued)***

	FG484 Pin Names		
Package Pin	**M2GL025**	**M2GL050**	**M2GL090**
W13	VDDI4	VDDI5	VDDI5
W21	VDDI3	VDDI4	VDDI4
Y16	VDDI4	VDDI5	VDDI5

For the other bank supplies that are equivalent, see the provided recommendations in the *IGLOO2 Pin Descriptions*.

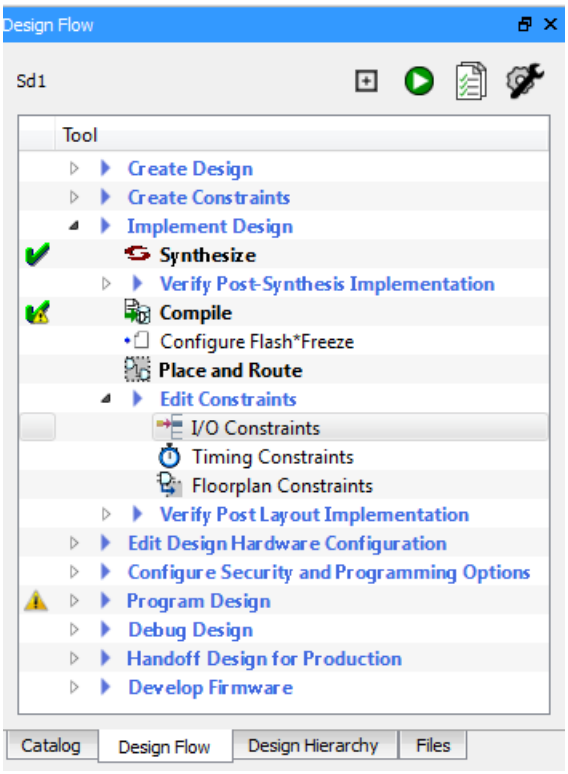
Any other board-level considerations are common among the two devices. See the *Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA Application Note* for more details.

2.1.5 Software Flow

The Libero SoC software provides the option of reserving pins for moving between different devices within the IGLOO2 family where pins within the current device that are not bonded in the destination device can be automatically reserved. This option is available in the **I/O Constraints** Editor which can be accessed from the **Design Flow** window as shown in the following figure. This is done in the early stages of the design cycle. Pins can be reserved as follows:

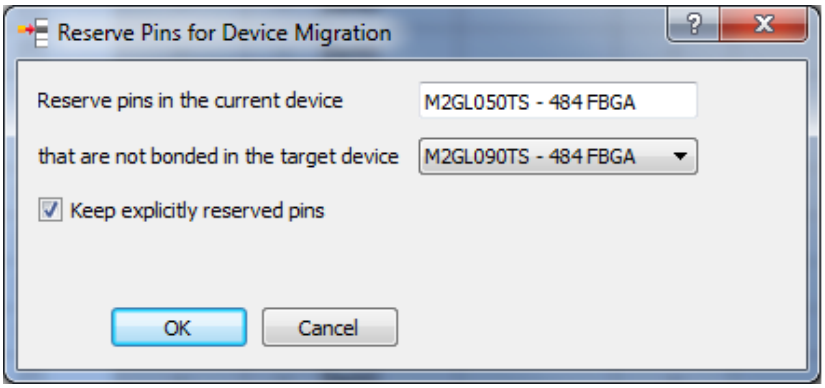
1. After finishing the **Compile** stage, select the **I/O Constraints** option from the **Design Flow** window as shown in the following figure.

Figure 4 • **I/O Constraint Editor Option part of the Design Flow**



2. Select the **Reserve Pins for Device Migration** option from the Tools menu. The window shown below in the following figure is displayed.

Figure 5 • **Reserve Pins for Device Migration**

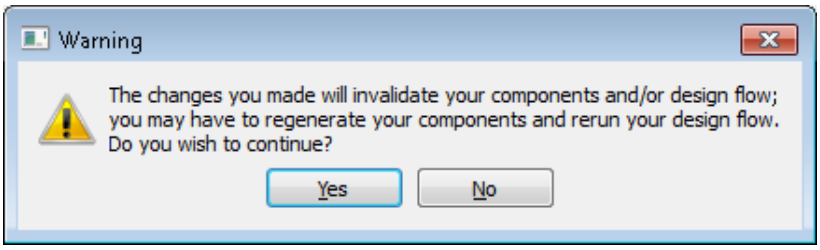


The first option shows the device that is currently being used in the Libero SoC project. From the drop-down list, select the device that eventually will be migrated to as the target device. See the Libero Soc software online help for more details on this window and other options.

The Libero SoC software provides the option of moving between different devices within the SmartFusion®2 family by changing the device selection using the **Project Settings** option in the Libero SoC software. Upon changing the device, Libero SoC software validates the features that are used within the design against the supported features within the new targeted device and package. Feedback messages are provided as part of the Libero SoC software flow listing the different actions taken by Libero SoC and the action required.

The first step that Libero SoC performs upon changing the device is to invalidate the original design components and the design flows. The message is displayed as shown in the following figure.

Figure 6 • **Invalidating Component and Design Flow Message**



As part of rerunning the design flow, Libero SoC checks the different steps to be performed for completing and updating the design flow. Furthermore, Libero SoC converts the HPMS configurations to be compatible with the selected device and package combination. Part of the HPMS conversion, any changes that were made automatically to be compatible with the device and package selected are printed to the log window. Libero SoC disables or defaults to different options, if the current selected options are not supported in the new targeted device and package.

After the HPMS configuration conversion is done, HPMS must be regenerated. To regenerate the HPMS component, open the HPMS component from **Libero SoC Design Hierarchy Flow** window and proceed through the different HPMS pages to complete the generation.

2.2 Conclusion

This application note describes the design migration among IGLOO2 family devices focusing on migration between the M2GL025, M2GL050, and M2GL090 devices within the FG484 package. IGLOO2 family devices share many common architectural features. Differences in architecture should be considered, to ensure seamless migration flow. Additionally, a key requirement is to run the functional simulation and timing analysis before and after the migration using Microsemi tools.