Release Notes For Model*Sim* ME 10.2c

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- **How to Get Support**

  Model*Sim* ME is supported by Microsemi Inc.

  - Telephone Support

    Call 1-800-262-1060

  - Email Support

    soc_tech@microsemi.com

  - World-Wide-Web Support

    http://www.actel.com/support

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Key Information

- The following lists the supported platforms:
  - win32acoem - Windows XP, Windows 7
  - linuxacoem - RedHat Enterprise Linux 4, 5 and 6, SUSE Linux Enterprise Server 10 and 11

Compatibility Issues with Release 10.2c

SystemVerilog Compatibility

- dvt34396 - (results) Conditional $nochange timing checks could report false timing check violations.

Mixed Language Compatibility

- dvt36274 - (results) Array indices would sometimes not line up between SystemVerilog and VHDL multi-d array signals used at the SV-VHDL mixed-language boundary, if the connections were made using either direct port-connections or mixed-language hierarchical references. This has been fixed.

Coverage Compatibility

- dvt37416 - (results) Expressions/Conditions with interface signals used as terminals are sometimes not considered for expression/condition coverage. This has been fixed. Expression coverage numbers may change due to this fix because of more expressions being considered for coverage.

- dvt27713 - (results) Incorrect matching input patterns were reported for some expressions containing a mixture of short-circuiting and non-short-circuiting operators. This has been fixed. This fix may result in different coverage numbers for expression and condition coverage.

General Defects Repaired in 10.2c

- dvt37465 - Fixed possible vopt internal error with -nodebug specified. This error occurred only using the flat library type.

User Interface Defects Repaired in 10.2c

- dvt37091 - Some members of class objects were missing when expanding the class in the Objects window. This issue is now fixed.
- dvt37380 - GUI will crash randomly when browsing SV Class related source code when UVM is present. This issue has been fixed.
- dvt37197 - The error reporting that message 3607 is not suppressible is not printed before vsim exits. This oversight has been corrected.

SystemVerilog Defects Repaired in 10.2c

- dvt34396 - (results) Conditional $nochange timing checks could report false timing check violations.
- dvt37449 - Using a 'disable' statement inside a fork..join_none block in a function would sometimes cause code after the disable to be skipped even when the current thread was not disabled.
- dvt32543 - Vlog and vopt would sometimes generate an internal error when using an inline randomization constraint inside a fork..join block in a class method.
- dvt37749 - Using SV bind construct with a SV module as the target would sometimes make vsim error out with '(vsim-3171) machine code not found' error if the bind's target module contained nested modules. This has been fixed.
- dvt37678 - Using SV bind construct to bind an interface into another interface inside a PDU would make vsim error out with error 'vsim-3843'. This has been fixed.
- dvt37262 - Using SV bind construct to bind an interface int a SV module and having the bound interface access an item in another interface that is passed as a port to the target module of bind would result in an invalid error in vopt, if the target module of bind was inside a PDU. This has been fixed.
- dvt37893 - Using SV bind construct to bind to a PDU target located in a different library than the bind statement and bound module would sometimes result in vsim exiting with an invalid '(vsim-7) Failed to open info file' error. This has been fixed.

- dvt37434 - Using -f option with qverilog would sometimes generate an invalid '(vish-3296) invalid error' if the arguments file contained -R arguments. This has been fixed.
- dvt36988 - Logical equivalence (<->) operator over constant literals gave incorrect result.
- dvt37962 - vopt crashed under certain scenario when DPI import declarations omit the formal argument names.

VHDL Defects Repaired in 10.2c

- dvt37271 - The compiler could incorrectly remove statements containing impure calls to subprograms defined in package instances when the subprogram calls must remain in order to alter the state of shared variables.
- dvt37228 - In a configuration declaration, a block configuration that configures a given block will imply a default binding for a component instantiation statement contained in the block under certain circumstances. The circumstances under which this can happen are when neither an explicit configuration specification in the block, nor an explicit component configuration (having a binding indication) in the block configuration, applies to the component instantiation statement. When the USE clauses in effect for the block configuration provide more libraries in which to look for an entity as per the default binding rules, then the default binding at the place of the block configuration is potentially different from the default binding at the place of the component instantiation statement in the block being configured. In this case, the default binding at the place of the block configuration will be used. An implicit component configuration (having no binding indication) is assumed to exist for any component instantiation statement that has no explicit configuration specification (in the block) or component configuration (in the block configuration), so these default binding rules also apply to any unconfigured component instantiation statements in any given block. Use the vcom switch "-nocompconfigdefaultbinding", or INI file [vcom] section variable "NoVHDLCompConfigDefaultBinding = 1", to revert to prior behavior.
- dvt37646 - When the compiler generates native code for a configuration declaration (as happens when -novopt is given), every architecture body configured by a block configuration must have had its native code already generated. The error message occurring when this requirement was not met was too cryptic. A better error message (#1512) has been implemented when this situation arises.

Mixed Language Defects Repaired in 10.2c

- dvt36589 - Using $bits on a VHDL signal as a parameter actual in a SystemVerilog bind statement with a VHDL target scope would make vopt error out with an 'Illegal use of signal as parameter actual' error. This has been fixed.
- dvt36274 - (results) Array indices would sometimes not line up between SystemVerilog and VHDL multi-d array signals used at the SV-VHDL mixed-language boundary, if the

connections were made using either direct port-connections or mixed-language hierarchical references. This has been fixed.

SystemVerilog Enhancements in 10.2c

- dvt36764 - Added new vsim switch "-trace_dpi <n>" to trace DPI-C import/export calls.
- `-trace_dpi <n>  Set DPI tracing to level <n>. The default is 0 which turns off tracing.`
- `The levels of support are:`
- `1 - turning on all tracing`
- `0 - turning off all tracing (default)`
- `i - turning on the tracing of DPI import call only`
- `e - turning on the tracing of DPI export call only`
- `a - turning on the tracing of DPI import/export call arguments only`