UG0362
User Guide
Three-phase PWM v4.1

Microsemi
Power Matters.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

The following is a summary of the changes in revision 6.0 of this document.

- The Key Features and Supported Families sections were added to the Overview chapter.
- The Inverter Bridge for AC Motors section was renamed Theory of Operation in the Overview chapter.
- Figure 5 was corrected with additional input.

1.2 Revision 5.0

The following is a summary of the changes in revision 5.0 of this document.

- A new pin is added in the block diagram of three-phase PWM. For more information, see Figure 5, page 5.
- Added the en_dual_trig_i entry in the input and output ports of three-phase PWM table. For more information, see Table 1, page 5.
- Deleted the Configuration Parameters section from the Hardware Implementation chapter.
- Updated Resource Utilization Report of Three-phase PWM values in the table. For more information, see Table 2, page 6.

1.3 Revision 4.0

Updated and merged the user guide (w.r.t UG0362).

1.4 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Updated Table 2 (SAR 64756).
- Added Table 5 (SAR 64756).

1.5 Revision 2.0

The following is a summary of the changes in revision 2.0 of this document.

- Updated the title of the user guide (SAR 63245).
- Updated Table 3 (SAR 63245).

1.6 Revision 1.0

Initial release.

2 Overview

The three-phase PWM generates carrier based center aligned PWM to trigger the switches of a three-phase inverter. The module also introduces a configurable dead time to avoid dead short circuits. A delay time can be introduced to synchronize multiple three-phase PWM block instantiations for multi-axis or for harmonic cancellation in case of multi-level inverters.

2.1 Key Features

The three-phase PWM IP block supports the following features:

- Generate three-phase pulse width modulated signals based on three independent references
- Introduce a delay time to adjust the phase of PWM cycles between two three-phase PWM blocks
- Introduce a configurable dead time to avoid dead shorts in the inverter bridge
- Enable/disable signal to shut down the PWM output signals within one system clock cycle
- Generate timing pulses for other blocks—configurable as one/two pulses per period

2.2 Supported Families

The three-phase PWM IP block supports the following families:

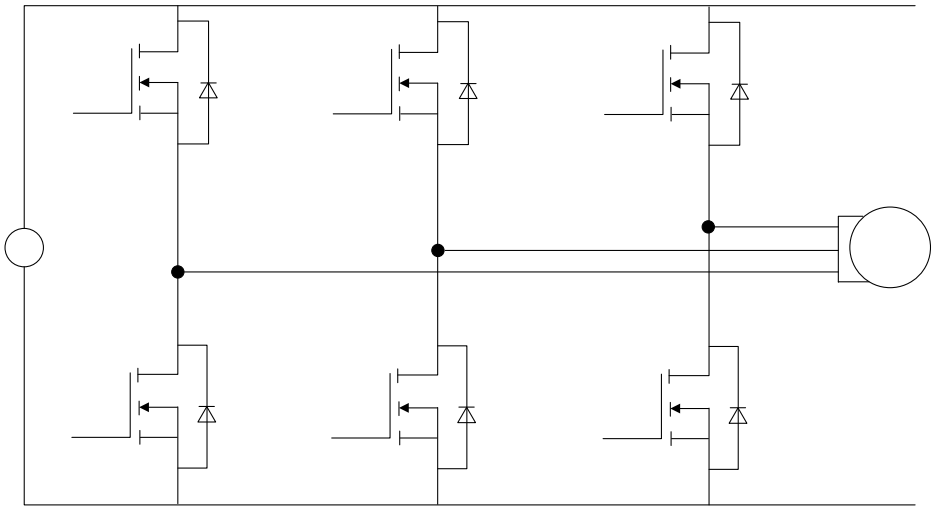
- SmartFusion2
- IGLOO2
- RTG4™

2.3 Theory of Operation

The three-phase inverter is the core of any AC motor drive. PWM pulses generated by the three-phase PWM drive the inverter bridge.

The following figure shows the inverter bridge.

Figure 1 • **Three-phase Inverter Bridge**

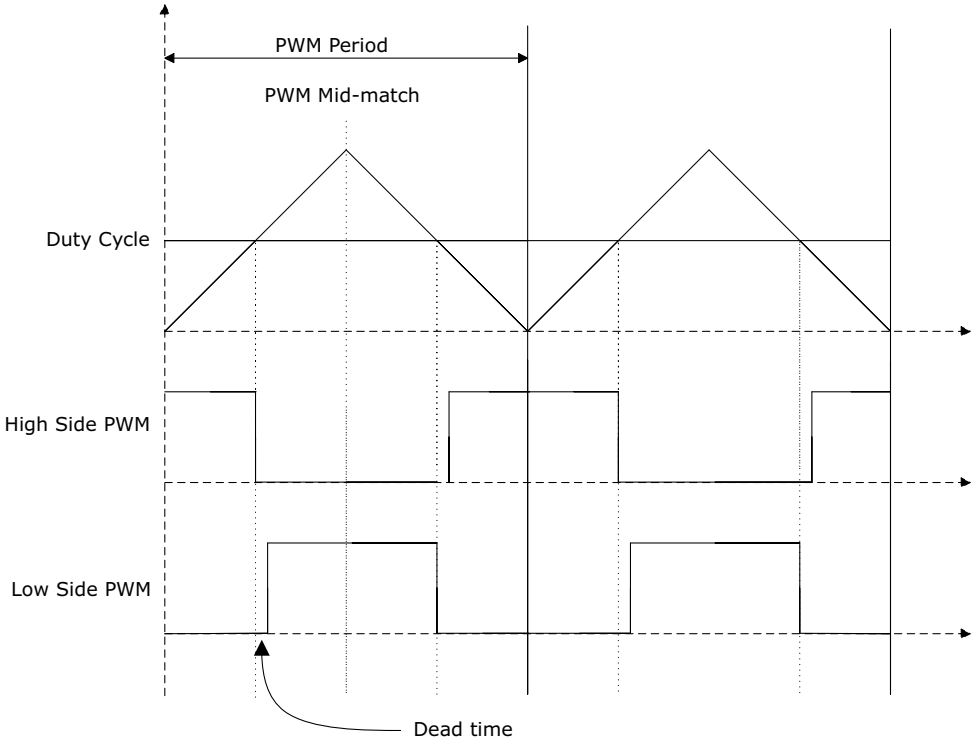


A three-phase two level inverter consists of three power electronic switches (Transistors), two in each leg for each phase of motor winding. The switches in each leg are driven by complementary pulses to switch the phase voltage between positive and negative DC voltage. The DC voltage passes through the transistor switches to the load when at least one of the three-phase pulses is active. Dead time is introduced between these high and low pulses of a phase or channel to allow the transistor to turn off completely, so that the DC source does not get shorted during operation.

2.4 Generating Center Aligned PWM

In center aligned PWM, the PWM counter goes from a down-count to an up-count to down-count again, and so on. Figure 2, page 3 represents the operation of center aligned PWM. The PWM counter keeps running as long as the module is not in reset state, even when the PWM module is not enabled.

Figure 2 • **Center Aligned PWM**

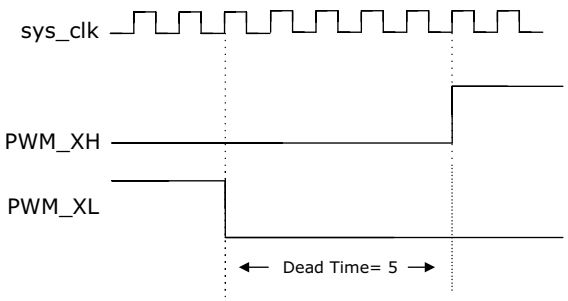


2.5 Dead Time and Delay Time

A time delay is introduced between turning off one of the transistors of a leg of an inverter to turning on the other transistor to ensure that a dead short circuit does not occur. This is called dead time.

The following figure shows the dead time insertion.

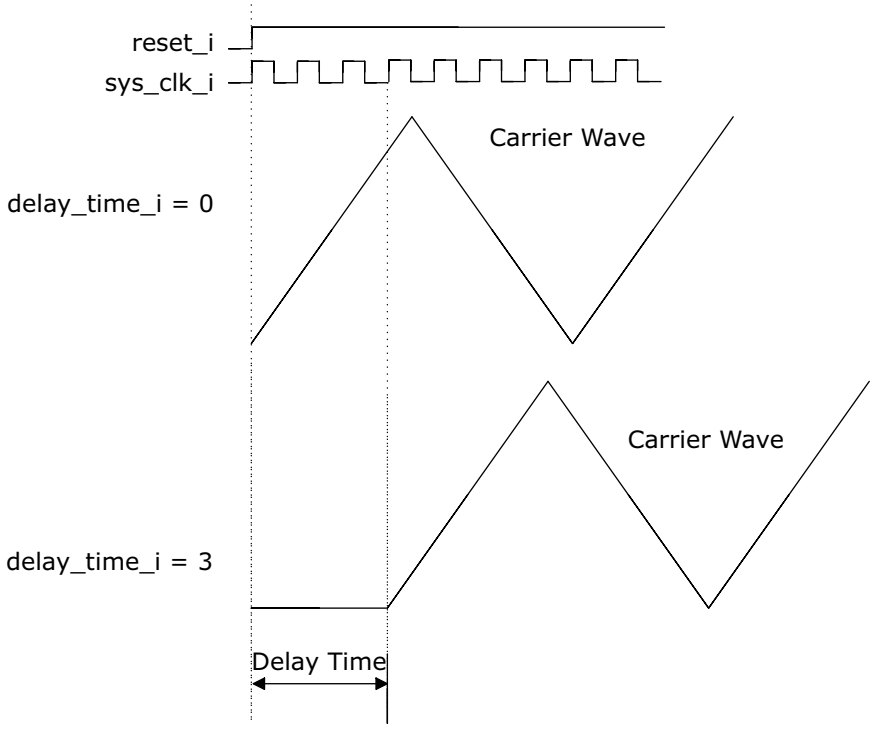
Figure 3 • **Dead Time Insertion**



When multiple PWM blocks are present in a single system, some harmonics can be eliminated by phase shifting the PWM carrier wave. This time delay is referred to as delay time. This time delay is accounted for by the delay in generating carrier waves after reset.

The following figure shows how delay time is introduced.

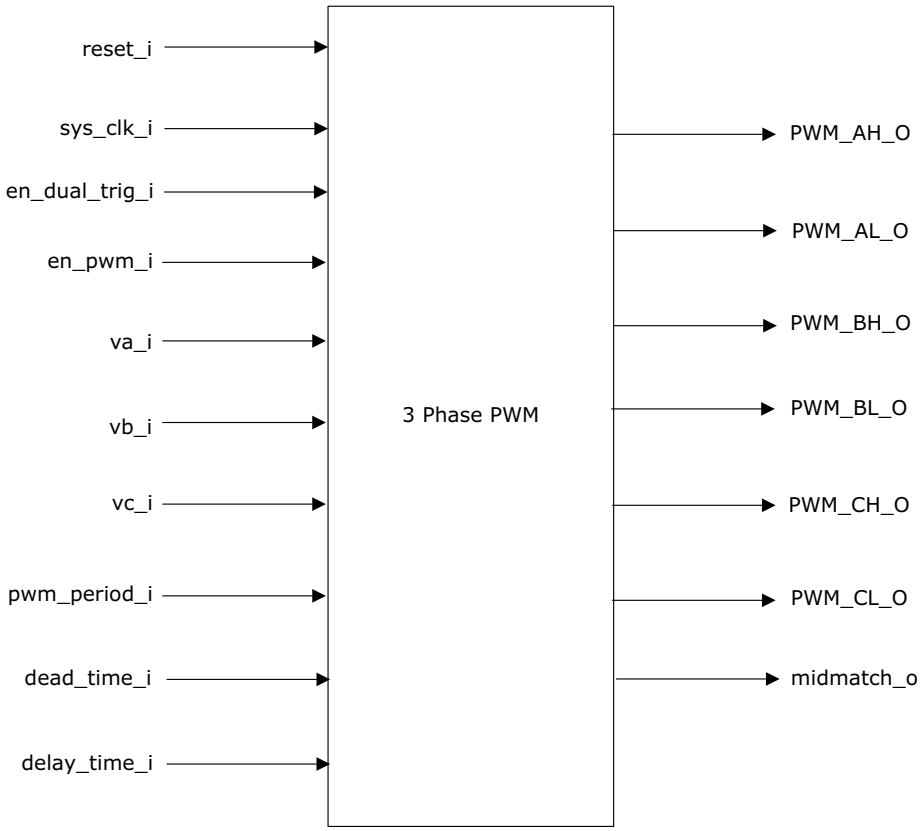
Figure 4 • **Effect of Delay Time**



3 Hardware Implementation

The following figure shows the block diagram of three-phase PWM.

Figure 5 • **System-level Block Diagram of Three-phase PWM**



3.1 Inputs and Outputs

The following table lists the input and output ports of three-phase PWM.

Table 1 • **Inputs and Outputs of Three-phase PWM**

Signal Name	Direction	Description
reset_i	Input	Asynchronous active low reset signal
sys_clk_i	Input	System Clock
en_pwm_i	Input	Asynchronous enables: When 0, PWM outputs are driven to 0 When 1, PWM outputs are generated
en_dual_trig_i	Input	When 1, PWM produces two trigger pulses distributed evenly per cycle at the midmatch_o output. When 0, PWM produces one trigger pulse per cycle at the midmatch_o output.
va_i	Input	Phase A duty cycle with respect to pwm_period
vb_i	Input	Phase B duty cycle with respect to pwm_period

Table 1 • **Inputs and Outputs of Three-phase PWM *(continued)***

Signal Name	Direction	Description
vc_i	Input	Phase C duty cycle with respect to pwm_period
pwm_period_i	Input	Time period of PWM in number of system clock time
dead_time_i	Input	Dead time
delay_time_i	Input	Delay time
midmatch_o	Output	Period mid-match interrupt produces two pulses per PWM cycle when en_dual_trig_i input is 1, and produces one pulse per PWM cycle when en_dual_trig_i input is 0.
PWM_AH_O	Output	Channel A PWM for high side switch
PWM_AL_O	Output	Channel A PWM for low side switch
PWM_BH_O	Output	Channel B PWM for high side switch
PWM_BL_O	Output	Channel B PWM for low side switch
PWM_CH_O	Output	Channel C PWM for high side switch
PWM_CL_O	Output	Channel C PWM for low side switch

Note: Configurable parameters are not available for this IP.

3.2 Resource Utilization

The following table lists the resource utilization report after synthesis.

Table 2 • **Resource Utilization**

Cell Usage	Count
SLE (Sequential)	40
Combinational Logic	230
MACC	0
RAM1Kx18	0
RAM64x18	0