Silicon Explorer II Frequently Asked Questions

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Microsemi

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I. General

1. What is Silicon Explorer II?

Silicon Explorer II is Microsemi®'s proprietary real-time FPGA debug tool. You have access to 100 percent of the internal nets of the Microsemi FPGA while the device is operating in a prototype or production system. You can select any of the two nets and probe nodes at the same time without changing the placement and routing, or using any additional resource. Moreover, the timing of a design does not change while selecting new nodes to probe.

2. What is different between Silicon Explorer I and Silicon Explorer II?

The first version of Silicon Explorer was designed to support only 3.3 V and 5.0 V devices. It also takes its power from the board causing potential limitations while sampling at high frequencies.

Silicon Explorer II has its own external power supply. It allows Silicon Explorer II to operate correctly on devices which utilize 2.5 V power supplies, and eliminates the power burden on the board. Other new features include four levels of triggering for each signal, decompression on download to speed-up response time, and system acquisition rates up to 100 MHz.

3. Does Silicon Explorer II support Flash FPGA debugging?

No. As of today, Silicon Explorer II does not support Flash FPGA debugging. For Flash FPGA debugging, refer to the *SoftConsole* or *SmartDebug* pages.

4. Can I use the probe pins as regular I/Os?

All of the probe pins, except the MODE and TMS pins, can be used as the user I/O. After the device enters the probe mode, I/Os switch to the probe functionality. Microsemi highly recommends that you do not use these pins as inputs, since your device does not accept the inputs during the probe mode.

II. Hardware

5. If my computer does not have a parallel port, can I use an adapter or converter with the corresponding driver to use Silicon Explorer II?

Microsemi did not test any adapters or converters with Silicon Explorer II. The only supported way of using Silicon Explorer II is with a laptop or PC that has a built-in serial port.

6. Can I use Silicon Explorer II on a laptop?

This is an excellent way to use Silicon Explorer II. Silicon Explorer II connects to a PC through a serial port. As long as a serial port is available on your laptop, you can have the ultimate portable debug solution.

Note: *As Silicon Explorer II does not get its power from the PC, you can also run the laptop on battery power.*

III. Software

7. What are the supported platforms for Silicon Explorer II software?

This software is compatible with Windows 98, Windows NT 4.0 SP6, Windows 2000, and Windows XP (SP1 and SP2) only. This software has not been tested on Windows XP SP3 or newer versions.

8. Where can I download the latest release of Silicon Explorer II software?

The latest version of the software is Silicon Explorer v5.2. It can be downloaded from the *Silicon Explorer II Downloads* page.

9. What file do I need to probe the device?

The only file required to probe the device is the probe file, which has an extension of `.prb`.

10. What is the recommended sampling rate?

For an accurate reading, the sampling rate of a particular signal should be at least twice the rate at which the signal is changing (according to the Nyquist theorem). For example, a clock operating at 25MHz should be sampled to at least 50 MHz frequency. Sampling at higher frequencies causes Silicon Explorer II to consume more power.

11. What are the features of the software provided with Silicon Explorer II?

Silicon Explorer II comes with the software that emulates an 18-channel logic analyzer. Two channels are used to monitor two internal nodes, and the other 16 channels are available to probe additional external signals. Moreover, the software allows you to set multi-level triggering schemes for each channel, multiple cursors to filter through the design internal nets, to define buses, and many other features commonly available in very expensive systems. The system also allows you to sample data up to 100 MHz, verify the checksum of your device while it is on the board, and the newest feature is cross-probing using Microsemi's ChipEdit tool.

IV. Probing

12. What are the PRA, PRB, PRC, and PRD pins? And what are they used for?

All of the antifuse FPGAs, except AX/RTAXS, have two probe pins, PRA and PRB. AX/RTAXS devices support two additional probe pins, PRC and PRD.

13. What is the probing limitation for RTAX/AX?

Worst case RTAX-S simulations show that 100 MHz signals can be observed without distortion. Typical case RTAX-S simulations show that up to 150 MHz signals can be observed without distortion.

14. What are the limitations in probing a device using Silicon Explorer II?

AX/RTAXS has the same limitations as SXA devices.Refer to *Troubleshooting Errors* section in *Silicon Explorer II User Guide*.

15. What is cross-probing?

This feature establishes communication between Microsemi's Timer, ChipEdit, and Silicon Explorer II for a complete debug loop. While evaluating the timing of critical paths in Timer, ChipEdit automatically highlights the placement of modules in these paths allowing observability of the relative placement of logic cells. From ChipEdit, you can call the highlighted nets in Silicon Explorer II to observe their real time values.

16. Is there a way to disable probing capability for security reasons?

Yes, by programming the security feature on the Microsemi FPGA, the built-in probe circuitry is permanently disabled.

V. Miscellaneous

17. Does Silicon Explorer II support chains of several RTSX-SU, RTAX-S, or AX devices?

RTAX: Only one device is supported at a time.

RTSX-SU: Only one device is supported at a time.

AX: Silicon Explorer Software v5.1 SPA and above support a chain of two AX devices. Refer to *New Features and Enhancements* section of the *Release Notes for Silicon Explorer Software v5.1 SPA*.

Note: *AX is the only device in which the Silicon Sculptor software can probe a chain of devices (maximum two devices).*

18. Does the Silicon Explorer II probe circuitry require the use of additional internal device resources?

No, this is one of the major benefits of the debugging system. Each Microsemi antifuse FPGA has built-in, dedicated circuitry just for probing purposes. Silicon Explorer II does not require any logic cells or routing when probing the device. Additionally, Silicon Explorer II does not require or sacrifice device I/Os. On SX-A and eX devices, the JTAG pins are used to control probing. On the older families, special probe pins are used for probing.

Regardless of the device, all of the probe pins, except the MODE and TMS pins, can be used as user I/O. After the device enters the probe mode, I/Os switch to the probe functionality. Microsemi recommends not using these pins as inputs, because they will not be available as inputs during the probe mode.

19. Does Silicon Explorer II retain any memory after debugging?

Silicon Explorer II has no memory devices on the board within the unit. No information is retained internally after power is removed.

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