Microsemi Corporation

October 24, 2013

Change Notification No: CN1306

CN Change Level: Minor

Customer Notification – Action Required

Subject: Libero SoC Software bugs for SmartFusion2 and IGLOO2 designs

Description of Issue(s):

1. There are two cases using Libero SoC v11.1 SP1 and v11.1 SP2 where a design simulates fine but will not operate correctly in silicon:

    a. If you use DDR_OUT macro in your design.
    b. If you combine an output or output enable register with an I/O using the PDC command set_io <portName> -register yes

Solution: The design should be migrated to Libero SoC 11.1 SP3, and compile and layout re-run.

2. Dedicated differential I/O driving the reference clock of a CCC may cause a functional issue due to a software bug.

When a design has a dedicated differential I/O pair driving the reference clock of the CCC, the input clock may not propagate to the CCC due to a software bug and the device will fail during silicon testing.

Details: There are several options to drive the ref clock of the CCC. One of the options is to drive from "Dedicated Input PAD x" (x = 0 to 3); this option uses hardwired routing. In this option, the user can choose single-ended I/O or differential I/O as the ref clock. The issue manifests itself when the differential I/O option is chosen (ie the dedicated differential I/O is used as the CCC reference clock input).

Please note that the issue can't be detected during functional simulation, and can only be detected in silicon testing.

Solution: The design should be migrated to Libero SoC 11.1 SP3, and compile and layout re-run.
http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc#downloads

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Products Affected by this Change: SmartFusion2 and IGLOO2 devices

Contact Information: Microsemi SoC Products Group

For any clarifications or questions, please contact Microsemi SoC Tech Support

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Regards,

Microsemi Corporation

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