



SmartFusion2 Software FAQs

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1. Where can I find information about the DSP flow?

DSP Quickstart and Design Tutorial document demonstrates the essential flow for directly generating RTL files from the design/higher-level algorithm created in the MathWorks' MATLAB®/ Simulink® software.

Refer to the [DSP Flow For SmartFusion2 SoC FPGA Quickstart and Design Tutorial](#) for more information.

To use the DSP flow, you should have the MathWorks MATLAB /Simulink software and license already installed. In addition, you need to install the Synopsys® Symphony Model Compiler AE. The Symphony Model Compiler AE can only be launched from the MATLAB/Simulink tools.

For more information about Symphony Model Compiler AE and the recommended, supported, and compatible MathWorks' tools versions, refer to the [Design Software](#) page.

2. Can I use the SmartFusion2 drivers provided by Microsemi together with my own application code eventually in production?

Yes, you can use SmartFusion2 devices firmware drivers, such as USB and MAC along with your application code for production purpose.

3. Why is Cortex-M3 processor not running at 166 MHz in my design as published?

When any peripheral is connected to Cortex-M3 processor, the frequency decreases. It might not run at the maximum speed of 166 MHz. The frequency depends on interconnected peripherals.

4. What is the speed of a mathblock?

A mathblock runs up to 350MHz depending on the application.

Refer to [Implementation of 9x9 Multiplications, Wide-Multiplier, and Extended Addition Using IGLOO2/ SmartFusion2 Mathblock](#) application note for further details.

Note: This is applicable only for SmartFusion2/IGLOO2 devices.

5. Does the MATLAB/Simulink front-end tool have a blockset that uses mathblocks?

A mathblock is available in an IP catalog. Apart from this, you can use mathblocks by using Symphony Model Compiler integrated with the Matlab tool.

Refer to the [DSP Flow For SmartFusion2 SoC FPGA Quickstart and Design Tutorial](#) for more information.

For more information on how to integrate and download Symphony model compiler, refer to the [Design Software](#) page.

6. Can the internal 25 MHz/ 50 MHz SmartFusion2 oscillator be used as the clock source for PCIe?

Yes, refer to [SmartFusion2 SoC FPGA Clocking Resources User Guide](#) for more information.

7. Can the internal 25 MHz/50 MHz SmartFusion2 oscillator be used as the clock source for USB?

Yes, refer to [SmartFusion2 SoC FPGA Clocking Resources User Guide](#) for more information.

8. What is maximum payload size for PCIe?

The maximum payload size for PCIe is 512 bytes.

9. How should the JTAGSEL pin of the SmartFusion2 device be connected?

JTAGSEL pin of SmartFusion2 device should be pulled high for use with SoftConsole and should be pulled low for use with IAR and Keil products.

10. What is the purpose of CoreConfigP core?

CoreConfigP facilitates the configuration of peripheral blocks (MDDR, FDDR, and SERDESIF) in a SmartFusion2 device.

It has a mirrored master APB port and several mirrored slave APB ports. The mirrored master port should be connected to the FIC_2_APB_MASTER master port of the microcontroller subsystem (MSS).

For example,

The MDDR controller must be configured to match the external DDR memory specifications. The configuration of the MDDR is defined in a file and is imported using the MDDR GUI configurator.

The configuration is done through the CoreConfigP soft IP core which is the master of the configuration data initialization process. Upon reset, the soft IP core CoreConfigP will copy the data from embedded nonvolatile memory (eNVM) to the configuration registers of the MDDR controller through the FIC_2 advanced peripheral bus (APB) Interface.

11. For which memories can SECEDED protection be enabled?

The single error correct double error detect (SECEDED) protection is available for following memories:

- Ethernet buffers
- CAN message buffers
- Cortex-M3 embedded scratch pad memory (eSRAMs)
- USB buffers
- PCIe buffer
- DDR memory controllers

Refer to the [SmartFusion2 SoC FPGA Reliability and Security User Guide](#) for more information on SECEDED.

12. What is the state of SmartFusion2 I/Os during JTAG programming?

While programming in JTAG mode, the Cortex-M3 processor is in reset. All I/Os (MSIO, MSIOD, and DDRIO) are controlled by boundary scan registers according to IEEE1149.1 and IEEE1532 standards. I/O state can also be configured before programming, in Libero SoC software using the "Specify I/O states during programming window" as shown in [Figure 1 on page 6](#).

Refer to the *Libero SoC v11.0 User Guide* for more information.

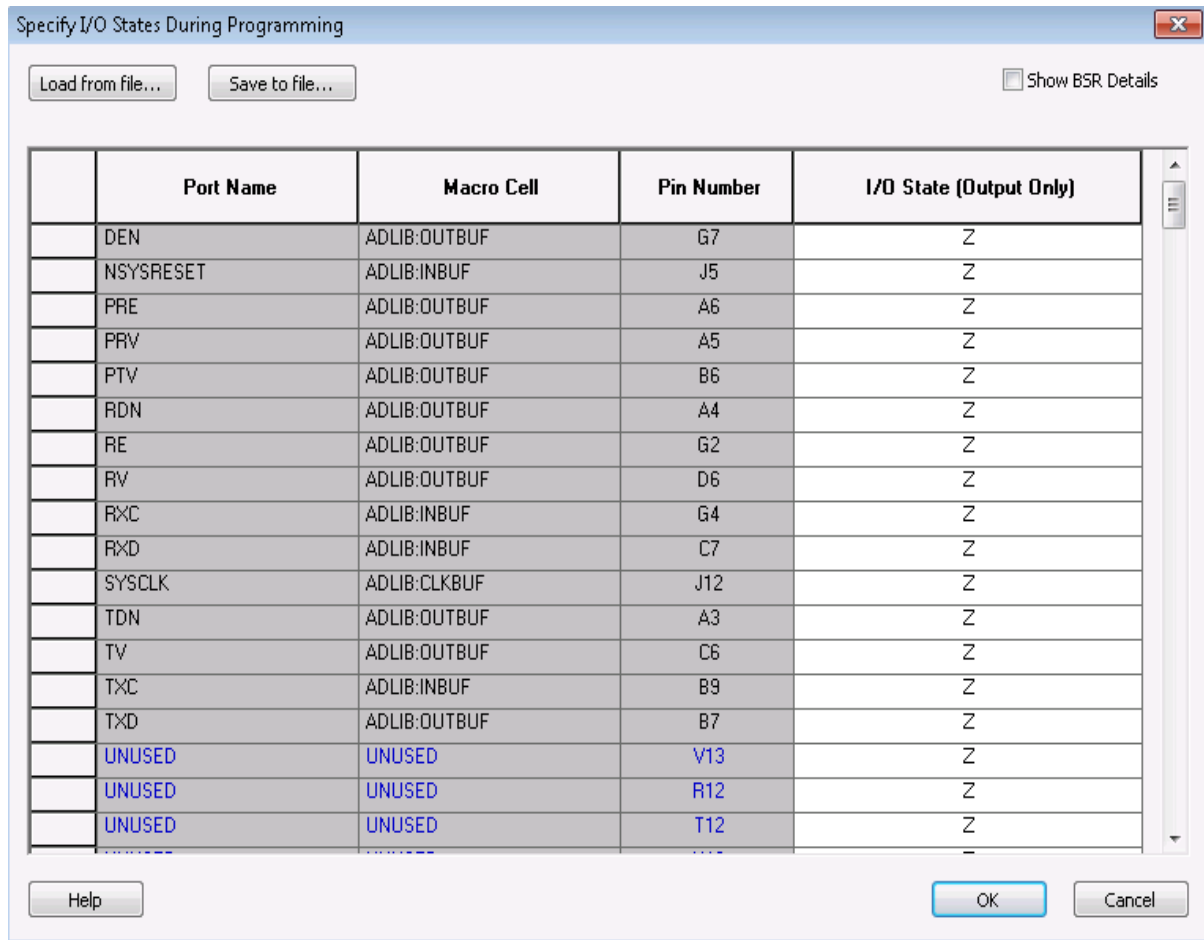


Figure 1: Specify I/O States During Programming Window

13. Where can I get the SmartFusion2 peripheral firmware drivers?

The firmware drivers are accessible from the SoftConsole firmware catalog. See [Figure 2](#).

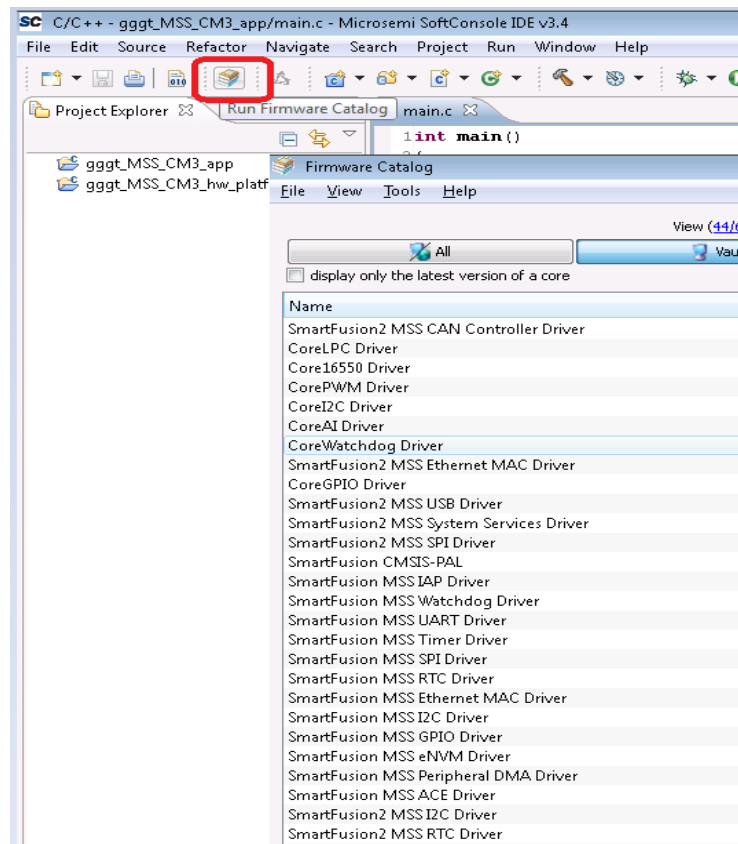


Figure 2: Firmware Catalog

14. What is the purpose of POWER_ON_RESET_N signal and what scenarios will assert this?

It is a power-on reset from system controller to the FPGA fabric. The system controller initiates reset due to power-on reset, assertion of DEVRST_N input, completion of programming, or completion of Zeroization. POWER_ON_RESET_N signal can be used in the user design as a system power-on-reset for the FPGA fabric. It is an active Low-output signal.

The POWER_ON_RESET_N signal is available by instantiating the SYSRESET macro (see [Figure 3](#)), from the Libero SoC IP catalog into SmartDesign or by instantiating it directly inside HDL file.

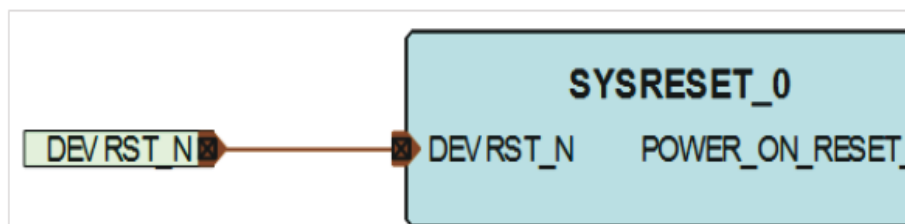


Figure 3: SYSRESET Macro

15. What does a mirrored master or mirrored slave port mean?

The mirrored interfaces are complementary interfaces located in the CoreAHB/APB that allow AHB/APB bus masters to connect to AHB/APB slaves through the CoreAHB/APB. The AHB/APB master port gets connected to the mirrored master port on the CoreAHB/APB, and the slave ports get connected to the mirrored slave ports on the CoreAHB/APB. In short, the mirrored ports are same ports as the normal interfaces but the directions of these ports are reversed.

16. Why is SPLL used for in PCIe?

The SPLL is used to re-time the bridge interface between the fabric and the hardened blocks of the SERDESIF.

17. What is the source for the SPLL clock in SERDES?

CLK_BASE is the input reference clock (source) of the SPLL.

18. Which clock is used for the AHB buses in PCIe?

The SPLL output is used as the AXI/AHB bridge clock.

19. Can fabric clock be used as reference clock in EPCS mode (In SERDES IP)?

Yes, fabric clock can be used as reference clock in the EPCS mode.

20. Is the "Repair minimum delay violation" option for the router supported for SmartFusion2 device?

This option is currently not supported for the SmartFusion2 device.

21. Is it possible to get SmartFusion2 symbol and footprint files for Altium?

Altium tool foot print and symbols are currently not available for Smartfusion2 device.

22. Does the SERDES simulation model have a feature to reduce simulation run times?

Presently, there is no option to bypass the clock and data recovery logic to reduce the simulation run time.

23. Can the SERDES IP simulation model be used for simulating a PCIe system?

Yes. BFM model can be used where SERDES acts as AXI/AHB bus master and slave. However, serial protocol is not implemented in this case.

24. Is simulation of serial behavior of SERDES IP supported?

Yes, it is supported. For all SERDES modes, full RTL model is used to simulate the SERDES serial behavior.

25. How are SmartFusion2 hardware blocks initialized?

SmartFusion2 hardware blocks are initialized through a combination of flash bits and Libero generated logic (CoreConfigP).

26. How does cache controller improve the execution time?

For details on improving the execution time using Cache Controller, refer to the [SmartFusion2 SoC FPGA - Cache Controller Configuration](#) application note.

27. What is Zeroization and is it supported by SmartFusion2 device?

Zeroization is a system service that destroys the sensitive data in the device and then verifies that the data is gone before allowing any further operations to take place. Yes, SmartFusion2 SoC FPGAs support Zeroization.

28. How to use MSS clock conditioning circuit (CCC)?

Run the following steps:

- Instantiate the SmartFusion2 MSS component into your Libero SoC project.
- Configure (enable/disable) the MSS components appropriately for the application needs using MSS configurator.
- Configure the MSS CCC input and output clock frequencies using the MSS_CCC configurator.
- Set the MPLL analog supply voltage to 2.5 V or 3.3 V to match the supply on the board.

29. Does Microsemi have plans to support lower core voltage parts?

Currently, SmartFusion2 works on 1.2 V core voltage. We are planning for 1.0 V core voltage support in future.

30. Can SmartFusion2 support USB OTG and what type of USB is supported?

Yes, SmartFusion2 device supports USB OTG. The following USB flash drives are currently supported:

- Sandisk Cruzer Blade™ - 16 GB/8 GB/4 GB/1 GB
- Kingston DataTraveler® - 4 GB/2 GB
- Kingston® DataTraveler®109 - 8 GB
- Transcend JetFlash® - 4 GB

31. How should unused SERDES pins/power supplies on SmartFusion2 device be connected on the board?

Refer to the [Knowledge Base Article](#) to know about handling unused SERDES pins.

32. Do blank devices have ramp rate? What is the default ramp rate?

No, the blank devices do not have default ramp rate values.

Note: The 50 us, 1 ms, 10 ms, and 100 ms ramp rates are not applicable for blank devices, and they are valid only for the programmed devices.

33. What is the percentage deviation from power calculator values with the actual silicon results?

The deviation percentage from power calculator with the actual silicon results is less than 10%.

34. What is the default toggling rate used by power calculator to calculate the power?

The power calculator engine uses inputs at 12.5% toggle rate and provides the power estimation.

35. How to configure PCIe address parameter of SERDES configurator?

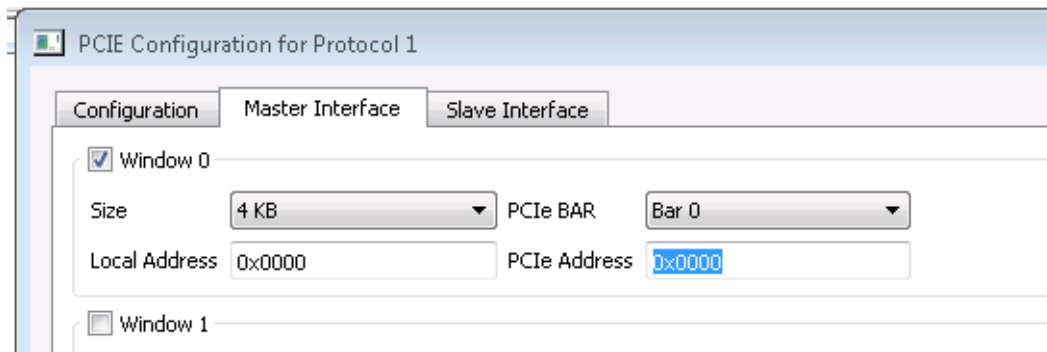


Figure 4: PCIe Configurator

PCIe address is mapped to bits [31:12] (LSB of Base address AXI Master WindowsX_2) and bits [31:0] (MSB of Base address AXI Master WindowsX_3). The zeros in these fields indicate the offset.

Table 1: AXI_MASTER_WINDOW Registers

Bit Numbers	Name	Description
[31:12]	AXI_MASTER_WINDOWx[0]	Base address AXI3 master window x
[11:0]		Reserved
[31:12]	AXI_MASTER_WINDOWx[1]	Size of AXI3 master window x
[11:1]		Reserved
0		Enable bit of AXI3master window x
[31:12]	AXI_MASTER_WINDOWx[2]	LSB of base address PCIe window x
[11:6]		Reserved
[5:0]		These bits set the BAR. To select a BAR, set the following values: 0*01: BAR0 (32-bit BAR) or BAR0/1 (64-bit BAR) 0*02: BAR1 (32-bit BAR) only 0*04: BAR2 (32-bit BAR) or BAR2/3 (64-bit BAR) 0*08: BAR3 (32-bit BAR) only 0*10: BAR4 (32-bit BAR) or BAR4/5 (64-bit BAR) 0*20: BAR5 (32-bit BAR) only
[31:0]	AXI_MASTER_WINDOWx[3]	MSB of base address PCIe window x

For example, If the PCIe address value is set to be 0x1000 in the GUI, then the BAR0 address + 0x1000_000 is mapped to 0x0 of AXI window.

36. Are IBIS models different for SmartFusion2 and IGLOO2?

IBIS models are identical for SmartFusion2 and IGLOO2 given package.

37. How to set seed value for SmartFusion2/IGLOO2 place and route?

For example, set a seed value of 6 for place and route.

The 'extended_run_lib' Tcl script enables you to set the starting seed value in batch mode from a command line prompt.

To set a seed value of 6,

```
<prompt>C:/Microsemi/Libero_v11.3/Designer/bin/libero.exe script:C:/Microsemi/
Libero_v11.3/Designer/scripts/extended_run_lib.tcl logfile:extended_run.log
"script_args:-root F:/SF2_seed/seed_check/designer/top -n 3 -starting_seed_index 6 -
slack_criteria tns -stop_on_success"
```

Refer to the [Libero Tcl Commands Reference Guide](#) for more information.

Here,

- C:/Microsemi/Libero_v11.3/Designer/bin/libero.exe = Libero installation directory
- C:/Microsemi/Libero_v11.3/Designer/scripts/extended_run_lib.tcl = Scripts file location in the Libero installation directory
- F:/SF2_seed/seed_check/designer/top = Root module location under designer directory in Libero project

38. What does the below RGB error message mean, which is observed during place and route?

```
Error: RGB: Cannot place all RGB's in row 60.
```

RGB stands for row global buffer. The error message indicates that the particular row of FPGA runs out of global resources. Change or edit the placement constraints provided in the PDC file. Refer to the [SmartFusion2 Clocking Resources User Guide](#) for more information.

39. Are basic blocks available for SmartFusion2 and IGLOO2?

Basic blocks are not available for SmartFusion2 and IGLOO2.

40. How to enable system timers or MSS timers?

System timers or MSS timers are enabled by default, refer to Chapter 18 in [MSS User Guide](#) for more information.



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