SmartFusion2 Silicon FAQs

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Microsemi

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1. Where can I find Flash*Freeze information for SmartFusion2?

Refer to *SmartFusion2 SoC FPGA Low Power Design User Guide* for information on Flash*Freeze.

2. What is the recommended FlashPro programmer for SmartFusion2?

Use FlashPro 4 to program SmartFusion2.

3. Where can I find information about handling unused I/Os/pins?

Refer to the following links for handling unused I/O pins:

For pin descriptions, refer to the *SmartFusion2 Pin Descriptions* document.

For board design guidelines, refer to the *SmartFusion2 Board Design Guidelines* application note.

4. What is the MSL level for M2S050TS-FG484I and M2S050TS-FG896I?

M2S050TS-FG484I and M2S050TS-FG896I are rated MSL-3.

These are plastic molded BGA packages. The first-level interconnection method is wire bonding. It uses SAC305 solder ball material for lead-free (FGG package code) and uses SnPb for leaded solder ball (FG package code).

5. Where do I get information on SmartFusion2 dedicated global I/O naming conventions?

Refer to the *SmartFusion2 Pin Descriptions* document to understand the I/O naming conventions.

6. What is the state of the SmartFusion2 I/O's during RESET?

All I/O's are held in high-impedance state. Refer to the "Power Supply Sequencing and Power-On Reset" section of the *SmartFusion2 System-on-Chip FPGAs* datasheet.

7. What is the recommended crystal oscillator for SF2?

Refer to the *Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGA* application note for details on the recommended crystal oscillator.

8. What if scenario: PLL is connected to 3.3V on board and is set to 2.5V during configuration in Libero software?

The behavior is unpredictable and it is not recommended to use this scenario.

9. Where can I find SmartFusion2 security and anti-tamper information?

Brief Information:

Anti-tamper countermeasures in SmartFusion2 are intended to address various types of attacks including non-invasive, semi-invasive and invasive attacks.

Secret factory and user design security keys are stored in encrypted form in specially designed security flash arrays using a unique-per-device encryption-key. Pass codes are stored in hashed form, so even if discovered could not be used to unlock a device.

Selected models have the ability to detect and report certain tampering events. This information can be used to command the device to zeroize (destroy) all sensitive stored data.

For more information, refer to *SmartFusion2 SoC FPGA Reliability and Security User Guide*.

10. What are Theta JC values for M2S050T-FG484 and FG896?

Table 1: **Package Thermal Resistance**

Product	θJA			θJB	θJC	Units
	Still Air	1.0 m/s	2.5 m/s			
M2S050T - FG896	14.7	12.5	10.9	7.2	4.9	°C/W
M2S050T - FG484	15.3	12.2	11.0	6.3	3.2	°C/W

11. What are the 'ramp rate' settings in SmartFusion2 design tools and what are the available values?

The power-on reset circuitry in SmartFusion2 devices requires the VDD and VPP supplies to ramp monotonically from 0 Volts to the minimum recommended operating voltage within a predefined time. This is termed as ramp rate.

Following four our ramp rate options are available: 50 us, 1 ms, 10 ms, and 100 ms.

Each selection represents the maximum ramp rate to apply to VDD and VPP.

12. What is the frequency range of SmartFusion2 Fabric CCCs?

SmartFusion2 Fabric CCC ranges from 20 MHz to 400 MHz.

13. What is the Significance of Auxiliary crystal oscillator?

Auxiliary (RTC) Crystal Oscillator

SmartFusion2 devices, except M2S050, have an auxiliary crystal oscillator dedicated to RTC clocking as an alternative source for a 32 KHz clock. The RTC can generate a real-time clock by taking the 32 KHz clock as input from the auxiliary crystal oscillator when the main crystal oscillator is being used for another purpose.

Similar to the main crystal oscillator, the auxiliary crystal oscillator works with an external crystal, ceramic resonator, or an RC circuit to generate a high precision clock in the range of 32 KHz to 20 MHz. There are two I/O pads for the auxiliary crystal oscillator-EXTLOSC1 and XTLOSC1-for providing an input. These I/O pads can be connected to a crystal, ceramic resonator, or an RC circuit. The output frequency range, operating modes, and characteristics for the auxiliary crystal oscillator are the same as those for the main crystal oscillator.

14. What is the Differential-Impedance between the SOLDER-BALLS (measured at the solder-balls) of device?

The differential impedance ranges from 95 to 100 ohm.

15. Can FMC connector be used for connecting 3.3V I/Os?

It is not possible to use the 3.3V I/Os with FMC connector.

16. What is the state of clock conditioning circuit (CCC) in Flash*Freeze mode?

CCCs are not operational. CCCs are turned off during Flash*Freeze mode. The CCC configuration retains its state during Flash*Freeze operation and recovers the previous state upon Flash*Freeze exit.

17. What is the state of mathblocks in Flash*Freeze mode?

Mathblocks are not operational. They are turned off during Flash*Freeze mode. A mathblock configuration retains its state during the Flash*Freeze operation and recovers the previous state on Flash*Freeze exit.

18. What are the LVDS I/O types supported in SmartFusion2 other than SERDES?

Table 2 lists the LVDS supported in different I/O types:

Table 2: **LVDS Support**

	MSIO	MSIOD	DDRIO
LVDS 3.3V	Yes	No	No
LVDS 2.5 V	Yes	Yes	No

For more information about different I/O standards supported by SmartFusion2, refer to *SmartFusion2 SoC FPGA Fabric User Guide*.

19. What is Pre-Emphasis?

Pre-Emphasis refers to a system process designed to increase the magnitude of transitions in LVDS signal in order to achieve higher speeds by compensating for lossy transmission medium. This feature is configured inside the LVDS I/O. It can be enabled or disabled for output signals, and this is available with MSIOD I/O pins only. If you select MSIOD pin and select LVDS as I/O standard then you can enable/ disable the Pre-Emphasis option as shown below.

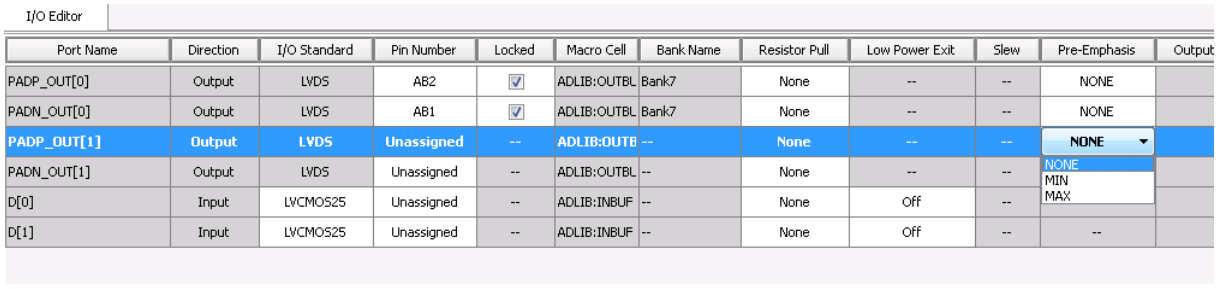

Figure 1: **Enable/Disable Pre-Emphasis Option**

The following table shows the different values when the Pre-Emphasis is set to 'NONE', 'MIN', 'MED'.

Table 3: **Different Values when Pre-Emphasis is set to NONE, MIN, MED**

	t_{DOUT}		t_{ENZL}		t_{ENZH}		t_{ENHZ}		t_{ENLZ}		
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	Units
LVDS (for MSIO I/O bank)	2.294	2.698	2.493	2.933	2.459	2.892	2.553	3.003	2.519	2.962	ns
LVDS (for MSIOD I/O bank)											
No pre-empahsis	1.765	2.076	1.963	2.31	1.914	2.251	2.063	2.428	2.014	2.369	ns
Min. pre-emphasis	1.666	1.961	1.966	2.313	1.914	2.252	2.066	2.431	2.014	2.37	ns
Max. pre-emphasis	1.616	1.902	1.969	2.317	1.917	2.255	2.069	2.435	2.017	2.373	ns

Notes:

- No pre-emphasis represents 'NONE' in the Pre-Emphasis tab of I/O editor
- Min pre-emphasis represents 'MIN' in the Pre-Emphasis tab of I/O editor
- Max pre-emphasis represents 'MED' in the Pre-Emphasis tab of I/O editor

20. What is the size of eSRAM in SmartFusion2?

The size of eSRAM in SmartFusion2 is:

- 2 x 32kB (optional EDAC support)
- Additional 8kB (in non-EDAC mode)

21. What types of memories are supported by MDDR/FDDR controller?

SmartFusion2 has supports up to 4GB of external DDR:

- DDR2/DDR3/LPPDR
- Configurable data widths
- x32 (Full bus width - without EDAC)
- x36 (Full bus width - with EDAC)
- x16 (Half bus width - without EDAC)
- x18 (Half bus width - with EDAC)

22. Is Trimode Ethernet supported in SmartFusion2?

Yes.

Details:

- 10, 100, 1000 mode
- Built-in DMA, Performance Monitors
- 8K Byte Receive FIFO
- 4K Byte Transmit FIFO

23. What is Flash*Freeze entry time?

The time taken from the initiation of Flash*Freeze trigger to disabling of the clock is known as Flash*Freeze entry time.

24. What features of USB are supported in SmartFusion2?

The following features are supported:

- HS USB OTG
- Device mode: Mass Storage, HID, & CDC (Serial Communication Only)
- Host mode: Mass Storage

25. How many channels does PDMA support?

PDMA implements eight DMA channels performing the data transfers to/from peripherals/memory independent of Cortex-M3 processor.

26. Does Smartfusion2/IGLOO2 PCI buffer compliant with the PCI AC overshoot/ undershoot specification?

The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/ undershoot specifications. Refer to the *SmartFusion2 datasheet* for more information.

27. What are overshoot/undershoot limits for the AC signals?

For AC signals, the input signal is in undershoot limit during transitions to -1.0V for no longer than 10% of the period. The power supply passes through AC signals during the transition must not exceed 100mA.

For AC signals, the input signal is in overshoot limit during transitions to VCCI + 1.0V for no longer than 10% of the period. The power supply passes through AC signals during the transition must not exceed 100mA.

28. Does MSS MAC get powered-up during Flash*Freeze?

The MSS MAC uses fabric I/Os' which are not powered-up during Flash*Freeze.

29. Are SmartFusion2 050 and 090 pins compatible?

No, they are not compatible. Refer to the *AC404 Application Note* for more information.

30. What is the moisture sensitivity level of FCS325 package, per IPC/JEDEC J-STD-020?

The moisture sensitivity level of FCS325 package per IPC/JEDEC J-STD-020 is MSL3.

31. Is an external brown-out detection(BOD) circuit recommended? Why?

Yes, the external BOD circuit is recommended for brown-out detection.

If the external BOD circuitry is not provided, then any VDD value which is below datasheet limits results in an unexpected functional behavior. This behavior may persist even after the supplies are back. Refer to the *SmartFusion2 and IGLOO2 Board Design Guidelines Application Note* for more information on Brown-out Detection.

32. Where to find Package Mechanical Drawings?

Package Mechanical Drawings

33. Why cannot the Pin D18 of M2S050 be used as a fabric output pin on VF400 package?

The pin number D18 is a special pin. It is listed as MSI46NB1/MMUART_0_TXD/GPIO_27_B in the Pin Assignment Table of *SmartFusion2 Pin Description*. It is a bi-directional pin by nature, but if the MSI46NB1 feature is used, then it can only be configured as a input pin. Also, it cannot be configured as differential, refer to the *SmartFusion2 Pin Descriptions* on page 7.

34. How many fabric interface controllers (FICs) are present in each of the SmartFusion2 devices?

Table 4 lists the FICs in the SmartFusion2 device:

Table 4: **FICs in SmartFusion2 Devices**

Feature	M2S005	M2S010	M2S025	M2S050	M2S090	M2S150
Fabric Interface Controller	1	1	1	2	1	2

35. What are VPP voltage requirements for different SmartFusion2 devices?

VPP can be 2.5 or 3.3 for devices such as M2S005, M2S010, M2S025, and M2S050, higher density SmartFusion2 devices such as M2S090 etc, require only VPP 3.3V.

36. Is an external termination required for LVDS I/O?

The external termination is not required for LVDS I/O inputs, however, it is recommended for outputs.

37. What is the maximum baud rate for SmartFusion2 MMUART?

The tested baud rate is 115200bps for SmartFusion2 MMUART, but the PHY supports up to 12Mbps for SmartFusion2 Development Kit Board as per specifications.

38. Does real time counter (RTC) have a battery backup?

The RTC does not work after powering off the device as it lacks a battery input and low power oscillator. But a default value is provided to the RTC in SmartFusion2 so that it keeps counting from that value. Refer to the *SmartFusion2 Microcontroller Subsystem User Guide* for more information.

39. Does failed integrity check trigger SmartFusion2 self-recovery from golden image?

Auto programming does not get started automatically. The FLASH_GOLDEN pin is required to assert the auto programming mode.

40. Do similar packages of IGLOO2 and SmartFusion2 have pin compatibility?

Yes, the similar packages of IGLOO2 and SmartFusion2 are pin compatible.

41. What is the adapter module that is used to program M2S010 device in FG484 package?

The SM2S-484FG adapter module is used to program M2S010 device in FG484 package.

42. What is proper termination of JTAG signals (TDI, TDO, TMS, TCK, and TRST) on the IGLOO2/SmartFusion2 FPGAs? Should they be pulled up or down and what value of resistor should be used?

Refer to the *IGLOO2 Programming User Guide* for JTAG pins related information.

Table 5: **JTAG Pin Names and Descriptions**

Name	Direction	Termination	Description
JTAGSEL	Input	Pull to JTAG power supply via 1 K	JTAG controller selection. If JTAGSEL is pulled high, an external TAP controller connects to the System Controller TAP using JTAG interface. This is recommended for setup programming.
JTAG_TCK	Input	Pull to JTAG power supply through 500 Ohm to 1 K or tie to GND directly	Clock input to JTAG controller. The TCK pin does not have an internal pull-up/pull-down resistor. If JTAG is not used, Microsemi recommends tying it off. The tied off resistor should be placed close to the FPGA pin. This prevents totem-pole current due to random oscillations on the input buffer and operation in case TMS enters an undesired state.
JTAG_TDI	Input	Not required	Serial data input to JTAG controller Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
JTAG_TDO	Output	Not required	Serial data output from JTAG controller. Serial output for JTAG boundary scan, ISP, and UJTAG usage. The TDO pin does not have an internal pull-up/-down resistor.
JTA_TMS	Input	Not required	The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, and TRSTB). There is an internal weak pull-up resistor on the TMS pin.
JTAG_TRSTB	Input	Tie to GND via 1 K	Reset pin for JTAG controller. The TRSTB pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TSRTB pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in Reset mode. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, Microsemi recommends tying off TRSTB to GND through a resistor placed close to the FPGA pin.

43. What is the termination network of SERDES reference clock receiver?

The reference clocks (REFCLKs) are MSIOD input buffers. The REFCLKs has an on-die programmable termination structure as a generic MSIOD, refer to the *Fabric User Guide* for more information.

44. What is the performance of AES engine in SmartFusion2/IGLOO2?

Following is the performance details for AES-128/256 small and large message sizes of AES engine:

- AES128: 220us + 135us per 128-bit block
- AES256: 290us + 135us per 128-bit block

After receiving the AES encryption command, the AES engine initially takes 220 us (AES128) and 290 us (AES256) to get initialized and then 135 us to process 128-bit block.

- Time taken to process the number of blocks = Number of blocks X 135 us

45. What is the flame retardant performance of M2S090 device?

Flammability offered for three packages (that are, FG484, FG676, and FCS325) of the M2S090 device is a UL-94 rating of V-0.

46. Are System Controller SPI pins tri-stated (high impedance) during reset?

The System Controller SPI pins such as SC_SPI_SS, SC_SPI_CLK, SC_SPI_SDO, and SC_SPI_SDI are set to floating when DEVRST_N is asserted.

47. Are all the programming interfaces disabled permanently when SmartFusion2 is set to the permanent flashlock (OTP) mode? Does OTP mode affect only the specific programming interface?

The OTP mode disables all the programming interfaces.

48. Are all the I/O bank VSS pins tied together on the die? Yes, all the I/O bank VSS pins are tied together on the die.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Date	Changed Chapters	List of Changes
16 December 2014	Revision 2	Removed all instances of and references to M2S100 devices from Table 4 (SAR 62858).
05 July 2014	Revision 1	First Release.

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