



Microsemi Corporation

October 9, 2013

Product Change Notification No:1309

Change Level: Minor

Subject: Synopsys Synplify Pro Software Bug Regarding Safe State Machine Recovery

Dear Customer,

This notification provides information on a synthesis software bug affecting the state machine recovery for all FPGA family designs where the safe state machine synthesis attribute was enabled (*syn_encoding=safe*).

This bug affects every release of Synopsys Synplify that supported the “safe” option for *syn_encoding attribute* until it was fixed in:

Microsemi Edition versions:

H-2013.03M-1 released in June 2013

G-2012.09A-SP3 released in June 2013

All-Vendor version:

H-2013.03-SP1 released in June 2013

Description of the Problem:

When a design is synthesized with the “safe” state machine encoding style, Synplify Pro is expected to implement the state machine with the default encoding and infer extra logic to force the state machine into a reset state—if it gets into an illegal state. However, if this bug affects the design, the extra logic is not inferred and the state machine will not go into a reset state. This problem can occur only when *all* of the following conditions are true:

- The design is synthesized with the “safe” encoding style for the state machine (the user has specified *syn_encoding=safe*).
- The state machine in the design uses the synchronous reset registers.
- The Synopsys Compiler erroneously optimized part of the next-state logic leaving no reset state for the state machine to recover, or a user error was made that did not specify the reset state in the RTL code.

Method of Identifying an Affected Design:

This problem cannot be detected with a simple simulation test bench. It will be seen if the designer forces the state machine into an illegal state during simulation and observes the state machine unable to recover. You can verify whether this issue really affected your design by checking if *all* of the following conditions are true for the Synplify project, where the design was synthesized:

1. The *syn_encoding attribute* is set to "safe."
2. The FSM Compiler is ON.
3. Synplify Pro extracts an FSM (RTL view, .srs, shows the state machine symbol for FSM).
4. The state machine has synchronous reset specified in RTL along with the reset state.
5. The encoding style and state assignment for this state machine is such that there exists an invalid state. This is always true with one-hot encoding.
6. The safe state machine logic does not exist, which can be verified by:

Search for the register instance *<state_machine_instance_name>_illegalpipe* in the EDIF netlist. If the register instance is NOT present, the design is affected by this bug.

OR

Open the technology view in the HDL analyst and search for the *<state_machine>_illegalpipe* instance. If the instance is NOT present, the design is affected by this bug.

Solution:

Microsemi recommends that all new designs use the latest software below:

Synplify Pro ME H-2013.03M-1 and later includes the fix for this bug. Additionally, it generates an error message if the reset state wasn't specified in the RTL code for such cases. This release is available standalone and is also included with the Libero SoC v11.1. This software supports our newer flash devices and can be downloaded from the Microsemi website:

<http://www.microsemi.com/fpga-soc/design-resources/design-software/synplify-pro-me#downloads>.

Synplify Pro ME G-2012.09A SP3 includes the fix and supports our antifuse and legacy flash devices. Additionally, it generates an error message if the reset state wasn't specified in the RTL code for such cases. This is available standalone for use with the Libero IDE. This software can be downloaded from the Microsemi website:

Windows:

http://soc.microsemi.com/download/reg/download.aspx?p=f=SynplifyProME_G201209A-SP3_WIN

Linux :

http://soc.microsemi.com/download/reg/download.aspx?p=f=SynplifyProME_G201209A-SP3_LIN.



Contact Information:

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Regards,

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