Libero SoC v11.1 SP2 Release Notes

Libero SoC v11.1 SP2 delivers full support for IGLOO2 FPGAs and SmartFusion2 SoC FPGAs. This service pack must be installed over Libero SoC v11.1 or v11.1 SP1.

Contents

Supported Families

IGLOO2, SmartFusion2, SmartFusion, Fusion
ProASIC3, ProASIC3E, ProASIC3L
IGLOO, IGLOOe, IGLOO+

IGLOO2 Device Support

M2GL150, M2GL150T, M2GL150TS, M2GL150S	1152 FC
M2GL100, M2GL100T, M2GL100TS, M2GL100S	1152 FC
M2GL050, M2GL050T, M2GL050TS, M2GL050S	400 VF, 484 FBGA, 896 FBGA
M2GL025, M2GL025T, M2GL025TS, M2GL025S	400 VF, 484 FBGA
M2GL010, M2GL010T, M2GL010TS, M2GL010S	400 VF, 484 FBGA
M2GL005, M2GL005S	484 FBGA

SmartFusion2 Device Support

M2S150, M2S150T, M2S150TS, M2S150S	1152 FC
M2S100, M2S100T, M2S100TS, M2S100S	1152 FC
M2S050, M2S050T, M2S050TS, M2S050S	400 VF, 484 FBGA, 896 FBGA

M2S025, M2S025T, M2S025TS, M2S025S	400 VF, 484 FBGA
M2S010, M2S010T, M2S010TS, M2S010S	400 VF, 484 FBGA
M2S005, M2S005S	484 FBGA

Programming Support

Programming file generation is enabled on Windows OS for these devices.

SmartFusion2

M2S050, M2S050S, M2S050T, M2S050TS
M2S025, M2S025S, M2S025T, M2S025TS
M2S010, M2S010S, M2S010T, M2S010TS
M2S050T_ES

IGLOO2

M2GL050, M2GL050S, M2GL050T, M2GL050TS
M2GL010, M2GL010S, M2GL010T, M2GL010TS

What's New

IGLOO2 and SmartFusion2 Enhancements

Programming Support

Programming file generation is enabled on Windows OS for SmartFusion2 M2S025, M2S025S, M2S025T, and M2S025TS

I/O Register Combining through PDC

The I/O modules of SmartFusion2 and IGLOO2 have dedicated input, output and enable registers. You can use the '*set_io'* PDC command to set constraints in your design, which will enable packing of the input and output registers in to the I/O module.

Using the PDC file a register directly connected to an I/O can be combined into the I/O module assuming the I/O Register combining rules are met. The set_io PDC command has been extended with –register, –in_reg, –out_reg and –en_reg parameters.

For more details, please read set_io (Smartfusion2 and IGLOO2) under PDC Command Reference in Libero SoC Online Help.

Infer CLKBUF to Reduce Clock-insertion Delays

For SmartFusion2 and IGLOO2 families, Libero automatically optimizes the connection of an I/O driving a global network (CLKINT) to reduce the clock-insertion delay. The I/O to GB Connections section in the Global Net report will mark the Net Type as HARDWIRED when the optimization is feasible.

Automatic Pin Reports

For SmartFusion2 and IGLOO2 families, Pin reports are automatically created after Layout both by pin name and by pin number. These reports are updated as you commit changes from the I/O Editor, or rerun Compile.

IO Editor Physical Package View

This view shows the physical package with all the pin locations. You can drag and drop pin assignments or configure the banks.

Enhanced DDR Configurator

The DDR Configurator, accessible through System Builder and SmartDesign, has been redesigned and enhanced. Valid configuration values for the DDR Controller parameters are specified in the General page, Memory Initialization page and Memory Timing page.

You can use the Import feature to import a Register file created with a previous release.

SmartPower UI Supporting Large Devices

A Graphical User Interface is now available for use with the larger SmartFusion2 and IGLOO2 150/100 devices. Design tools for these devices require a 64-bit OS.

SmartFusion2 and IGLOO2 150/100 Pre-silicon Timing Update

FlashPro Lite Parallel Port Driver for Win7 64-bit OS

FlashPro Lite is available for Programming ProASIC^{PLUS} devices

Updating your SmartFusion2 Design from v11.0 to v11.1

All SmartFusion2 designs created using Libero SoC v11.0 must be updated using Libero SoC v11.1 before programming production silicon.

1. When the v11.0 project file opens in v11.1, the Convert Project dialog box displays with an option to back-up your existing design. Check the box to Create a backup of your original project.
2. Click **OK**. Your design will be invalidated.
3. Follow the instructions in the tools to update your design using the latest cores.
   - Download all new cores available. Select **View > Windows > Catalog** and click **Download them now**.
   - For SmartDesign, update all instantiated components and cores to the latest versions available in the Libero Catalog.
   - Do not open System Builder components as a SmartDesign. Double-click to open the System Builder, proceed through all the pages and re-generate. There is no notion of replace for System Builder cores.
   - After all component and core instances are updated to the latest versions, check the configuration of each core before generating the design.
   - Open the Design Firmware window and download all the latest Firmware. Select the new version of each Firmware core and the **Download Required** dialog box appears. Click **Yes** to download the Firmware core.

   Pay particular attention to the PLL message displayed after your project is updated:

   ```
   Info: Project is updated. All PLL supply voltages must be sourced
   from a single Supply Voltage. Use the Project Settings dialog box to
   verify that your global PLL Supply Voltage is set correctly.
   ```
4. Regenerate your design.
5. Check that your constraint files are properly organized and that the tool options are correct.
6. Continue through the design flow.

Resolved Issues

Issues Fixed in v11.1 SP2 that were reported in previous Release Notes

SAR 42451 - Programming Tcl commands in the Libero flow do not work in batch mode.

SAR 43530 - SmartFusion2 M2S050T_ES must be enabled after other devices in a chain.

SAR 45419 - Linux: SmartTime is unable to launch the web browser to display Help.

SAR 46814 - The Placer ignores timing paths that go through a BIBUF (bidirectional I/O) if the path includes clock-to-input or clock-to-output constraints.

SAR 46845 - The setup analysis fails to use the clock source latency constraint for ProASIC3 and IGLOO families.

SAR 47395 – Automatic I/O register combining for SmartFusion2 and IGLOO2 issue resolved.

SAR 47963 - Incorrect values for Input and Output Delay are entered automatically when external Setup and Hold values are entered in the Constraints Editor.

SAR 50472 - Simulations for IGLOO2 designs containing HPMS DDR or SERDES fails for M2GL005, 010, and 025 devices.

SAR 50761 – In 11.1 SP1 you cannot generate a programming file for the M2S050_ES device that has security features.

Fixed Customer Reported SARs in the v11.1, SP1 and SP2 Releases

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

Resolved SARs in Libero SoC v11.1 SP2 Release

SAR	CASE	PRODUCT	SUMMARY
48265	493642-1379027302	Designer	Added EPCS Support for custom speed
47180	493642-1285352776	Designer	The min-delay repair feature is enabled along with high-effort routing on the A3PE3000/L devices.
43941	493642-1193065892	Project Manager	Pin report will be generated anytime the pins are affected (compile, Layout, MVN). The pin report will be present at the level of the datasheet under the root in the report.
44132		Project Manager	Improve file handling when HDL type is modified
48232	493642-1343942365 493642-1378862259	Timing	Properly initialize timing analysis to retrieve best case, with or without EMD, from SDF writer.

Resolved SARs in Libero SoC v11.1 SP1 Release

SAR	CASE	PRODUCT	SUMMARY
48656	493642-1362924708	Designer	Corrected a problem where adding max delay constraints substantially increased the amount of runtime required by the Placer
48404	493642-1347533092	FlashPro	FlashPro fixed to allow reprogramming of a secured device
48814	493642-1356097722	Help	USB: ULPI XCLK should be shown as only Input
47670	493642-1328020900	Help	SmartFusion2 Macro Library Guide correction

48828	493642-1336172062	Power	Corrected deviation between SmartPower estimations and real power measurements
46688	493642-1286695158	Project Manager	Fixed Libero Linux crash when LC_ALL is set to "C"
48604	493642-1360357320	Timing	Fixed the Auto-Generated Constraints Multiplier/Divider values mismatch with MSS_CCC Configurator
48515	493642-1355056818	Timing	Fixed Tcl command st_expand_path to generate the proper report format

Resolved SARs in Libero SoC v11.1 Release

SAR	Case Number	Product	Summary
46996 47513	493642-1298148007 493642-1318150504 493642-1311141474	Microcontroller Subsystem	Eliminated SoftConsole debugger DAPReadRange failed error when ENVM DS client placeholder is used.
46964	493642-1298303954	Microcontroller Subsystem	Fixed cause of Compile error: This design has an MSS configured to use an external 32Khz RTC XTL. This device has only one XTL which is shared with the fabric and the configuration of the XTL is not matching.
45912	493642-1260871847	Project Manager	Fixed cause of Compile error: MSS Connectivity: Incorrect fan-out 9 for pin
44142	493642-1176543702	Project Manager	Fixed exported Tcl commands that did not execute.
47716	493642-1328708170	SmartTime	Fixed generate clock constraint mapping when the master clock is not known (differential i/o, gated clocks, etc.). Allows the master clock to be found later when the clock is added.
39878	493642-1202183800	Synplify Pro	Added TMR support for SmartFusion2 and IGLOO2 designs.
32302	493642-47063910 493642-1265247710	Timing	Exported SDC for the external setup/hold constraints does not match what is set in UI.
46978	493642-1110045502	SmartFusion Layout	Added A2F500 message. Warning: PLC503: Instance CLKINT_0/U_CLKSRC/U_GL is using the A2F500M3G fabric CCC/PLL GLA output. This resource is using the glitchless mux (NGMUX) connected to the GLA output of the fabric CCC/PLL. In order for the NGMUX to operate correctly, the signal driving this instance must be a free-running clock signal. Refer to SmartFusion Microcontroller Subsystem User Guide for more details. Verify that this signal is a continuous clock signal.

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the InstallShield Wizard displays a message stating "The installation of Microsoft Visual C++ 2005 SP1 Redistributable Package (x86) appears to have failed. Do you want to continue the installation?" Select **Yes** and the installation will complete successfully.

SmartFusion2 and IGLOO2

For IGLOO2 projects do not use the following cores from the Catalog. Use System Builder.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

IBIS models cannot be generated within Libero SoC. Please download them from our web site.

Block Design will be supported in a future release.

SAR 48448 - Zeroization will be available in a future release.

SAR 46571 - M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

Libero

SAR 41668 – SW Update Check window opens in full screen; cannot see buttons.

Workaround: Double-click in the header section of the window and it will redisplay correctly.

SAR 50267 – In Fusion Advanced Analog System Options dialog, selecting SMEV RAM degrades the Resolution performance.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI.

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block.

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows.

This issue will be fixed in a future release.

SAR 42954 - Not all remote cores are visible in the Catalog after switching to a new vault.

Workaround: Reload the Catalog after switching to a new vault. Select the **Settings** icon in **Catalog** and choose **Reload Catalog**.

SAR 46334 – Ordering of PDC files may be incorrect after using the ChipPlanner.

Workaround: The ChipPlanner generates a *_fp.pdc file using the design name by default. PDC files are automatically organized alphabetically, which may not be the order that you want them applied. Prior to running Layout review the order of your PDC files by right-clicking **Compile** to open the **Organize Constraints** dialog. Reorder the *_fp.pdc files as required.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 49693 - Changing the default I/O technology in Project Settings should invalidate Compile and Layout.

After changing the I/O technology you must recompile for the changes to take effect.

SAR 50580 - Serdes configurator does not retain values for certain registers.

This issue will be fixed in a future release.

SAR 49044 –Linux error when using MVN can be ignored.

The following messages are displayed on the Linux terminal when the Floorplan Constraints Editor is opened.

```
Start Server 1
Start Server 2
Failed to open Def Table: 9
Failed to open Def Table: 8
Failed to open Def Table: 12
Running in orphan mode!
```

The following message appears on exiting MVN and a core file is created:

```
…/bin/mvn: line 69:  1675 Segmentation fault
(core dumped) "$exedir/../lib/$exename" "$@"
```

SmartTime

SAR 34365 - Asynchronous Register paths are not displayed in Timing Analysis view.

This issue will be fixed in a future release.

SAR 43095 - In the Domain Browser of the Analysis window, Edit Clock for a Generated Clock does not open the Edit Clock dialog box.

Workaround: Open the Constraint Editor tool to edit the generated clock constraint.

SAR 43767 – Maximize Window button is missing from the title bar for Constraints Editor, Max Analysis and Min Analysis

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

Synthesis

SAR 42808 - Warning: Unrecognized option ignored: "-_include"

When Synplify Pro is invoked through Libero and the design has RTL with “-_include” <file_name>, the following option is added in the *.prj file:

```
add_file -_include <file_name>
```

Synplify Pro issues this message:

```
Warning: Unrecognized option ignored: "-_include"
```

This warning message can be ignored. The synthesis tool will locate the file in the Libero project /hdl folder.

SAR 46982 - Synplify Pro treats the PLL as a black box.

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the create_clock and create_generated_clock constraints. More information can be found in KI70291.

SAR 46983 - False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro.

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

```
Unrecognized part [die] specified for device [silicon_family] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

```
Unrecognized package [package_name] specified for part [die] in
[design_name]:synthesis
```

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

```
Warning: Unrecognized technology: [silicon_family]
Unrecognized technology: [silicon_family] in [design_name]:synthesis
```

Synplify Pro halts.

Programming

SmartFusion2 and IGLOO2 programming file generation on Linux will be available in a future release. Use Libero for Windows.

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

You may get an exit 6 idcode failure when chain programming within Libero using a PDB file. Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming

SAR 47535 – Multiple dialog windows should not open for Programmer Settings, Update eNVM Memory Content and Device I/O States.

If you double-click in these elements in the Design Flow window more than once then multiple windows open. If this happens close the extra windows.

SAR 47452 - FlashPro verify and erase errors are reported as programming failures.

If you run programming ACTION VERIFY/ERASE and there is a failure, then the error code will indicate it is a programming failure even though you were running action VERIFY/ERASE.

SmartDebug

SmartDebug Tcl commands in the Libero flow will be supported in a future release.

SmartFusion2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the Flash Memory.

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.

System Requirements

Refer to System Requirements on the web for more information regarding operating systems support and minimum system requirements. 64-bit OS is required for designing SmartFusion2 and IGLOO2 150/100 devices.

Setup Instructions for Red Hat Enterprise Linux OS can be found on the Libero SoC Documents webpage.

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.1 installation.

Synplify Pro ME H-2013.03M-1 Release Notes

ModelSim AE 10.1c

Identify ME H-2013.03M Release Notes (Windows only)

Synphony Model Compiler ME H-2013.03M SP1 Release Notes (Windows only)

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.1 SP2

Windows or Linux

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