

CR0021
Characterization Report
SmartFusion2 SoC and IGLOO2 Characterization
Report For PCI Express



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

The following is a summary of the changes in revision 3.0 of this document.

- Rebranded the document.
- This report covers both SmartFusion2 SoC and IGLOO2 FPGA families. Hence, updated the document title and content accordingly (SAR 84058).

1.2 Revision 2.0

In revision 2.0 of this document, [Table 8](#), page 16 was updated (SAR 69150).

1.3 Revision 1.0

Revision 1.0 was the first publication of this document.

2 SmartFusion2 SoC and IGLOO2 Characterization Report For PCI Express

The Microsemi SmartFusion[®]2 SoC and IGLOO[®]2 FPGA families provide a fully embedded PCI Express[®] Gen1/2- x1/x2/x4 endpoint. This embedded PCI Express solution is part of the SERDESIF module which supports 4 lanes of SERDES with data rates supported up to 5Gbps. The number of SERDESIF modules on the SmartFusion2 SoC and IGLOO2 depends on the device size. The smaller devices support a single SERDESIF with a single PCI Express interface. The larger devices support up to 4 SERDESIF modules for a total of 4 PCI Express interfaces. More information on the SmartFusion2 SoC FPGA family can be found on the Product Page at www.microsemi.com/smartfusion2. More information on the IGLOO2 FPGA family can be found on the Product Page at <http://www.microsemi.com/products/fpga-soc/fpga/igloo2-fpga>.

2.1 Scope of this Report

Complete testing and validation of specifications required by Gen 1 and Gen 2 PCI Express standards were conducted on the SmartFusion2 SoC and IGLOO2 FPGA devices. This report provides the user community a summary of both PCIe related device testing and characterization as well as results of the compliance testing conducted at PCISIG testing workshops. Comprehensive testing was done to characterize the PCIe electrical performance of the device. The testing analyzed voltage, temperature, and process variations for specific PCIe parameters and higher level testing was conducted to verify the link and protocol functionality of the SmartFusion2 and IGLOO2 PCIe solution. This report serves as a reference to the specific testing used to provide high confidence that the devices will perform as expected in PCI Express systems.

2.2 PCISIG Compliance Testing

PCISIG is the industry organization chartered to develop and manage the PCI standards. The PCISIG Compliance Program offers the latest in PCI device testing, including the opportunity to test your system or Add-in Card with other members' PCI products. Completing testing at the PCISIG Compliance Workshop will enable devices to be added to the PCISIG Integrators Listing.

A traditional PCI Express system utilizes a CPU connected to a root device, which is responsible for configuring and enumerating all PCI Express endpoint devices within the system. A point-to-point PCIe system requires a switch device to grow the number of endpoint devices present with one root and one or more endpoint devices. An FPGA-based endpoint provides a high level of integration enabling high-performance, fully compliant PCI Express systems in a single device. The use of the FPGA-based endpoint add-in cards have become the “de-facto” means for testing PCIe Gen 1 and 2 standards at PCI Express workshops.

PCI Express endpoint add-in cards developed by Microsemi, provide the physical capabilities to test devices at the compliance workshop. A standardized interface of the printed circuit boards is utilized to test the device performance and to exercise the IP used to implement the PCI Express functionality. The boards are tested for electrical compliance, subjected to link and transaction protocol tests, and checked for proper configuration space implementation. Participants pass or fail at the compliance workshop by attending testing sessions.

2.3 Compliance Testing

There are four encompassing areas of PCI Express compliance testing for components tested on add-in cards:

Electrical Testing—Examines the device and add-in card signal quality for eye pattern, jitter, and 2.5/5Gbps data rate analysis.

Configuration Space Testing (CV)—Examines the configuration space in PCI Express devices by verification of required fields and values.

Link and Transaction Protocol Testing (PTC)—Tests the device behavior for link-level protocol and device behavior for transaction-level protocol. Link and transaction layers are exercised for protocol boundary conditions. Tests include error injection and check error-handling capabilities.

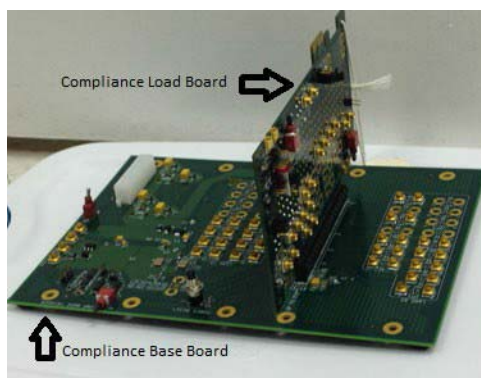
Interoperability Testing—Tests conducted between workshop participants that show compatibility between PCI Express technologies.

These tests were all conducted and validated by Microsemi. PCIe compliance was verified at a test compliance workshop held by the PCISIG.

2.3.1 Electrical Testing

PCI Express Electrical Testing was developed to verify product-level physical compliance to the PCI Express CEM specification(s). PCI Express Electrical Testing consists of a series of tests used to evaluate PCI Express products. A series of tests were performed on Microsemi boards in conjunction with the PCISIG compliance base board (CBB) and the compliance load board (CLB) to validate signal quality of TX, Ref Clock, and PLL Loop Bandwidth.

Figure 1 • PCIe Compliance Test Channel



Once data is collected from the test platforms, analysis software is used on the collected information to determine whether the device meets the specifications or not.

The test criteria are specified in the *PCI Express Architecture PHY Electrical Test Considerations Revision 2.0**.

PCIe Gen1 and Gen2 electrical tests conform to section 4.3 of the *PCI_Express_Base_r2_1_04March09.pdf** and the *PCI_Express_CEM_r2.0.pdf**.

2.3.2 Configuration Space Testing

The PCI Express Configuration Verifier (CV) test is a software application provided by PCISIG that runs on a Windows 7 32-bit PC and exercises access to the configuration space registers of the device under test. Its purpose is to check for compliance with the PCIe specification for configuration space registers (type 1-switch/bridge). A detailed description of tests performed can be found in the document *PCI EXPRESS ARCHITECTURE CONFIGURATION SPACE TEST SPECIFICATION, REV. 2.0**. The tests are conducted with the Add-in Card placed in a PCI Express slot in the PC. The test software accesses the Add-in Card and issues configuration read and write requests and checks for the correct response.

Note: These specification documents are only available to PCISIG members at: <http://www.pcisig.com/specifications/pciexpress>.

The tests check the following:

- Configuration space registers can be read
- Read-only registers retain their value when attempted to be written to
- Writable registers can be written to
- Registers have the correct default value after reset
- Capabilities lists are valid and correctly linked
- PCI Express 2.0, 1.1, and/or 1.0a specific fields and capabilities are present

The test program also performs functional stress tests to ensure the endpoint can re-train and re-link in an acceptable amount of time. It also tests to ensure the card can properly handle hundreds of cycles of link-up/link-down and all registers are operational (such as the endpoint firmware has not locked up). In summary, the CV test suite verifies that the PCI Express endpoint is truly functional in a PC and covers all aspects of hardware and operating system interaction. It shows that the card can be recognized by the PCI Express hardware and can be enumerated and configured by the operating system for access by software applications.

2.3.3 Link and Transaction Protocol Testing

The PCI Express Link and Transaction Layer protocol testing was developed to test the add-in card compliance to the Link and Transaction protocol specification requirements. The testing utilizes the E2969B Protocol Test Card 2 (PTC-2) and the test code from Agilent Technologies or the Teledyne LeCroy Protocol Test Card. Both PTC cards exercise all required tests that the PCISIG will conduct during its compliance workshops by using this Agilent hardware. The PTC-2 exercises specifications for the Transaction Layer and the Data Link Layer, and monitors the behavior of the device in response to certain error conditions. The PTC card is simply attached to the PCI Express add-in card under test and performs all mandatory tests from the PCISIG.

Figure 2 • Agilent PTC-2



These vendors' test packages contain PTC test code that is compatible with, and requires any of the Agilent E2960B or LeCroy PTCG2 family software packages, available on the Agilent or LeCroy websites free of charge. During link testing, the following tests are run using the PTC card. All of the following tests must be passed in order to be included on the Integrators List.

Table 1 • Link Tests Using PTC Card

| | |
|----------------------------|--|
| Bad CRC | Device detects, drops, and logs (DLLPs and TLPs) |
| Bad Sequence Number | Device detects, drops, and logs |
| Duplicate TLP | Device returns data once |
| Link Retrain | Device will retrain if continued no response |
| NAK Response | Device will resend after receiving NAK |
| Replay Count | Device will resend multiple times when no response |
| Replay Timers | Device will resend packet if no response |
| Replay TLP Order | Device replays TLPs in proper order |
| Reserved Fields | Device ignores reserved fields |
| Undefined Packet | Device ignores undefined packets |

2.3.4 Interoperability

The interoperability test sessions are used to show consistent functionality between PCI Express component vendors. During these sessions, the participants set their own test procedures and must

agree on what comprises a pass or a fail. Participants are expected to demonstrate some degree of functionality to substantiate that their interface is functional with another vendor's products.

The PCISIG recognizes that participants may bring designs that are not fully compliant or have unknown or undisclosed bugs. For this reason, to pass the interoperability tests vendors must only demonstrate a success rate of 80%. If they have passed 100% of the PCISIG mandatory tests (Gold Tests) and 80% interoperability, the device is eligible to be included on the Integrators List. The Integrators List is proof a product has passed the rigorous PCISIG tests and has demonstrated interoperability with others. This status implies that the device is viable for use in PCI Express systems.

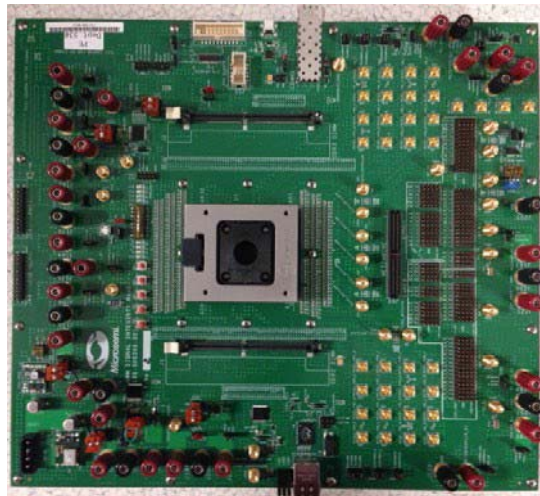
2.4 Microsemi Test Boards

Testing is performed on two types of boards which are dependent on the test requirements. Both boards are equipped with a test socket, which accommodates testing a variety of parts. The socket slightly contributes to attenuation and jitter, which will slightly degrade the testing results although the design of the boards minimize this effect.

2.4.1 Signal Integrity Board (SI)

The SI board is equipped with a test socket and provides connections to vary power supply conditions. To ensure the integrity of the characterization measurements, special attention is given to the signal integrity of the high-speed serial channels. Detailed analysis ensures the board performs as designed. The transmitter (TX) and receiver (RX) signal paths for each SERDES are carefully routed to high-bandwidth SMP connectors to ensure good signal integrity and performance. The PCB channel is measured and de-embedded when performing tests.

Figure 3 • SmartFusion2 Signal Integrity Board



2.4.2 PCIe Validation Board (PV)

The PV board is built specifically with PCIe-defined edge fingers. This PCIe validation board provides the capability to perform detailed PCIe testing on protocol analyzers and standardized PCIe testers. It also provides an accurate channel representative specified for PCIe add-on boards. This board has PCIe edge fingers that interconnect with PCIe sockets of PC motherboards. This interface allows for interoperation and evaluations in PCIe systems or industry standard test fixtures and test equipment.

Figure 4 • SmartFusion2 Validation Board



2.5 Device Testing

2.5.1 CV Testing

2.5.1.1 Description of Test

PCIe CV requires installation of software provided to members of the PCISIG group. The testing involves installation of the PCIe validation board into a PCIe slot on a host PC with the testing software installed. The PCIe validation board requires a separate power supply from the PC PCIe slot. The standalone testing exercises all specific testing as required by the PCISIG configuration verification specification. Refer to *PCIeCV 2.0 Configuration User Guide (2/25/2013)*.

Note: These specification documents are only available to PCISIG members at: <http://www.pcisig.com/specifications/pciexpress>.

2.5.1.2 Results

Configuration Testing

INFO PCIeCVApp.exe ver 1.5.1.9 INFO DriverInterfaceDLL.dll ver 1.4.7.0

INFO ttpi.dll ver 1.4.9.0

INFO Max Bus Number value: 50

INFO Beginning PCIeCV Test

INFO TEST OPTION SELECTED: Test against 2.0 Spec Only

INFO Virtual Function Detection Disabled.

INFO Test Endpoint was Selected.

INFO Device selected: Vendor ID= 11aa, Device ID= 0846

- Bus number= 0001, Device Number= 0000, Function= 0000

INFO Link Enable-Disable chosen as default reset type.

INFO Running the test at the maximum supported speed.

INFO Run All Tests Selected

INFO Link Width chosen:x4.

INFO TD_1_2_PCIExpressCapabilityStructureTest : PASSED

INFO TD_1_3_PCIExpressCapabilitiesRegisterTest : PASSED

INFO TD_1_4_DevCapControlStatusReg : PASSED

INFO TD_1_5_LinkCapControlStatusReg : PASSED

INFO TD_1_6_MSICapabilityStructureTest : PASSED

INFO TD_1_7_AdvancedErrorReportingCap : PASSED

INFO TD_1_8_VirtualChannelCap : PASSED

INFO TD_1_11_CommandStatusRegTest : PASSED

INFO TD_1_12_CacheLnSzMasterLatTimerMinGntMaxLatReg : PASSED

INFO TD_1_13_InterruptPinInterruptLine : PASSED

INFO TD_1_16_PowerManagementCap : PASSED

INFO TD_1_18_BaseAddressRegistersTest : PASSED

INFO TD_1_21_BISTRegisterTest : PASSED

INFO TD_1_23_PCINextCapabilityPointerTest : PASSED

INFO TD_1_24_PCIeNextEnhancedCapabilityPointerTest : PASSED
INFO TD_1_25_MiscType_0_ConfigSpaceHeaderRegTest : PASSED
INFO TD_1_27_Multi-FunctionTest : PASSED
INFO TD_1_32_PCIXCapabilityStructureTest : PASSED
INFO TD_1_39_MultiFunctionFLRTest : PASSED
INFO TD_1_40_DevCap2Control2Status2Reg : PASSED
INFO TD_1_41_LinkCap2Control2Status2Reg : PASSED
INFO TD_1_42_ACSExtendedCapabilityStructureTest : PASSED
INFO TD_1_50_SlotCap2Control2andStatus2RegTest : PASSED
INFO TD_2_1_ConfigurationStressTest : PASSED
INFO TD_2_2_LinkTrainingStressTest : PASSED
INFO TD_2_3_ResponseToControlMessagesTest : PASSED
INFO TD_2_4_ResponseToEarliestConfig : PASSED
INFO TD_2_7_LinkSpeedTest : PASSED
INFO TD_2_8_SupportedLinkWidthTest : PASSED INFO Test Summary

- Total Number of Tests Run: 29
- Number of Tests Passed: 29

Functional Testing

INFO PCIeCvApp.exe ver 1.5.1.9
INFO DriverInterfaceDLL.dll ver 1.4.7.0
INFO ttpi.dll ver 1.4.9.0
INFO Max Bus Number value: 50
INFO Beginning PCIeCV Test.
INFO TEST OPTION SELECTED: Test against 2.0 Spec Only
INFO Virtual Function Detection Disabled.
INFO Test Endpoint was Selected..
INFO Device selected: Vendor ID= 11aa, Device ID= 0846
Bus number= 0001, Device Number= 0000, Function= 0000
INFO Link Enable-Disable chosen as default reset type.
INFO Running the test at the maximum supported speed.
INFO Link Width chosen:x4.
INFO Beginning Functional Tests
Time from reset to first command: 250
INFO Upstream ASPM State Support: 3
INFO PCI Express Device ASPM State Support: 3
INFO TD_2_1 Configuration Stress Test Selected.
Device State : D0 - Uninitialized.
INFO TD_2_1_ConfigurationStressTest : PASSED
INFO TD_2_2_LinkTrainingStressTest : PASSED

INFO TD_2_3_ResponseToControlMessagesTest : PASSED

INFO TD_2_4_ResponseToEarliestConfig : PASSED

INFO TD_2_7_LinkSpeedTest : PASSED

INFO TD_2_8_SupportedLinkWidthTest : PASSED

INFO Test Summary

- Total Number of Tests Run: 6
 - Number of Tests Passed: 6
 - Number of Tests Failed: 0

2.5.2 PTC Testing

2.5.2.1 Description of Test

The PCIe validation board is installed and connected to the Agilent PTC2 (E2969B) exerciser. The PTC2 and the PCIe validation board require separate power supplies. The PTC2 is connected by the USB port to the controller PC, which has the PTC software installed. The card must be in PTC mode to perform the correct add-in tests on the PCIe validation board. For more information, see the Test Procedure for Agilent Gen 2 PTC for the [Link and Transaction Protocol Testing](#), page 4.

2.5.2.2 Results

This section includes example screenshots of the PTC test results.

Figure 5 • Gen 1 Agilent PTC Results

| Name | Description | Result |
|---------------------------------|--|--------|
| DLL_04_01_02 | To check that receiver ignores the reserved fields of the received DLLPs (ReservedFieldsDLLPReceive) | Passed |
| DLL_05_02_01 | To check that the link transmitter starts REPLAY after receiving a Nak (ReplayNumTest_ReplayTimerTest_ReXmitOnNak) | Passed |
| DLL_05_02_02 | To check that if REPLAY_NUM overflows, link retraining is triggered (LinkRetrainOnRetryFail_LinkRetrainOnRetryFailNoAckNack) | Passed |
| DLL_05_02_07 | To check that the retry buffer does not change in link retraining | Passed |
| DLL_05_02_10 | To check that the oldest unacknowledged TLP is sent first | Passed |
| DLL_05_02_15 | To check that corrupt DLLPs are discarded (CorruptedDLLPs) | Passed |
| DLL_05_02_16 | To check that a DLLP with undefined encodings is dropped silently (UndefinedDLLPEncoding) | Passed |
| DLL_05_02_17 | To check that an Ack with unknown sequence number is reported as FATAL_ERROR (WrongSeqNumInAckDLLP) | Passed |
| DLL_05_03_02 | To check for wrong LCRC detection (BadL_CRC) | Passed |
| DLL_05_03_03 | To check that a TLP with wrong sequence number is discarded, and any associated storage is freed (DuplicateTLPSeqNum) | Passed |
| EM_06_04 | To test link capabilities | Passed |
| LINKUPCONFIG | To check for correct linkup behavior | Passed |
| IDTRANS11_2_REQCOMPL_NOAER1 | To test UR handling in devices that do not implement AER | Passed |
| IDTRANS11_3_REQCOMPL_AER1 | To test UR handling in devices that implement AER | Passed |
| IDTRANS11_4_REQCOMPL_AER2 | To test UR handling in devices that implement AER | Passed |
| IDTRANS11_5_REQCOMPL_NOAER1 | To test UR handling in devices that do not implement AER | Passed |
| NegotiatedLinkWidth | To check Link negotiation | Passed |
| BadL_CRC | To check handling TLPs with bad CRC | Passed |
| CorruptedDLLPs | To check handling DLLPs with bad CRC | Passed |
| DuplicateTLPSeqNum | To check handling duplicate TLPs | Passed |
| LinkRetrainOnRetryFail | To check link retraining after replay | Passed |
| LinkRetrainOnRetryFailNoAckNack | To check link retraining after replay | Passed |
| ReplayNumTest | To check replaying transactions | Passed |
| ReplayTimerTest | To check the replay timer | Passed |
| ReplayTLPOrder | To check for correct TLP replay order | Passed |
| ReservedFieldsDLLPReceive | To check reserved fields in an ACK DLLP | Passed |
| ReXmitOnNak | To check retransmission of NAKed transaction | Passed |
| UndefinedDLLPEncoding | To check that DLLPs with undefined encoding are silently dropped | Passed |
| WrongSeqNumInAckDLLP | To check that ACK DLLPs with invalid sequence number are dropped | Passed |
| RequestCompletion11 | To check Basic Request and Completion handling | Passed |

Figure 6 • Gen 2 Agilent PTC Results

| Name | Description | Result |
|---------------------------------|---|--------|
| DLL_04_01_02 | To check that receiver ignores the reserved fields of the received DLLPs (ReservedFieldsDLLPReceive). | Passed |
| DLL_05_02_01 | To check that the link transmitter starts REPLAY after receiving a Nak (ReplayNumTest_ReplayTimerTest_ReXmitOnNak). | Passed |
| DLL_05_02_02 | To check that if REPLAY_NUM overflows, link retraining is triggered (LinkRetrainOnRetryFail_LinkRetrainOnRetryFailNoAckNack). | Passed |
| DLL_05_02_07 | To check that the retry buffer does not change in link retraining. | Passed |
| DLL_05_02_10 | To check that the oldest unacknowledged TLP is sent first. | Passed |
| DLL_05_02_15 | To check that corrupt DLLPs are discarded (CorruptedDLLPs). | Passed |
| DLL_05_02_16 | To check that a DLLP with undefined encodings is dropped silently (UndefinedDLLPEncoding). | Passed |
| DLL_05_02_17 | To check that an Ack with unknown sequence number is reported as FATAL_ERROR (WrongSeqNumInAckDLLP). | Passed |
| DLL_05_03_02 | To check for wrong L.CRC detection (BadL_CRC). | Passed |
| DLL_05_03_03 | To check that a TLP with wrong sequence number is discarded, and any associated storage is freed (DuplicateTLPSeqNum). | Passed |
| EM_06_01 | To test link capabilities. | Passed |
| LINKUPCONFIG | To check for correct linkup behavior. | Passed |
| IDTRANS11_2_REQCOMPL_NOAER1 | To test UR handling in devices that do not implement AER. | Passed |
| IDTRANS11_3_REQCOMPL_AER1 | To test UR handling in devices that implement AER. | Passed |
| IDTRANS11_4_REQCOMPL_AER2 | To test UR handling in devices that implement AER. | Passed |
| IDTRANS11_5_REQCOMPL_NOAER1 | To test UR handling in devices that do not implement AER. | Passed |
| NegotiatedLinkWidth | To check Link negotiation. | Passed |
| BadL_CRC | To check handling TLPs with bad CRC. | Passed |
| CorruptedDLLPs | To check handling DLLPs with bad CRC. | Passed |
| DuplicateTLPSeqNum | To check handling duplicate TLPs. | Passed |
| LinkRetrainOnRetryFail | To check link retraining after replay. | Passed |
| LinkRetrainOnRetryFailNoAckNack | To check link retraining after replay. | Passed |
| ReplayNumTest | To check replaying transactions. | Passed |
| ReplayTimerTest | To check the replay timer. | Passed |
| ReplayTLPOrder | To check for correct TLP replay order. | Passed |
| ReservedFieldsDLLPReceive | To check reserved fields in an ACK DLLP. | Passed |
| ReXmitOnNak | To check retransmission of NAKed transaction. | Passed |
| UndefinedDLLPEncoding | To check that DLLPs with undefined encoding are silently dropped. | Passed |
| WrongSeqNumInAckDLLP | To check that ACK DLLPs with invalid sequence number are dropped. | Passed |
| RequestCompletion1 | To check Basic Request and Completion handling. | Passed |

2.5.2.3 LeCroy PTC Results

Table 2 • Add-in Card Checklist – TXN TESTS

| Test | Description | Result |
|------------------------|---|--------|
| TXN Request Completion | Test 1.1 (TXN.2.7#9, TXN.2.21#15, TXN.2.21#19, TXN.3.1#1, TXN.3.1#2): Verify Basic Request and Completion handling of slotted Endpoint devices. | Pass |

Table 3 • Add-in Card Checklist – LINK TESTS

| Test | Description | Result |
|------------------------|---|--------|
| DLL WrongSeqNum | Test 52-170 (DLL.5.2#17): The intent of this test is to verify that the DUT drops any ACK DLLP that doesn't have a sequence number corresponding to an unacknowledged TLP and logs a BAD DLLP error associated with the port. | Pass |
| DLLP BadCRC | Test 52-150 (DLL.5.2#15): The intent of this test is to ensure that a DUT recognizes a DLLP with bad CRC, drops it and logs a BAD_DLLP port error. | Pass |
| DLLP ReservedFields | Test 41-20 (DLL.4.1#2): The intent of this test is to verify that the DUT truly ignores reserved fields in an ACK DLLP by sending arbitrary data in those fields. | Pass |
| DLLP UndefinedEncoding | Test 52-160 (DLL.5.2#16): The intent of this test is to verify that the DUT silently drops any DLLP with undefined encoding (any pattern for DLLP type that is reserved right now) and no error is associated with it. | Pass |

Table 3 • Add-in Card Checklist – LINK TESTS

| Test | Description | Result |
|----------------------------------|---|--------|
| LinkRecoveryRetryFail | Test 52-20 (DLL.5.2#2, DLL.5.2#7): The intent of this test is to ensure that the link connected to the DUT will go into retraining after trying for REPLAY_NUM of times to get a TLP through and failing. It will also test that while in retraining the retry buffer and link states are not changed and the pending TLP is retransmitted after link retraining completes. | Pass |
| LinkRecoveryRetryFail No Ack Nak | Test 52-20 (DLL.5.2#2, DLL.5.2#7): The intent of this test is to ensure that the link connected to the DUT will go into retraining after trying for REPLAY_NUM of times to get a TLP through and failing. It will also test that while in retraining the retry buffer and link states are not changed and the pending TLP is retransmitted after link retraining completes. | Pass |
| ReplayNum | Test 52-12 (DLL.5.2#1.1): The intent of this test is to ensure that a DUT will keep retransmitting a transaction for which a NAK has been issued on purpose until the number of times its REPLAY_NUM supports. | Pass |
| ReplayTimer | Test 52-11 (DLL.5.2#1.1): The intent of this test is to ensure that a DUT's REPLAY_TIMER is working properly by not sending neither an ACK nor a NAK. | Pass |
| ReXmitOnNak | Test 52-10 (DLL.5.2#1): The intent of this test is to ensure that a DUT will retransmit a transaction for which a NAK has been issued. | Pass |
| TLP BadLCRC(32bit) | Test 53-20 (DLL.5.3#2): The intent of this test is to verify that a receiver discards a TLP with bad CRC by NAKing it and reports a BAD TLP error associated with the port. | Pass |
| TLP DuplicateSeqNum | Test 53-31 (DLL.5.3#3.1): The intent of this test is to verify that the duplicate (TLP with the same sequence number associated at the link layer as that in the last 2048 TLPs received) TLPs are handled properly by the DUT. | Pass |
| TLP ReplayOrder | Test 52-100 (DLL.5.2#10): The intent of this test is to verify that the oldest unacknowledged TLP is retransmitted first in replay followed by the other unacknowledged TLPs in the same order they were transmitted first. | Pass |

Table 4 • Add-in Card Checklist – TRAINING TESTS

| Test | Description | Result |
|---------------------------------|--|--------|
| ReservedBitsInTrainingSequences | The intent of this test is to verify that the DUT truly ignores reserved fields in Training Sequences (TS1 and TS2). | Pass |

2.5.3 Electrical Testing

PCI Express I/O electrical characterization testing was completed by Microsemi over device process, voltage, and temperature variations (PVT). Testing was conducted on a sample of devices representing process fluctuations across silicon fabrication. These devices were separated from a large sample and represented the worse-case corners to report the results. The results are correlated and presented in the data as worst-case. The testing procedures verify the device can achieve critical specification targets such as:

- Jitter

- Eye mask
- Different De-emphasis levels
- Reference Clock
- Voltage and Jitter margining
- Receiver Margining

The following PCIe electrical characterization tests were conducted on the clock configuration:

- PCI Express Transmitter testing RefClk was externally generated by an on-board oscillator on the PCISIG, PCIe CBB Compliance Board
- PCI Express Receiver and PLL testing RefClk were externally generated by a signal generator and connected thru SMA's

The characterization was performed in accordance with PCI Express CEM specification that requires the add-in card be plugged into the PCISIG PCI Express compliance baseboard (CBB2) to perform PCIe measurements. The PCI Express CEM compliant test setup consists of a necessary compliance channel (Edge Finger Connector of an add-in card with 2" to 3" of trace to the silicon device, the PCI Express connector itself, and 2.5" to 3" of trace to the SMP connector). Device electrical tests were conducted on the signal integrity board, which has high-speed SMP connectors for bringing signals on and off the board. To build a necessary PCIe compliance channel per the PCIe CEM specification with the signal integrity board, a special setup was assembled. The setup uses the PCISIG compliance load board (CLB2) mated with a compliance baseboard (CBB2). This setup closely matches the correct PCIe channel as it is present between the device under test on the signal integrity board and the test equipment.

Testing was also conducted with the PCIe validation board. In this setup, the CBB provides the physical means to connect the validation board to the test equipment and provides the required PCIe add-in card channel. This test setup was used to provide a test platform at the PCISIG compliance workshop.

2.5.4 Electrical Testing Equipment/Software

- Agilent DSA91304A, 13GHz Real Time Scope or DSO93204A 32Ghz Real Time Scope
 - Agilent N5393C PCI Express Automation Test Application, Version 02.24 or newer
 - PCIe SIGTST 3.1.9 or newer
- BitifEye N5990A Test Automation Software Platform
 - PCI Express2 Application, Version 1.11.20101207 or newer
- Agilent J-BERT N4903B with A02 Option License
- Agilent N4916A De-Emphasis Signal Converter
- Agilent N6701A Power Supply Mainframe
 - Four individually controlled P/S Modules
- BertScope CR12500A, Clock Recovery Module and PLL Bandwidth S/W Application
- Silicon Thermal, Temperature Control Unit
 - Silicon Thermal Chiller CH400
 - Silicon Thermal Linear Power Supply PS190-L
 - Silicon Thermal Temperature Controller LB190-L
 - Silicon Thermal Head Adapter
- SMA-to-SMA cables
- SMA-to-SMP cables
- PCISIG, Compliance Base Board2 (CBB2) Fixture
- PCISIG, Compliance Load Board2 (CLB2) Fixture

2.5.5 Electrical Testing Environment

Device electrical testing was conducted by Microsemi using variations on power supply voltages and temperatures. Minimum voltage (V_{min}) and maximum voltage (V_{max}) were varied by +/-5% of the typical voltage (V_{typ}) supply for the supplies related to the PCIe blocks of the device. The devices were also tested at the industrial temperature limits (-40°C to +125°C).

2.5.6 Testing Conditions

Table 5 • Voltage and Temperature Matrix

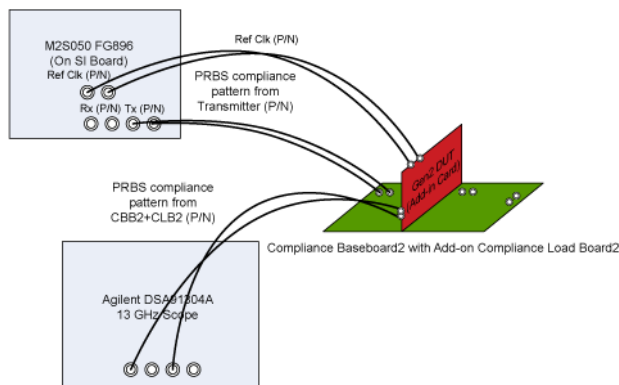
| Voltage Dependencies | 1.2 V VDD Device Range | | | | | |
|------------------------|------------------------|--------|---------|---------|--------|---------|
| | 3.15 V | 3.3 V | 3.45 V | 3.15 V | 3.3 V | 3.45 V |
| xDDR_PLL_VDDA | 3.15 V | 3.3 V | 3.45 V | 3.15 V | 3.3 V | 3.45 V |
| CCC_xyz_PLL_VDDA | 2.375 V | 2.5 V | 2.625 V | 3.15 V | 3.3 V | 3.45 V |
| SERDES_x_PLL_VDDA | 2.375 V | 2.5 V | 2.625 V | 3.15 V | 3.3 V | 3.45 V |
| SERDES_x_L[0:3]VDDAPLL | 2.375 V | 2.5 V | 2.625 V | 2.375 V | 2.5 V | 2.625 V |
| SERDES_x_L[0:3]VDDAIO | 1.14 V | 1.2 V | 1.26 V | 1.14 V | 1.2 V | 1.26 V |
| SERDES_x_VDD | 1.14 V | 1.2 V | 1.26 V | 1.14 V | 1.2 V | 1.26 V |
| VDD (Core Supply) | 1.14 V | 1.2 V | 1.26 | 1.14 V | 1.2 V | 1.26 V |
| Temperature | -40 °C | -40 °C | -40 °C | -40 °C | -40 °C | -40 °C |
| | 0 °C | 0 °C | 0 °C | 0 °C | 0 °C | 0 °C |
| | 25 °C | 25 °C | 25 °C | 25 °C | 25 °C | 25 °C |
| | 85 °C | 85 °C | 85 °C | 85 °C | 85 °C | 85 °C |
| | 100 °C | 100 °C | 100 °C | 100 °C | 100 °C | 100 °C |

2.5.7 Transmit Compliance Testing

2.5.7.1 PCI Express Transmitter Setup

The PCIe specification requires a transmitter to send a defined compliance pattern. This compliance pattern is continually sent when not connected to a link partner, because an exit response from electrical idle is never detected. See the PCI Express specification for full details on the electrical compliance pattern. With this pattern, a series of tests are conducted to analyze the quality of the transmitter data eye. The testing produces direct and indirect measured data that is correlated to the PCIe specifications. For more information, see *PCI EXPRESS ARCHITECTURE PHY TEST SPECIFICATION, REV. 2.0** for detailed procedures.

Note: These specification documents are only available to PCISIG members at:
<http://www.pcisig.com/specifications/pciexpress>.

Figure 7 • Transmitter Test Setup

2.5.7.2 Results

Table 6 • Transmitter Compliance Test Results – Gen 1

| Tx Compliance test parameters | 100 °C | 85 °C | 0 °C | -40 °C | 25 °C | 100 °C | 85 °C | 0 °C | -40 °C | Units | SPEC |
|---|---------------|---------------|---------------|---------------|---------------|--------------|--------------|--------------|--------------|-------|-----------------------------------|
| | Vmin | Vmin | Vmin | Vmin | Vtyp | Vmax | Vmax | Vmax | Vmax | | |
| | PT7/ TC101 | PT7/ TC102 | PT7/ TC104 | PT7/ TC105 | PT7/ TC124 | PT7/ TC80 | PT7/ TC81 | PT7/ TC83 | PT7/ TC84 | | |
| Add-in Card Tx, Unit Interval (PCIe 2.0, 2.5 GT/s) | 400.03 | 400.03 | 400.03 | 400.03 | 400.03 | 400.03 | 400.03 | 400.03 | 400.03 | ps | 399.8800 ≤ VALUE 400.1200 |
| Add-in Card Tx, Median to Max Jitter (PCIe 2.0, 2.5 GT/s) | 19.68 | 19.95 | 20.83 | 22.25 | 18.71 | 17.04 | 18.43 | 18.26 | 17.25 | ps | VALUE ≤ 56.50 |
| Add-in Card Tx, Eye-Width (PCIe 2.0, 2.5 GT/s) | 355.92 | 354.90 | 355.02 | 353.01 | 358.41 | 361.24 | 359.08 | 360.19 | 359.33 | ps | VALUE ≥ 287.00 |
| Add-in Card Tx, Peak Differential Output Voltage (Transition) (PCIe 2.0, 2.5 GT/s) | 947.50 | 935.30 | 948.20 | 959.30 | 988.60 | 1030.80 | 1031.90 | 1058.30 | 1063.30 | mV | 360.0m V ≤ VALUE ≤ 1.2000 V |
| Add-in Card Tx, Peak Differential Output Voltage (NonTransition) (PCIe 2.0, 2.5 GT/s) | 519.60 | 505.40 | 517.40 | 520.90 | 544.80 | 568.00 | 557.50 | 588.90 | 580.20 | mV | 360.0m V ≤ VALUE ≤ 1.2000 V |

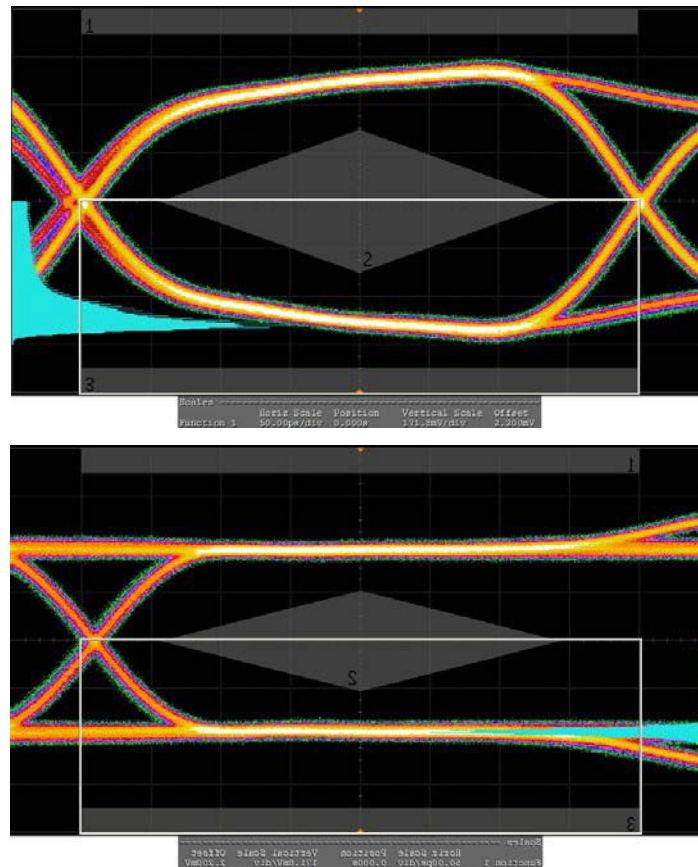
Table 7 • Transmitter Compliance Test Results – Gen 2 (- 3.5dB)

| Tx Compliance test parameters | 100 °C | 85 °C | 0 °C | -40 °C | 25 °C | 100 °C | 85 °C | 0 °C | -40 °C | Units | SPEC |
|---|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|----------------------|----------------------|----------------------|----------------------|-------|--|
| | Vmin PT7/ TC101 | Vmin PT7/ TC102 | Vmin PT7/ TC104 | Vmin PT7/ TC105 | Vtyp PT7/ TC124 | Vmax PT7/ TC80 | Vmax PT7/ TC81 | Vmax PT7/ TC83 | Vmax PT7/ TC84 | | |
| Add-in Card Tx, Peak Differential Output Voltage - 3.5dB (PCIe 2.0, 5.0 GT/s) | 902.30 | 909.80 | 910.20 | 914.30 | 943.70 | 992.40 | 990.10 | 1012.40 | 1028.30 | mV | 380.0m V <= VALUE <= 1.2000 V |
| Add-in Card Tx, Eye-Width - 3.5dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 145.26 | 147.13 | 145.10 | 143.53 | 148.07 | 152.51 | 153.96 | 152.06 | 152.81 | ps | VALUE >= 123.00 |
| Add-in Card Tx, RMS Random Jitter -3.5dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 1.70 | 1.64 | 1.78 | 1.90 | 1.73 | 1.57 | 1.55 | 1.61 | 1.65 | ps | VALUE <= 20.000 |
| Add-in Card Tx, Maximum Deterministic Jitter - 3.5dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 30.86 | 29.83 | 29.84 | 29.79 | 27.54 | 25.39 | 24.18 | 25.32 | 24.01 | ps | VALUE <= 57.000 |
| Add-in Card Tx, Total Jitter at BER-12 - 3.5dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 54.74 | 52.87 | 54.90 | 56.47 | 51.93 | 47.49 | 46.04 | 47.94 | 47.19 | ps | VALUE <= 77.000 |
| Add-in Card Tx, Eye-Width - 3.5dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 145.26 | 147.13 | 145.10 | 143.53 | 148.07 | 152.51 | 153.96 | 152.06 | 152.81 | ps | VALUE >= 126.00 |
| Add-in Card Tx, RMS Random Jitter -3.5dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 1.70 | 1.64 | 1.78 | 1.90 | 1.73 | 1.57 | 1.55 | 1.61 | 1.65 | ps | VALUE <= 20.000 |
| Add-in Card Tx, Maximum Deterministic Jitter - 3.5dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 30.86 | 29.83 | 29.84 | 29.79 | 27.54 | 25.39 | 24.18 | 25.32 | 24.01 | ps | VALUE <= 54.000 |
| Add-in Card Tx, Total Jitter at BER-12 - 3.5dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 54.74 | 52.87 | 54.90 | 56.47 | 51.93 | 47.49 | 46.04 | 47.94 | 47.19 | ps | VALUE <= 74.000 |

Table 8 • Transmitter Compliance Test Results – Gen 2 (- 6.0 dB)

| Tx Compliance test parameters | 100 °C | 85 °C | 0 °C | -40 °C | 25 °C | 100 °C | 85 °C | 0 °C | -40 °C | Units | SPEC |
|---|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|----------------------|----------------------|----------------------|----------------------|-------|---|
| | Vmin PT7/ TC101 | Vmin PT7/ TC102 | Vmin PT7/ TC104 | Vmin PT7/ TC105 | Vtyp PT7/ TC124 | Vmax PT7/ TC80 | Vmax PT7/ TC81 | Vmax PT7/ TC83 | Vmax PT7/ TC84 | | |
| Add-in Card Tx, Peak Differential Output Voltage - 6.0dB (PCIe 2.0, 5.0 GT/s) | 909.80 | 915.50 | 930.40 | 929.80 | 965.60 | 1003.30 | 1009.70 | 1024.30 | 1035.70 | mV | 306.0mV <= VALUE <= 1.2000V |
| Add-in Card Tx, Eye-Width - 6.0dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 159.77 | 156.40 | 155.74 | 154.74 | 158.42 | 162.89 | 163.11 | 161.97 | 162.90 | ps | VALUE >= 123.00 |
| Add-in Card Tx, RMS Random Jitter -6.0dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 1.60 | 1.71 | 1.72 | 1.85 | 1.72 | 1.54 | 1.55 | 1.59 | 1.60 | ps | VALUE <= 20.000 |
| Add-in Card Tx, Maximum Deterministic Jitter - 6.0dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 17.70 | 19.61 | 20.11 | 19.24 | 17.37 | 15.41 | 15.04 | 15.65 | 14.56 | ps | VALUE <= 57.000 |
| Add-in Card Tx, Total Jitter at BER-12 - 6.0dB with crosstalk (PCIe 2.0, 5.0 GT/s) | 40.23 | 43.60 | 44.26 | 45.26 | 41.58 | 37.11 | 36.89 | 38.03 | 37.10 | ps | VALUE <= 77.000 |
| Add-in Card Tx, Eye-Width - 6.0dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 159.77 | 156.40 | 155.74 | 154.74 | 158.42 | 162.89 | 163.11 | 161.97 | 162.90 | ps | VALUE >= 126.00 |
| Add-in Card Tx, RMS Random Jitter -6.0dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 1.60 | 1.71 | 1.72 | 1.85 | 1.72 | 1.54 | 1.55 | 1.59 | 1.60 | ps | VALUE <= 20.000 |
| Add-in Card Tx, Maximum Deterministic Jitter - 6.0dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 17.70 | 19.61 | 20.11 | 19.24 | 17.37 | 15.41 | 15.04 | 15.65 | 14.56 | ps | VALUE <= 54.000 |
| Add-in Card Tx, Total Jitter at BER-12 - 6.0dB without crosstalk (PCIe 2.0, 5.0 GT/s) | 40.23 | 43.60 | 44.26 | 45.26 | 41.58 | 37.11 | 36.89 | 38.03 | 37.10 | ps | VALUE <= 74.000 |

Figure 8 • Transmitter Eye Diagrams

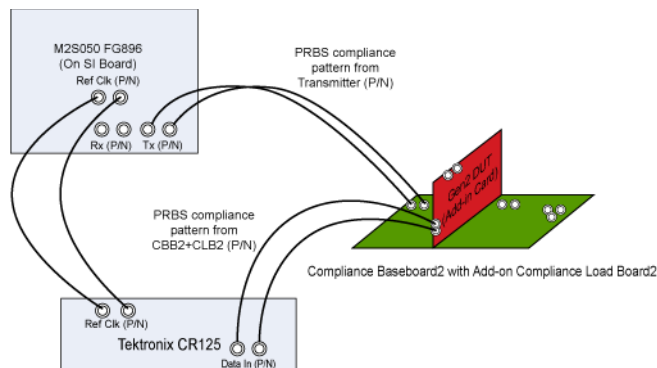


2.5.8 PLL Loop Bandwidth Testing

PLL bandwidth and peaking parameters are specified for 2.5 and 5Gbps operations. The Rx jitter for 2.5Gbps is inherently defined within the minimum eye width. However, the parameters for 5Gbps operation are separated for two-phase jitter frequency ranges. Each range specifies the allowable random and deterministic jitter components. The PLL bandwidth when measured with compliance pattern must be between 5 and 16 MHz if the peaking is less than 1 dB or must be between 8 and 16 MHz with a peaking of less than 3 dB. For 2.5 Gbps, the 3 dB point must fall between 1.5 and 22 MHz with peaking less than 3 dB.

2.5.8.1 PCI Express PLL Bandwidth Setup

The same PCI Express CEM Compliance Channel is applied to PCI Express PLL Bandwidth testing. The Ref CLK+/- is provided by the Tektronix CR125 Clock Recovery unit, and PCIe TX+/- lanes passing through both boards are connected to DATA_IN+/- of the CR125 unit. The CR125 DATA_OUT+/- must be terminated with 50 Ω terminators for M2S050-FG896 silicon to begin transmitting PCI Express Compliance Patterns upon power-up.

Figure 9 • PLL Bandwidth Test Setup**Table 9 • PLL Bandwidth Specifications**

| Category | Bandwidth Spec | Peaking Spec |
|----------------------------|-----------------|--------------|
| PLL Bandwidth Gen 1 | 1.5 to 22 MHz | < 3.0 dB |
| PLL Bandwidth Gen 2 Spec A | 5 MHz to 16 MHz | < 1.0 dB |
| PLL Bandwidth Gen 2 Spec B | 8 MHz to 16 MHz | < 3.0 dB |

Table 10 • PLL Bandwidth Testing Results

| Conditions | 100 °C | | 85 °C | | 0 °C | | -40 °C | | 25 °C | | 100 °C | | 85 °C | | 0 °C | | -40 °C | |
|---------------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|----------------|-------------|------|
| | Vmin | Vmax | Vmin | Vmax | Vmin | Vmax | Vmin | Vmax | Vtyp | Vmin | Vmax | Vmin | Vmax | Vmin | Vmax | Vmin | Vmax | |
| Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | Bandwidth(MHz) | Peaking(dB) | |
| Test Corner/ Device | TC38 PT4 | TC39 PT4 | TC41 PT4 | TC42 PT4 | TC61 PT4 | TC80 PT4 | TC81 PT4 | TC83 PT4 | TC84 PT4 | | | | | | | | | |
| Gen1 | 15.57 | 0.53 | 15.86 | 0.52 | 17.23 | 0.56 | 17.66 | 0.61 | 16.69 | 0.59 | 15.32 | 0.53 | 15.63 | 0.55 | 16.91 | 0.60 | 17.37 | 0.60 |
| Gen2 | 8.72 | 0.90 | 9.51 | 0.86 | 13.69 | 0.76 | 15.41 | 0.73 | 12.50 | 0.78 | 9.90 | 0.89 | 10.33 | 0.86 | 13.18 | 0.74 | 14.91 | 0.75 |

2.5.9 PCI Express Receiver Testing

Receiver testing stresses the incoming signal to determine its robustness to operate in typical system environments with a degree of noise and signal fluctuations. The test setup impairs the signal to the receiver by adding jitter, and determines that it can run normally with a long-term bit error rate target of 10^{-12} .

2.5.9.1 PCI Express Receiver Setup

The same PCI Express CEM Compliance Channel setup is used for the PCI Express Receiver testing. The JBERT and De-emphasis Box are interconnected together to provide a necessary generator for the PCI Express Receiver testing. The entire PCI Express CEM setup with an additional 7" of trace is calibrated to provide PCI Express Compliant Stressed Eye at the RX package balls of the M2S050-FG896 silicon under test. A 12 MHz CDR bandwidth was used to test the PCI Express Receiver Jitter Tolerance testing and was limited to only 5Gbps during the Worst Case Condition Phase of

Characterization. The test equipment stresses the receiver by imposing sinusoidal noise, and monitors the bit error rate of the system.

Figure 10 • Receiver Test Setup

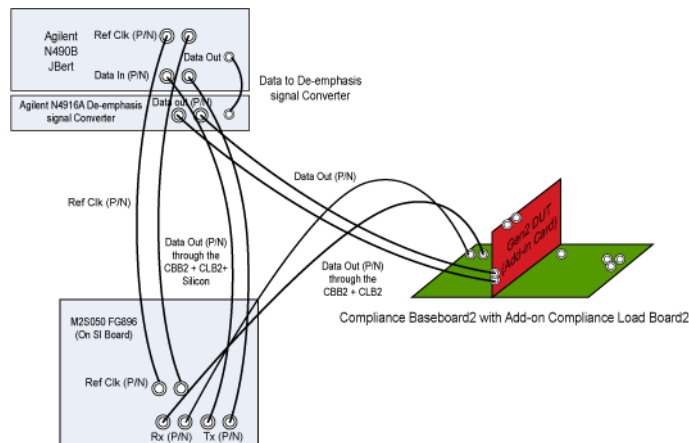
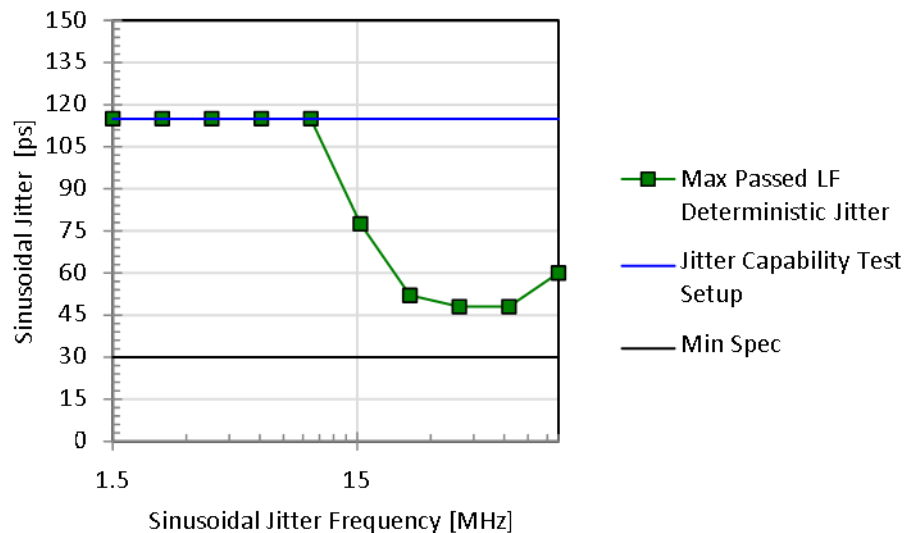


Table 11 • RX JTOL Compliance Tests (GEN1 & GEN 2)

| Conditions | 100 °C Vmin | 85 °C Vmin | 0 °C Vmin | -40 °C Vmin | 25 °C Vtyp | 100 °C Vmax | 85 °C Vmax | 0 °C Vmax | -40 °C Vmax |
|--------------------|----------------|---------------|--------------|----------------|---------------|----------------|---------------|--------------|----------------|
| Test Corner | TC115 | TC116 | TC118 | TC119 | TC138 | TC94 | TC95 | TC97 | TC98 |
| BER Results | > 1e-13 | > 1e-13 | > 1e-13 | > 1e-13 | > 1e-13 | > 1e-13 | > 1e-13 | > 1e-13 | > 1e-13 |

Rx_5GTps_Jitter Tol
PCI Express 2.0 Add-In Card

Figure 11 • Typical Receiver Tolerance Test Plot



2.6 Interoperability Results

The PCISIG Integrators List confirms that Microsemi has satisfied the PCISIG Compliance Program and that the endpoint solution successfully interoperated with other available systems at a PCISIG plug fest. Microsemi Smartfusion2 SoC and IGLOO2 FPGAs are listed under the Components section of the Integrators List. The list below highlights the many different partners, which interoperated successfully with Microsemi Smartfusion2 and IGLOO2 endpoints at the testing sessions.

Table 12 • PCIe Interoperability Systems

| System | Chip Set | CPU | Endpoint | System |
|-----------------------|--------------------|---------------|----------------|-------------|
| MindShare | Intel Sandy Bridge | Root Complex | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| X10SLM | Intel Lynx Point | Root Complex | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| RoseCity | Patsburgh | Root Complex | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| Gigabyte GA-Z77X-UD5H | Intel Z77 | Root Complex | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| ioMillennia | Intel | Switch/System | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| PLX | PEX 8748 | Switch/System | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| PLX 5 | PEX 8718 | Switch/System | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| PLX 4 | PEX 8714 | Switch/System | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |
| PLX 3 | PEX 8749 | Switch/System | 2.0 @ 2.5GT/s, | 3.0 A 8GT/s |

2.7 Conclusion

The test results demonstrate that the capabilities of the SmartFusion2 and IGLOO2 PCIe solution systems require high reliability devices to be robust. This report provides a baseline summary of the thorough testing performed by Microsemi to assure users that the device meets the performance and functional requirements in their customized PCI Express system.