

# Antifuse Product Information Brochure





Providing industry-leading FPGAs and SoCs for applications where **security** is vital, **reliability** is non-negotiable and **power matters.**

# Antifuse Product Information Brochure

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Please refer to [www.microsemi.com/fpga-soc](http://www.microsemi.com/fpga-soc) and appropriate product datasheets for the latest device information, valid ordering codes and more information.

The Axcelerator FPGA family is a single-chip, nonvolatile solution offering high performance and unprecedented design security at densities of up to 2 million equivalent system gates. Utilizing the AX architecture, Axcelerator devices have several system-level features, such as embedded SRAM (with embedded FIFO control logic), PLLs, segmentable clocks, chip-wide highway routing and carry logic. The solution is based upon 0.15  $\mu\text{m}$ , seven-layers-of-metal CMOS antifuse process technology and 350 MHz system performance.

- 500+ MHz internal performance
- 500+ MHz embedded FIFOs
- PLL output up to 1 GHz and 8 PLLs per device
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V mixed-voltage operation
- Bank-selectable I/Os—8 banks per chip
- 4.5 kbits variable-aspect RAM blocks with built-in FIFO control

## Axcelerator Devices

Axcelerator Devices	AX125	AX250	AX500	AX1000	AX2000
Capacity (in equivalent system gates)	125,000	250,000	500,000	1,000,000	2,000,000
Typical Gates	82,000	154,000	286,000	612,000	1,060,000
Register (R-cells)	672	1,408	2,688	6,048	10,752
Combinatorial (C-cells)	1,344	2,816	5,376	12,096	21,504
Maximum Flip-flops	1,344	2,816	5,376	12,096	21,504
Number of Core RAM Blocks	4	12	16	36	64
Total Bits of Core RAM	18,432	55,296	73,728	165,888	294,912
Clocks (hardwired)	4	4	4	4	4
Clocks (routed)	4	4	4	4	4
PLLs	8	8	8	8	8
I/O Banks	8	8	8	8	8
Maximum User I/Os	168	248	336	516	684
Maximum LVDS Channels	84	124	168	258	342
Total I/O Registers	504	744	1,008	1,548	2,052
Speed Grades	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2	Std., -1, -2
Temperature Grades	C, I	C, I, M	C, I, M	C, I, M	C, I, M

C – Commercial I – Industrial A – Automotive M – Military B – MIL-STD-883 Class B

## I/Os Per Package

Axcelerator Devices	AX125	AX250	AX500	AX1000	AX2000
PQFP		208	208		
PBGA				729	
FBGA	256, 324	256, 484	484, 676	484, 676, 896	896, 1152
CQFP		208, 352	208, 352	352	256, 352
CCGA/CLGA				624	624

The eX family of FPGAs, with its focused combination of features, can meet all of your power, speed, package and price requirements. eX devices are optimized for wired and mobile e-appliances, and enable designers to use a flexible single-chip FPGA for their traditional low-density ASIC requirements without the long lead times and costly NRE charges.

- Low power consumption
- Live at power-up
- 2.5 V, 3.3 V, and 5.0 V mixed-voltage operation with 5.0 V input tolerance and 5.0 V drive strength
- Up to 100% resource utilization with 100% pin locking
- Fuselock secure programming technology prevents reverse engineering and design theft
- Available in automotive temperature grades

## eX Devices

eX Devices	eX64	eX128	eX256
<b>Capacity</b>			
System Gates	3,000	6,000	12,000
Typical Gates	2,000	4,000	8,000
<b>Register Cells</b>			
Dedicated Flip-flops	64	128	256
Maximum Flip-flops	128	256	512
Combinatorial Cells	128	256	512
Maximum User I/Os	84	100	132
<b>Global Clocks</b>			
Hardwired	1	1	1
Routed	2	2	2
Speed Grades	-F, Std, -P	-F, Std, -P	-F, Std, -P
Temperature Grades	C, I, A	C, I, A	C, I, A
<b>Package (by pin count)</b>			
TQFP	64, 100	64, 100	100

C – Commercial I – Industrial A – Automotive M – Military B – MIL-STD-883 Class B

The SX-A family of FPGAs offers a cost-effective, single-chip solution for low-power, high-performance designs. SX-A devices can be used to generate system-wide savings by integrating multiple functions into a single-chip solution. Providing a combination of performance, security and low power, SX-A FPGAs decrease the premium for performance while providing a solution that is highly resistant to reverse engineering.

- 250 MHz system performance
- 350 MHz internal performance
- Power-up and power-down friendly (no sequencing required for supply voltages)
- 66 MHz, 64-bit 3.3 V / 5.0 V PCI performance (supporting target, master and master/target)
- 2.5 V, 3.3 V, and 5.0 V mixed-voltage support
- 100% resource utilization with 100% pin locking

## SX-A Devices

SX-A Device	A54SX08A	A54SX16A	A54SX32A	A54SX72A
Typical Gates	8,000	16,000	32,000	72,000
System Gates	12,000	24,000	48,000	108,000
Logic Modules	768	1,452	2,880	6,036
Combinatorial Cells	512	924	1,800	4,024
Dedicated Flip-flops	256	528	1,080	2,012
Maximum Flip-flops	512 *	990	1,980	4,024
Maximum User I/Os	130	180	249	360
Global Clocks	3	3	3	3
Quadrant Clocks	0	0	0	4
Boundary Scan Testing	Yes	Yes	Yes	Yes
3.3 V / 5 V PCI	Yes	Yes	Yes	Yes
Input Set-up (external)	0 ns	0 ns	0 ns	0 ns
Speed Grades	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2	-F, Std., -1, -2
Temperature Grades	C, I, A, M	C, I, A, M	C, I, A, M, B	C, I, A, M, B

C – Commercial I – Industrial A – Automotive M – Military B – MIL-STD-883 Class B

## I/Os Per Package

SX-A Devices	A54SX08A	A54SX16A	A54SX32A	A54SX72A
PQFP	208	208	208	208
VQFP				
TQFP	100, 144	100, 144	100, 144, 176	
PBGA			329	
FBGA	144	144, 256	144, 256, 484	256, 484
CQFP			84, 208, 256	208, 256

Featuring very low power consumption and the industry's highest design security, MX FPGAs offer designers a reliable, single-chip ASIC alternative. MX devices provide high performance while shortening the system design and development cycle. Offering an efficient, flexible 5.0 V architecture, MX is an ideal high-volume platform for integrating your legacy PLDs into a single device. Example applications include high-speed controllers and address decoding, peripheral bus interfaces, DSP and coprocessor functions.

- Single-chip ASIC alternative
- High performance mixed-voltage solution
- Contains embedded dual-port SRAM modules
- Ceramic devices available to DSCC SM
- Fast wide-decode circuitry
- QML certification

## MX Devices

MX Devices	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
System Gates	3,000	6,000	14,000	24,000	36,000	54,000
SRAM Bits	—	—	—	—	—	2,560
Sequential	—	—	348	624	954	1,230
Combinatorial	295	547	336	608	912	1,184
Decode	—	—	—	—	24	24
Clock-to-out	9.5 ns	9.5 ns	5.6 ns	6.1 ns	6.1 ns	6.3 ns
SRAM Modules (64x4 or 32x8)	—	—	—	—	—	10
Dedicated Flip-flops	—	—	348	624	954	1,230
Clocks	1	1	2	2	2	6
Maximum Flip-flops	147	273	516	928	1,410	1,822
User I/Os (maximum)	57	69	104	140	176	202
PCI	—	—	—	—	Yes	Yes
Boundary Scan Test (BST)	—	—	—	—	Yes	Yes
Speed Grades	-F, Std., -1, -2, -3	-F, Std., -1, -2, -3	-F, Std., -1, -2, -3	-F, Std., -1, -2, -3	-F, Std., -1, -2, -3	-F, Std., -1, -2, -3
Temperature Grades	C, I, M, A	C, I, M, A	C, I, M, A	C, I, M, A	C, I, M, A	C, I, M, A, B

C – Commercial I – Industrial A – Automotive M – Military B – MIL-STD-883 Class B

## I/Os Per Package

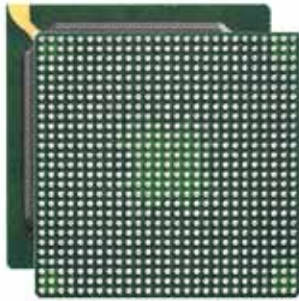
MX Devices	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
PLCC	44, 68	44, 68, 84	84	84	84	
PQFP	100	100	100, 160	100, 160, 208	160, 208	208, 240
VQFP	80	80	100	100		
TQFP			176	176	176	
CQFP						208, 256
PBGA						272

# FPGA Packages

**Key:** **f** – family **bs** – package body size excluding leads **ps** – overall package dimensions including package leads **h** – package thickness **p** – pin pitch / ball pitch

## BG729

**f** Axcelerator  
**ps** 35x35 mm  
**h** 2.33 mm  
**p** 1.27 mm



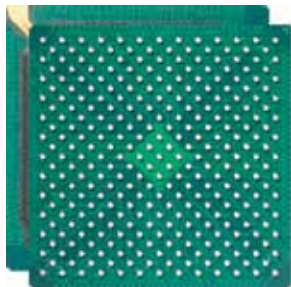
## BG329

**f** SX-A  
 SX  
**ps** 31x31 mm  
**h** 2.33 mm  
**p** 1.27 mm



## BG313

**f** SX  
**ps** 35x35 mm  
**h** 2.33 mm  
**p** 1.27 mm



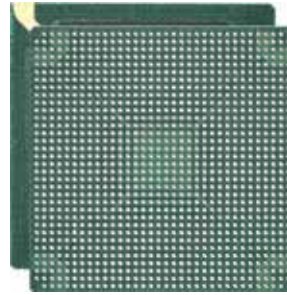
## BG272

**f** MX  
**ps** 27x27 mm  
**h** 2.33 mm  
**p** 1.27 mm



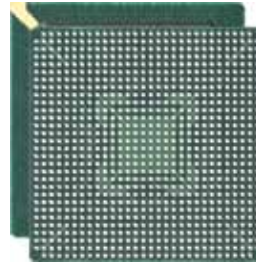
## FG1152

**f** Axcelerator  
**ps** 35x35 mm  
**h** 2.23 mm  
**p** 1.00 mm



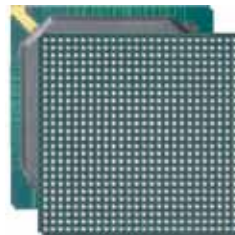
## FG896

**f** Axcelerator  
**ps** 31x31 mm  
**h** 2.23 mm  
**p** 1.00 mm



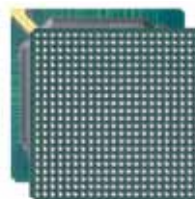
## FG676

**f** Axcelerator  
**ps** 27x27 mm  
**h** 2.23 mm  
**p** 1.00 mm



## FG484

**f** Axcelerator  
**ps** 23x23 mm  
**h** 2.23 mm  
**p** 1.00 mm



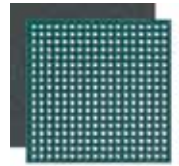
## FG484

**f** SX-A  
**ps** 27x27 mm  
**h** 2.23 mm  
**p** 1.00 mm



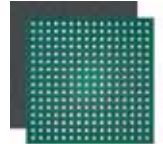
## FG324

**f** Axcelerator  
**ps** 19x19 mm  
**h** 1.63 mm  
**p** 1.00 mm



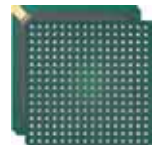
## FG256

**f** Axcelerator  
**ps** 17x17 mm  
**h** 1.60 mm  
**p** 1.00 mm



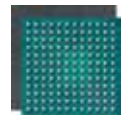
## FG256

**f** SX-A  
**ps** 17x17 mm  
**h** 1.76 mm  
**p** 1.00 mm



## FG144

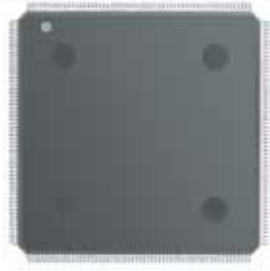
**f** SX-A  
 SX  
**ps** 13x13 mm  
**h** 1.45 mm  
**p** 1.00 mm





### PQ240

- f** MX
- bs** 32x32 mm
- ps** 34.6x34.6 mm
- h** 3.40 mm
- p** 0.50 mm



### PQ208

- f** Accelerator  
SX-A  
SX  
MX
- bs** 28x28 mm
- ps** 30.6x30.6 mm
- h** 3.40 mm
- p** 0.50 mm



### PQ160

- f** MX
- bs** 28x28 mm
- ps** 31.2x31.2 mm
- h** 3.37 mm
- p** 0.65 mm



### PQ100

- f** MX
- bs** 14x20 mm
- ps** 17.2x23.2 mm
- h** 2.80 mm
- p** 0.65 mm



### PL84

- f** SX  
MX
- ps** 1.154x1.154"
- h** 0.150"
- p** 0.050"



### PL68

- f** MX
- ps** 0.954x0.954"
- h** 0.150"
- p** 0.050"



### PL44

- f** MX
- ps** 0.654x0.654"
- h** 0.152"
- p** 0.050"



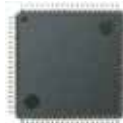
### VQ100

- f** SX  
MX
- bs** 14x14 mm
- ps** 16x16 mm
- h** 1.00 mm
- p** 0.50 mm



### VQ80

- f** MX
- bs** 14x14 mm
- ps** 16x16 mm
- h** 1.00 mm
- p** 0.65 mm



### TQ176

- f** SX-A  
SX  
MX
- bs** 24x24 mm
- ps** 26x26 mm
- h** 1.40 mm
- p** 0.50 mm



### TQ144

- f** SX-A  
SX
- bs** 20x20 mm
- ps** 22x22 mm
- h** 1.40 mm
- p** 0.50 mm



### TQ100

- f** SX-A  
eX
- bs** 14x14 mm
- ps** 16x16 mm
- h** 1.40 mm
- p** 0.50 mm



### TQ64

- f** eX
- bs** 10x10 mm
- ps** 12x12 mm
- h** 1.40 mm
- p** 0.50 mm



# Antifuse FPGA Selector Guide

	Accelerator					eX			SX-A				MX					
	AX125	AX250	AX500	AX1000	AX2000	eX64	eX128	eX256	A54SX08A	A54SX16A	A54SX32A	A54SX72A	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
System Gates	125 k	250 k	500 k	1 M	2 M	3 k	6 k	12 k	12 k	24 k	48 k	108 k	3 k	6 k	14 k	24 k	36 k	54 k
Typical Gates	82 k	154 k	286 k	612 k	1.06 M	2 k	4 k	8 k	8 k	16 k	32 k	72 k	2 k	4 k	9 k	16 k	24 k	36 k
Logic Modules	2,016	4,224	8,064	18,144	32,256	192	384	768	768	1,452	2,880	6,036	295	547	684	1,232	1,890	2,438
Dedicated Flip-flops	672	1,408	2,688	6,048	10,752	64	128	256	256	528	1,080	2,012	—	—	348	624	954	1,230
Maximum Flip-flops	1,344	2,816	5,376	12,096	21,504	128	256	512	512	990	1,980	4,024	147	273	516	928	1,410	1,822
SRAM Bits	18 k	55 k	74 k	166 k	295 k	—	—	—	—	—	—	—	—	—	—	—	—	2,560
Maximum I/O Available	168	248	336	516	684	84	100	132	130	180	249	360	57	69	104	140	176	202
Maximum I/O Single-ended	168	248	336	516	684	84	100	132	—	—	—	—	—	—	—	—	—	—
Maximum I/O Differential	84	124	168	258	342	—	—	—	—	—	—	—	—	—	—	—	—	—
1.5 V CMOS Drive	Yes	Yes	Yes	Yes	Yes	—	—	—	—	—	—	—	—	—	—	—	—	—
1.8 V CMOS Drive	Yes	Yes	Yes	Yes	Yes	—	—	—	—	—	—	—	—	—	—	—	—	—
2.5 V CMOS Drive	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—	—	—
3.3 V LVTTL Drive	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
5.0 V CMOS Drive	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
5 V Tolerant Inputs	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
3.3 V PCI I/O	Yes	Yes	Yes	Yes	Yes	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes
5.0 V PCI I/O	Yes <sup>1</sup>	Yes <sup>1</sup>	Yes <sup>1</sup>	Yes <sup>1</sup>	Yes <sup>1</sup>	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes
Slew Rate Control	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—	—	—
Routed Clocks <sup>2</sup>	4	4	4	4	4	2	2	2	3	3	3	3	1	1	2	2	2	6
Hard-wired Clocks <sup>2</sup>	4	4	4	4	4	1	1	1	0	0	0	4	—	—	—	—	—	—
PLL	8	8	8	8	8	—	—	—	—	—	—	—	—	—	—	—	—	—
JTAG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes
33 MHz PCI	Yes	Yes	Yes	Yes	Yes	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—	Yes	Yes
66 MHz PCI	Yes	Yes	Yes	Yes	Yes	—	—	—	Yes	Yes	Yes	Yes	—	—	—	—	—	—
Temp. Range	C, I	C, I, M	C, I, M	C, I, M	C, I, M	C, I, A	C, I, A	C, I, A	C, I, A, M	C, I, A, M	C, I, A, M, B	C, I, A, M, B	C, I, A, M	C, I, A, M	C, I, A, M	C, I, A, M	C, I, A, M	C, I, A, M, B
Speed Grades	Std, -1, -2	Std, -1, -2	Std, -1, -2	Std, -1, -2	Std, -1, -2	-F, Std, -P	-F, Std, -P	-F, Std, -P	-F, Std, -1, -2	-F, Std, -1, -2	-F, Std, -1, -2	-F, Std, -1, -2	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3	-F, Std, -1, -2, -3

C – Commercial I – Industrial A – Automotive M – Military B – MIL-STD-883 Class B

**Notes:**

1. With the use of an external resistor.
2. For SX-A routed clocks are called global clocks. Hard-wired clocks are called quadrant clocks.
3. Not all speed grades are available for all temperature ranges. Please refer to the Microsemi website and appropriate product datasheets for the latest device information and valid ordering codes.

# Antifuse I/Os by Package

		Accelerator					eX			SX-A				MX					
		AX125	AX250	AX500	AX1000	AX2000	eX64	eX128	eX256	A54SX08A	A54SX16A	A54SX32A	A54SX72A	A40MX02	A40MX04	A42MX09	A42MX16	A42MX24	A42MX36
CQFP	208		115	115								174	171						176
	256					136					228	213							202
	352		198	198	198	198													
CCGA	624				418	418													
PLCC	44												34	34					
	68												57	57					
	84													69	72	72	72		
PQFP	100												57	69	83	83			
	160														101	125	125		
	208		115	115					130	175	174	171				140	176	176	
	240																		202
VQFP	80												57	69					
	100														83	83			
TQFP	64						41	46											
	100						56	70	81	81	81	81							
	144									113	113	113							
	176										147					104	140	150	
PBGA	272																		202
	329										249								
	729				516														
FBGA	144								111	111	111								
	256	138	138							180	203	203							
	324	168																	
	484		248	317	317						249	360							
	676			336	418														
	896				516	586													
	1152					684													

Learn more about Microsemi's FPGAs and SoC FPGAs at [www.microsemi.com/fpga-soc](http://www.microsemi.com/fpga-soc)

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MS2-013-13/8.13