

Libero SoC v11.1 SP1 Release Notes

Libero SoC v11.1 SP1 delivers full support for IGLOO2 FPGAs.

Visit the IGLOO2 FPGA Documents page to download the Datasheet and Silicon User's Guides.

Customers designing SmartFusion2 and IGLOO2 devices should install v11.1 SP1 to take advantage of enhancements and fixes.

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- I/O Register combining is available through PDC for SmartFusion2 and IGLOO2

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What's New in this Release

IGLOO2 Device Support

Die	Programming
M2GL010, M2GL010T, M2GL010TS & M2GL010S	ENABLED

I/O Register combining is available through PDC for SmartFusion2 and IGLOO2.

Resolved Issues in the v11.1 SP1 Release

These Known Limitations that were documented in Libero SoC v11.1 Release Notes are fixed:

SAR 46571 - M2S050 has only one Oscillator

SAR 47395 – Automatic I/O register combining for SmartFusion2 and IGLOO2

SAR 46814 - The Placer ignores timing paths that go through a BIBUF (bidirectional I/O) if the path includes clock-to-input or clock-to-output constraints.

SAR 45419 - Linux: SmartTime is unable to launch the web browser to display Help.

SAR 46845 - The setup analysis fails to use the clock source latency constraint for ProASIC3 and IGLOO families.

SAR 47963 - Incorrect values for Input and Output Delay are entered automatically when external Setup and Hold values are entered in the Constraints Editor.

SAR 42451 - Programming Tcl commands in the Libero flow do not work in batch mode.

Fixed Customer Reported SARs

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

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Table 1 Resolved SARs in Libero SoC v11.1 SP1 Release

SAR	CASE	PRODUCT	SUMMARY
48656	493642-1362924708	Designer	Corrected a problem where adding max delay constraints substantially increased the amount of runtime required by the Placer
48404	493642-1347533092	FlashPro	FlashPro fixed to allow reprogramming of a secured device
48814	493642-1356097722	Help	USB: ULPI XCLK should be shown as only Input
47670	493642-1328020900	Help	SmartFusion2 Macro Library Guide correction
48828	493642-1336172062	Power	Corrected deviation between SmartPower estimations and real power measurement
46688	493642-1286695158	Project Manager	Fixed Libero Linux crash when LC_ALL is set to "C"
48604	493642-1360357320	Timing	Fixed the Auto-Generated Constraints Multiplier/Divider values mismatch with MSS_CCC configurator
48515	493642-1355056818	Timing	Fixed Tcl command st_expand_path to generate the proper report format



Known Limitations, Issues and Workarounds

SmartFusion2 and IGLOO2

For IGLOO2 projects, do not use the following cores from the Catalog. Use System Builder.

- DDR Memory Controller
- CoreConfigP
- CoreResetP
- CoreConfigMaster

IBIS models cannot be generated within Libero SoC. Please download them from our web site.

Block Design will be supported in a future release.

SECDED for the DDR Controllers will be supported in a future release.

Libero

SAR 41668 – SW Update Check window opens in full screen; cannot see buttons.

Workaround: Double-click in the header section of the window and it will redisplay correctly.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI.

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block.

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows.

This issue will be fixed in a future release.

SAR 42954 - Not all remote cores are visible in the Catalog panel after switching to a new vault, unless you reload the Catalog.

Workaround: Reload the Catalog after switching to a new vault. Select the **Settings** icon in **Catalog** and choose **Reload Catalog**.

SAR 46334 -Floorplanning PDC file names (*_fp.pdc) may not be in alphabetical order.

Workaround: Make sure the latest placement assignment changes are in the FP PDC file with a name last in the alphabetical ascending order with respect to other FP PDC files.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 49693 - Changing the default IO technology in Project Settings should invalidate Compile and Layout.

After changing the IO technology you must recompile for the changes to take effect.

SAR 49044 - On Linux, a segmentation fault occurs when MVN is closed

MVN functions normally otherwise.

SmartTime

SAR 49386 - Add set causes crash.

This will be fixed in the next release.



SAR 34365 - Asynchronous Register paths are not displayed in timing analysis view.

This issue will be fixed in a future release.

SAR 43095 - In the Domain Browser of the Analysis window, Edit Clock for a Generated Clock does not open the Edit Clock dialog box.

Workaround: Open the Constraint Editor tool to edit the generated clock constraint.

SAR 43767 - Maximize window button is missing from the Title bar.

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

Synthesis – See Libero SoC v11.1 Release Notes

Programming

SmartFusion2 and IGLOO2 programming file generation on Linux will be available in a future release. Use Libero for Windows.

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 48448 - Zeroization will be available in a future release.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 STAPL will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

You may get an exit 6 idcode failure when chain programming within Libero using a PDB file.

Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming

SAR 43530 - SmartFusion2 M2S050T_ES must be enabled after other devices in a chain.

When you have a chain with the M2S050T_ES enabled before other devices, you cannot enable programming for the non-SmartFusion2 devices.

Workaround:

- Disable the M2S050T_ES device for programming.
- 2. Enable each non-SmartFusion2 device for programming.
- 3. Enable the M2S050T_ES device for programming and proceed.

SAR 47535 - Programmer Settings, Update eNVM Memory Content, and Device I/O States During Programming should not open multiple dialogs.

If you click from Design Flow more than once multiple windows open. If this happens close the extra windows.

SAR 47452 - FlashPro verify and erase errors are reported as programming failures.

Regardless of the action that fails, the error code indicates a programming failure.

SAR 49990 - Error: The command 'load_programming_data' failed.

M2S050T_ES Generate Programming Data fails with the following error when security is used. This will be fixed in the next release.

Error: The identifier 'DO_ERASE_SECURED' is used before or without declaration.

Workaround: Do not use security.



SmartDebug

SmartDebug Tcl commands in the Libero flow will be supported in a future release.

SmartFusion2 and IGLOO2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the Flash Memory

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.



System Requirements

Refer to <u>System Requirements</u> on the web for more information regarding operating system support and minimum system requirements.

Setup Instructions for Red Hat Enterprise Linux OS can be found on the Libero SoC Documents webpage.

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Windows and Linux Version Libero SoC v11.1 SP1



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