Total Ionizing Dose Test Report

No. 13T-RTSX72SU-CQ208-D63Q4

June 29, 2013

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (SiO2)
2. Power Supply Current (ICCA/ICCI)	Passed 40 krad (SiO2)
3. Input Threshold (VTIL/VIH)	Passed 100 krad (SiO2)
4. Output Drive (VOL/VOH)	Passed 100 krad (SiO2)
5. Propagation Delay	Passed 100 krad (SiO2) for 10% degradation criterion
6. Transition Characteristics	Passed 100 krad (SiO2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and clock pin is grounded through a jumper; during annealing each input and clock pin is grounded through a 1-k ohm resistor.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP208
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72SCQ208_25strings
Die Lot Number	D63Q4
Quantity Tested	6
Serial Number	100 krad(SiO2): 380, 518 60 krad(SiO2): 536, 552 40 krad(SiO2): 577, 583
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 5.0 V/2.5 V

B. Test Method

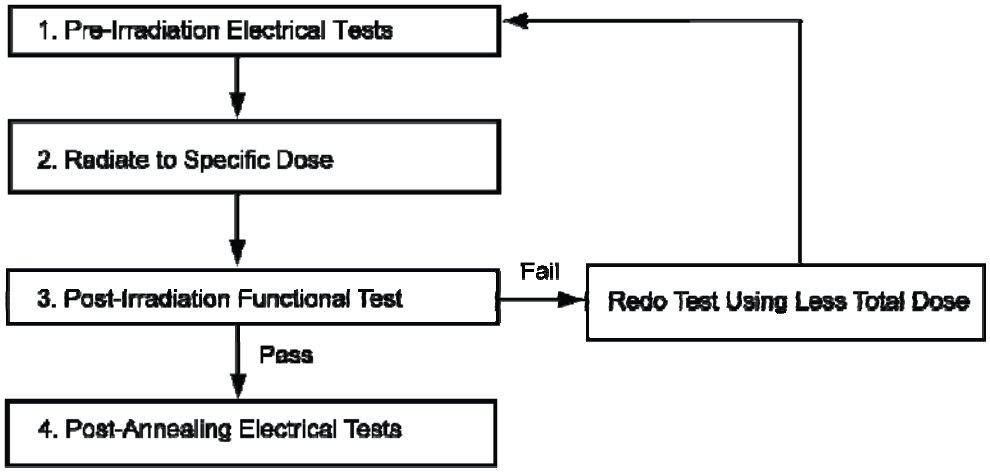


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by the deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from the radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTSX72SU are due to the radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72SCQ208_25strings) to test total dose effects in typical space applications. Appendix A contains the schematics illustrating the logic design which is the same as the one for the package CQ256.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic thresholds (VIL/VIH) and output-drive voltages (VOL/VOH) are measured on combinational nets, listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (VOL/VOH)	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin CLOCK to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Table 3 summarizes the pre-irradiation and post-annealing ICCA and ICCI data.

In compliance with TM1019.8, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCA/ICCI in the RTSX-SU spec sheet is 25 mA.

Table 3 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
380	100 krad	1.7	212.7	62	1.2	272.9	93
518	100 krad	1.6	213.6	55	1.0	270.8	95
536	60 krad	2.2	18.5	12	1.0	42.4	18
552	60 krad	2.2	19.2	12	1.0	45.0	19
577	40 krad	2.5	12.0	9	1.0	2.7	3
583	40 krad	2.2	3.8	3	1.0	2.5	3

It indicates that the post-annealing ICCA and ICCI for 40 krad (SiO2)-irradiated DUTs pass the spec.

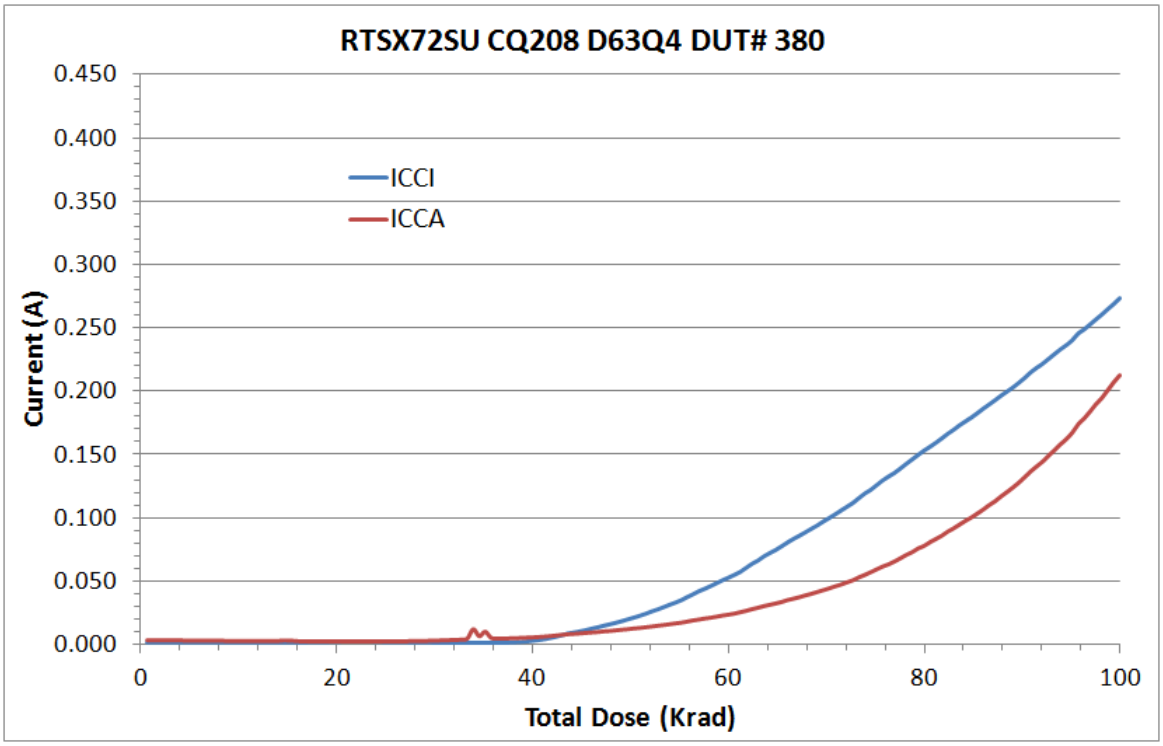


Figure 2 DUT 380 Influx ICCA and ICCI

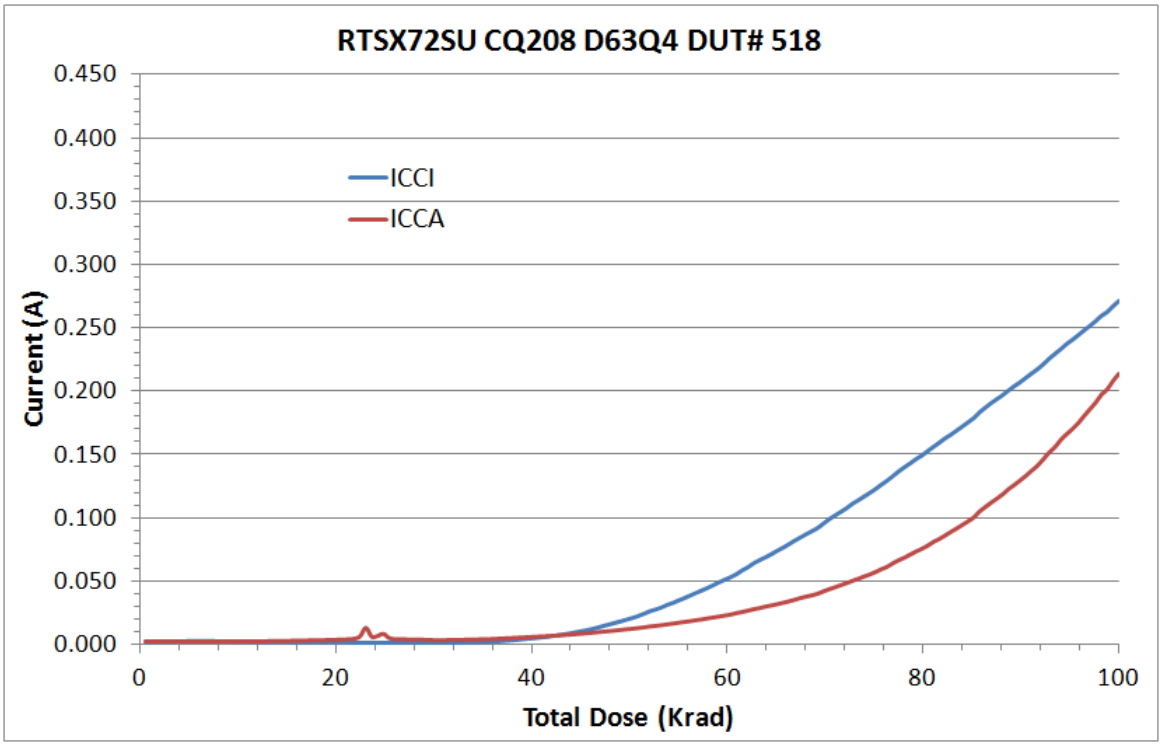


Figure 3 DUT 518 Influx ICCA and ICCI

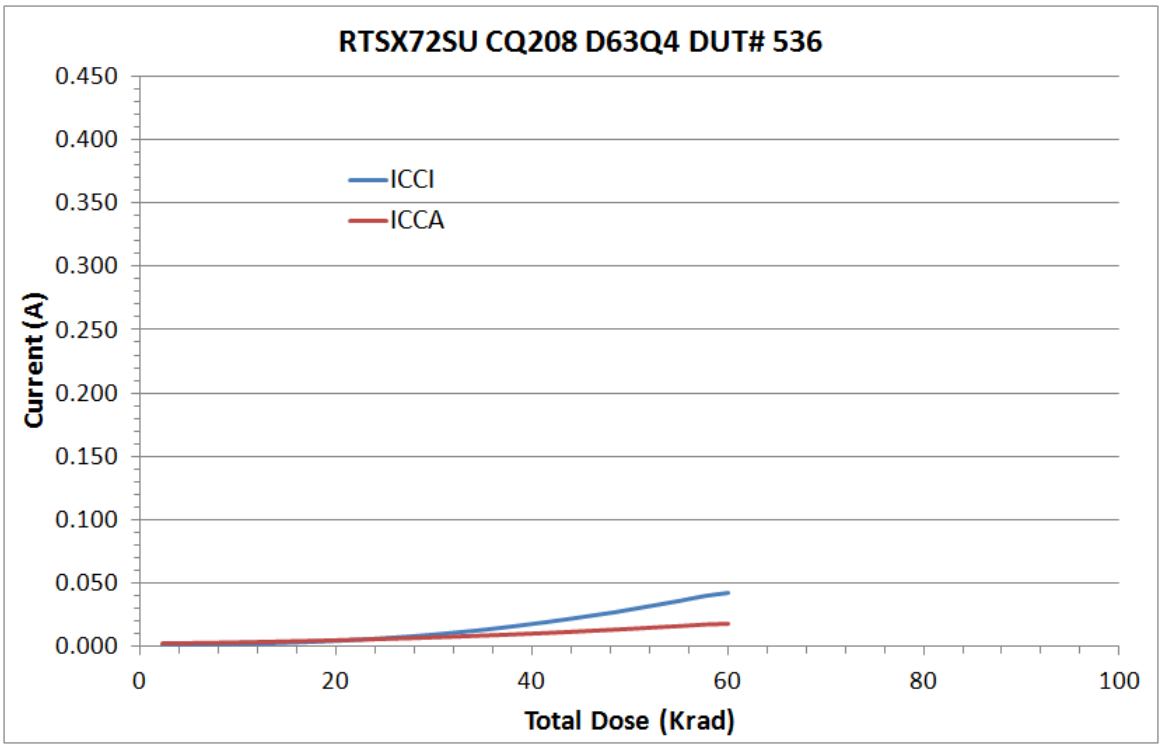


Figure 4 DUT 536 Influx ICCA and ICCI

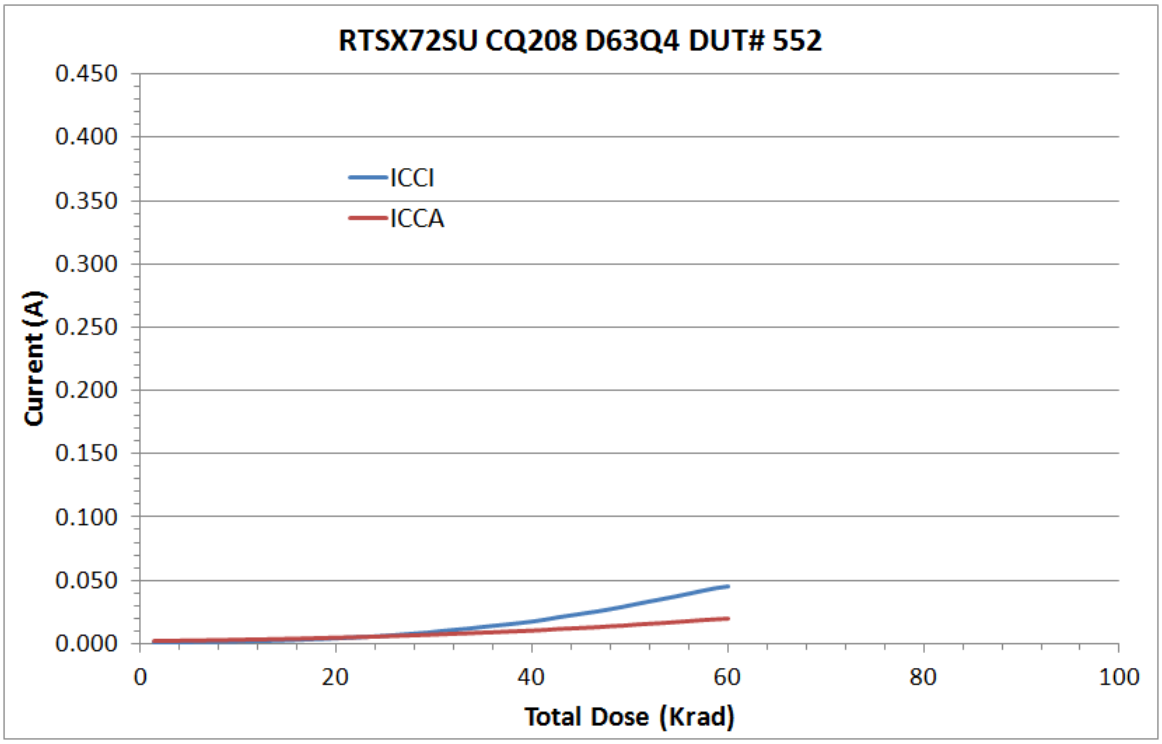


Figure 5 DUT 552 Influx ICCA and ICCI

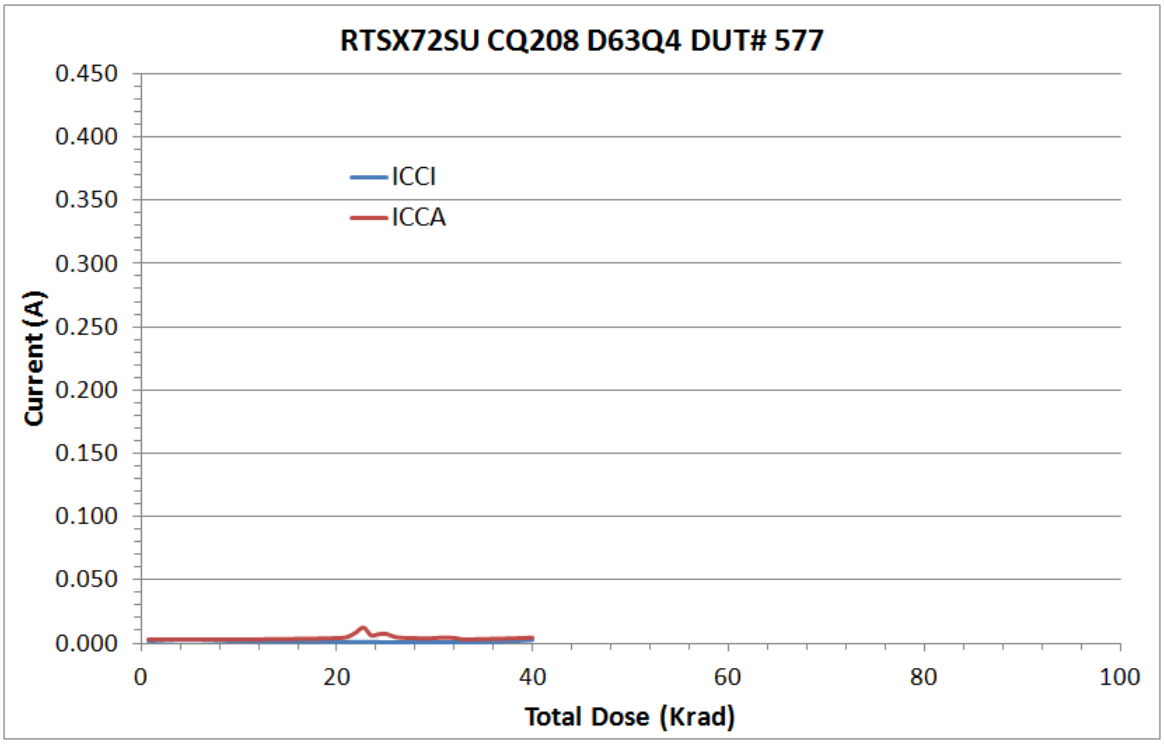


Figure 6 DUT 577 Influx ICCA and ICCI

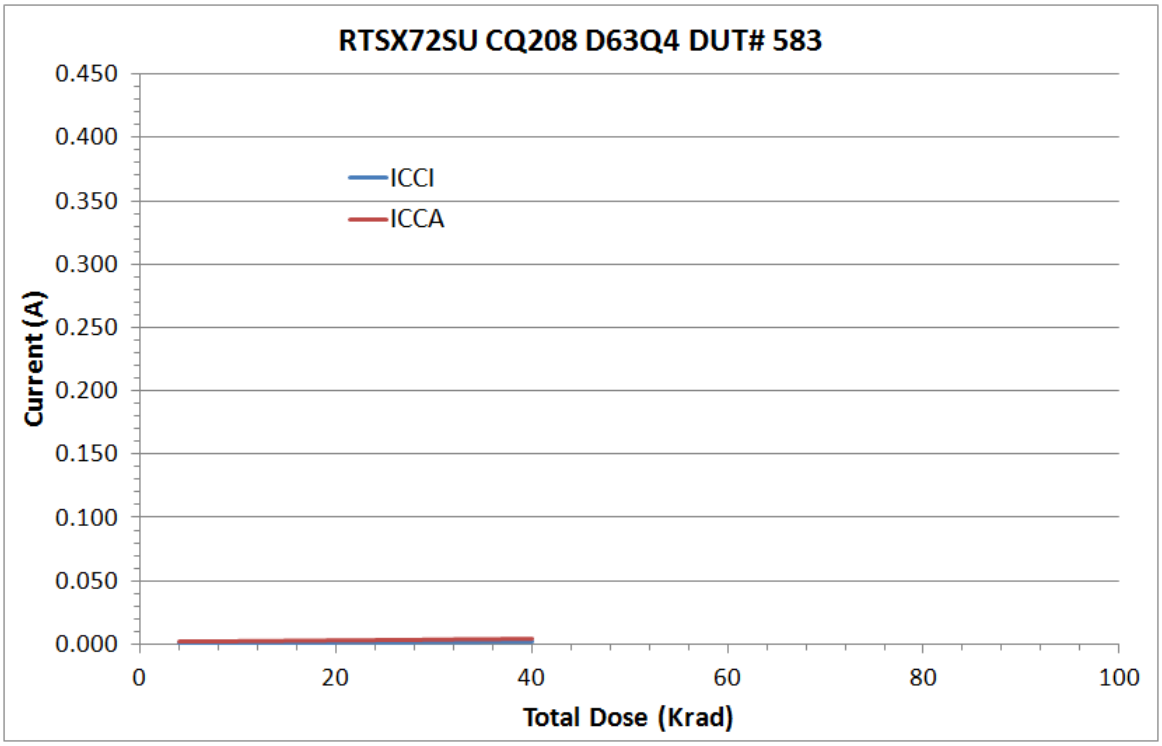


Figure 7 DUT 583 Influx ICCA and ICCI

C. Input Logic Threshold (VIL/VIH)

Table 4a through Table 4c list the pre-irradiation and post-annealing input logic thresholds. All data are within the specification limits. The post-annealing shift in every case is very small.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

DUT	380 (100 krad)				518 (100 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1320	1165	1495	1465	1345	1360	1490	1485
DAH/QA0H	1385	1425	1365	1425	1185	1400	1380	1360
ENCNTRH/YO0	1440	1385	1370	1440	1440	1415	1380	1370
IDII0/IDIO0	1350	1440	1395	1460	1305	1230	1405	1425
IDII1/IDIO1	1455	1365	1370	1425	1455	1410	1365	1365
IDII2/IDIO2	1330	1385	1390	1410	1345	1290	1415	1425
IDII3/IDIO3	1325	1390	1405	1350	1325	1265	1410	1395
IDII4/IDIO4	1340	1335	1415	1390	1385	1310	1440	1425
IDII5/IDIO5	1440	1370	1375	1380	1440	1445	1400	1375
IDII6/IDIO6	1380	1385	1385	1490	1385	1380	1395	1385
IDII7/IDIO7	1435	1390	1430	1395	1435	1315	1435	1375

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

DUT	536 (60 krad)				552 (60 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1325	1225	1510	1465	1310	1375	1510	1505
DAH/QA0H	1375	1460	1375	1445	1380	1395	1380	1385
ENCNTRH/YO0	1440	1385	1375	1435	1445	1425	1385	1410
IDII0/IDIO0	1285	1480	1415	1450	1270	1220	1445	1475
IDII1/IDIO1	1460	1275	1370	1445	1490	1425	1370	1410
IDII2/IDIO2	1345	1455	1395	1390	1345	1355	1485	1460
IDII3/IDIO3	1385	1395	1405	1390	1325	1440	1400	1425
IDII4/IDIO4	1335	1285	1420	1425	1385	1420	1430	1400
IDII5/IDIO5	1430	1415	1360	1375	1440	1475	1400	1395
IDII6/IDIO6	1395	1425	1395	1400	1385	1425	1395	1430
IDII7/IDIO7	1440	1395	1435	1410	1440	1295	1435	1395

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

DUT	577 (40 krad)				583 (40 krad)			
Input Pin	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
	VIL (mV)		VIH (mV)		VIL (mV)		VIH (mV)	
DA/QA0	1320	1225	1530	1445	1315	1240	1550	1455
DAH/QA0H	1395	1450	1390	1420	1390	1455	1395	1430
ENCNTRH/YO0	1445	1440	1390	1435	1430	1385	1385	1400
IDII0/IDIO0	1255	1440	1470	1410	1290	1390	1435	1450
IDII1/IDIO1	1490	1220	1375	1430	1470	1305	1385	1445
IDII2/IDIO2	1380	1470	1410	1400	1310	1465	1405	1395
IDII3/IDIO3	1450	1425	1415	1375	1335	1420	1410	1365
IDII4/IDIO4	1395	1260	1440	1570	1390	1295	1430	1575
IDII5/IDIO5	1450	1350	1390	1380	1450	1360	1370	1385
IDII6/IDIO6	1400	1430	1395	1395	1420	1430	1400	1390
IDII7/IDIO7	1445	1385	1440	1385	1445	1400	1440	1400

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 5 and 6. The post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Current

Sourcing Current	380 (100 krad)		518 (100 krad)		536 (60 krad)		552 (60 krad)		577 (40 krad)		583 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	11	10	11	12	11	10	11	11	11	10	11	10
12 mA	119	115	120	132	117	114	117	128	121	112	119	114
20 mA	197	191	200	220	195	189	195	213	201	187	199	190
50 mA	495	479	501	551	491	476	490	534	506	470	499	476
100 mA	1014	982	1026	1125	1004	976	1004	1091	1036	964	1020	975

Table 6 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Current

Sourcing Current	380 (100 krad)		518 (100 krad)		536 (60 krad)		552 (60 krad)		577 (40 krad)		583 (40 krad)	
	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
1 mA	4979	4975	4979	4975	4978	4976	4979	4976	4978	4977	4978	4978
8 mA	4847	4846	4845	4832	4844	4846	4846	4836	4843	4847	4843	4847
20 mA	4614	4617	4609	4583	4608	4619	4611	4590	4605	4617	4606	4617
50 mA	3987	3997	3970	3908	3966	4003	3977	3927	3961	3994	3961	3993
100 mA	2569	2567	2500	2346	2468	2581	2514	2399	2481	2535	2464	2543

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

Table 7 Radiation-Induced Propagation-Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Anneal (µs)	Degradation (%)
380	100 krad	1.42	1.40	-1.07%
518	100 krad	1.40	1.39	-1.15%
536	60 krad	1.39	1.35	-3.54%
552	60 krad	1.41	1.37	-3.44%
577	40 krad	1.43	1.39	-2.93%
583	40 krad	1.42	1.37	-3.79%

F. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

Figure 9a DUT 380 Pre-Irradiation Rising Edge

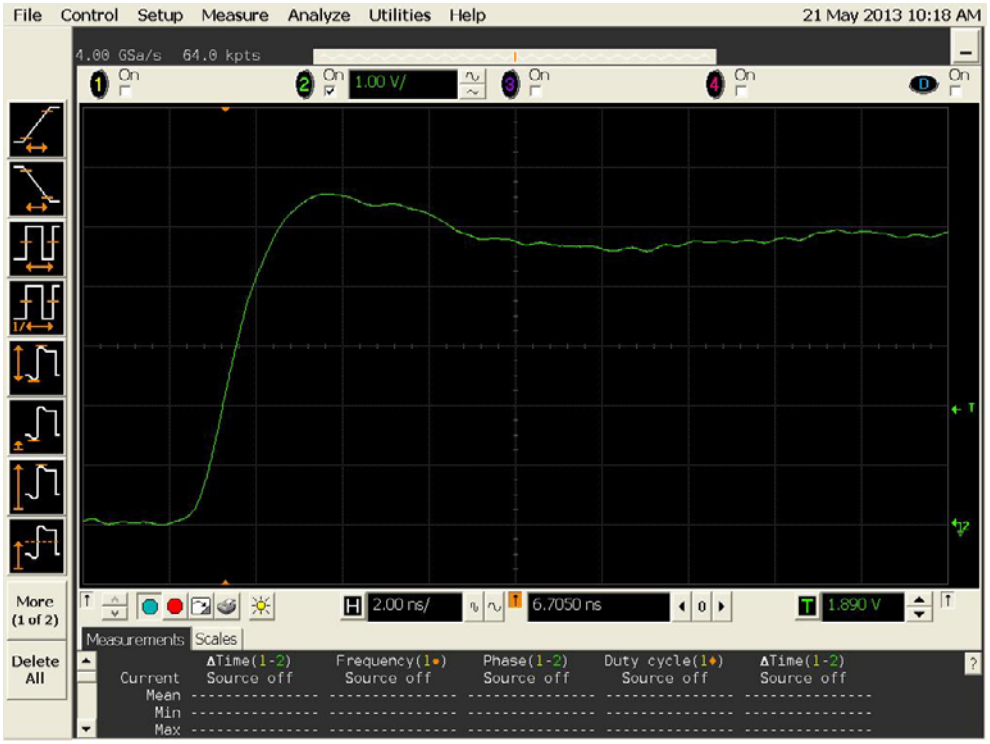


Figure 9b DUT 380 Post-Annealing Rising Edge

Figure 10a DUT 518 Pre-Irradiation Rising Edge

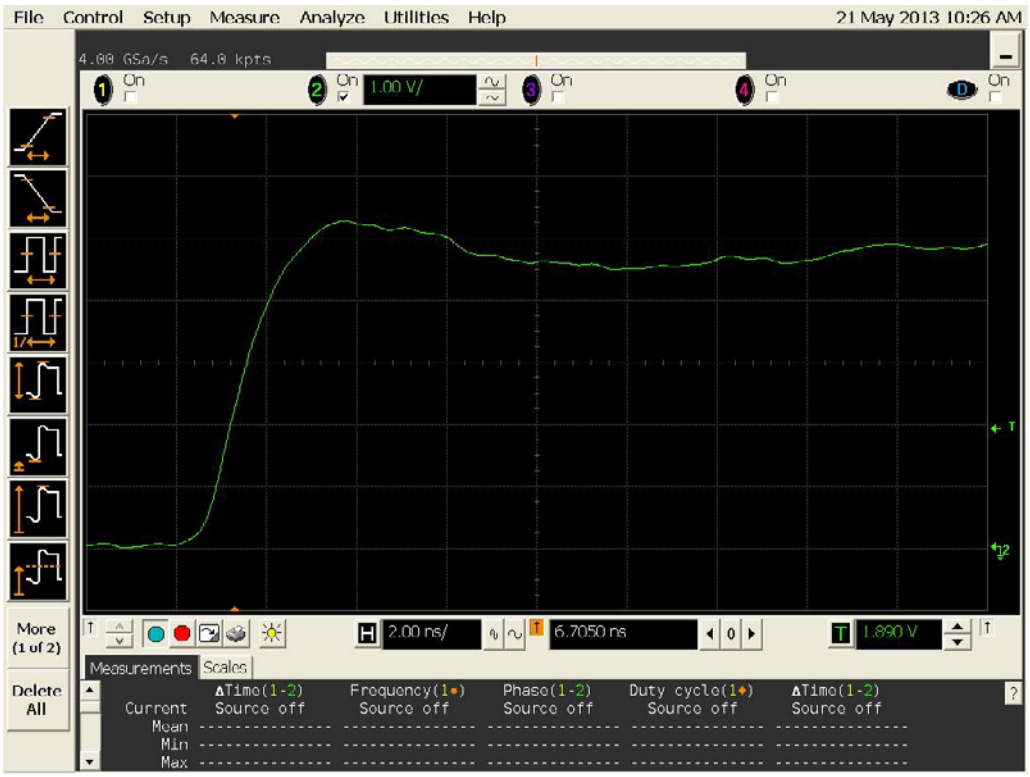


Figure 10b DUT 518 Post-Annealing Rising Edge

Figure 11a DUT 536 Pre-Radiation Rising Edge

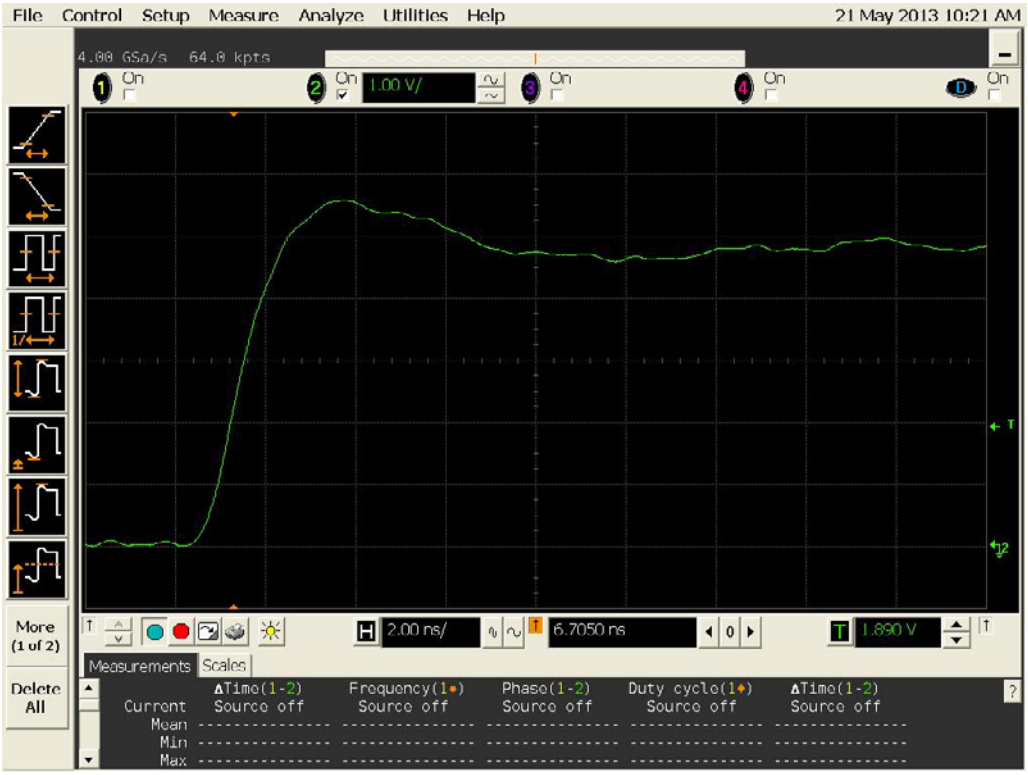


Figure 11b DUT 536 Post-Annealing Rising edge

Figure 12a DUT 552 Pre-Irradiation Rising Edge

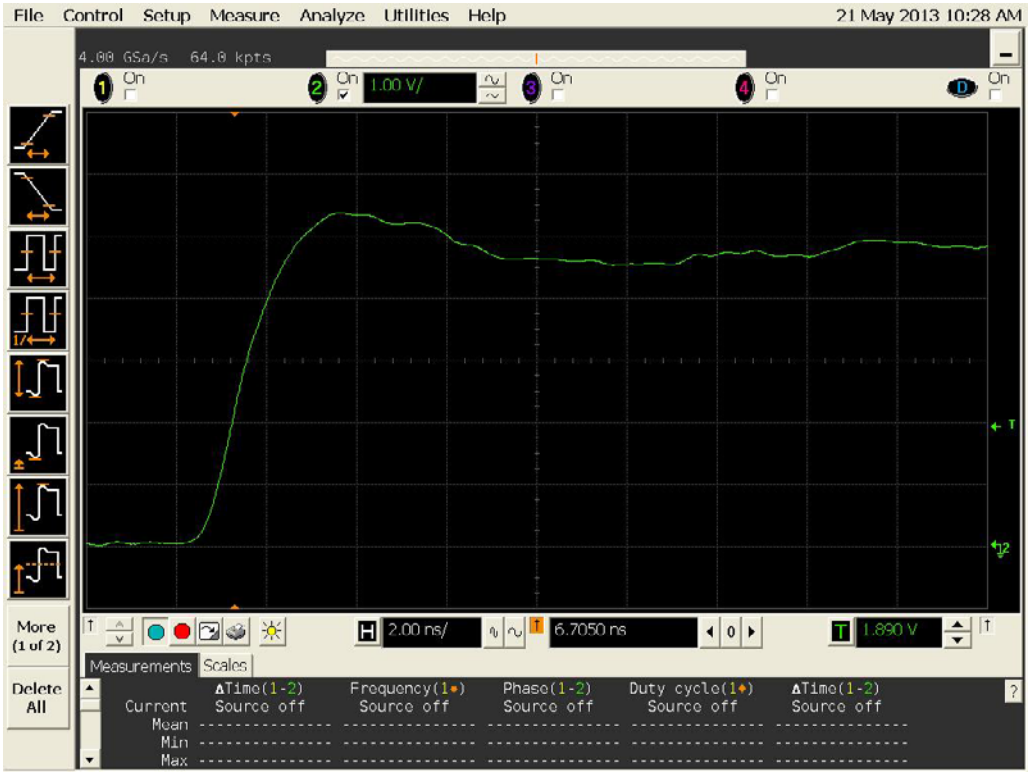


Figure 12b DUT 552 Post-Annealing Rising Edge

Figure 13a DUT 577 Pre-Irradiation Rising Edge

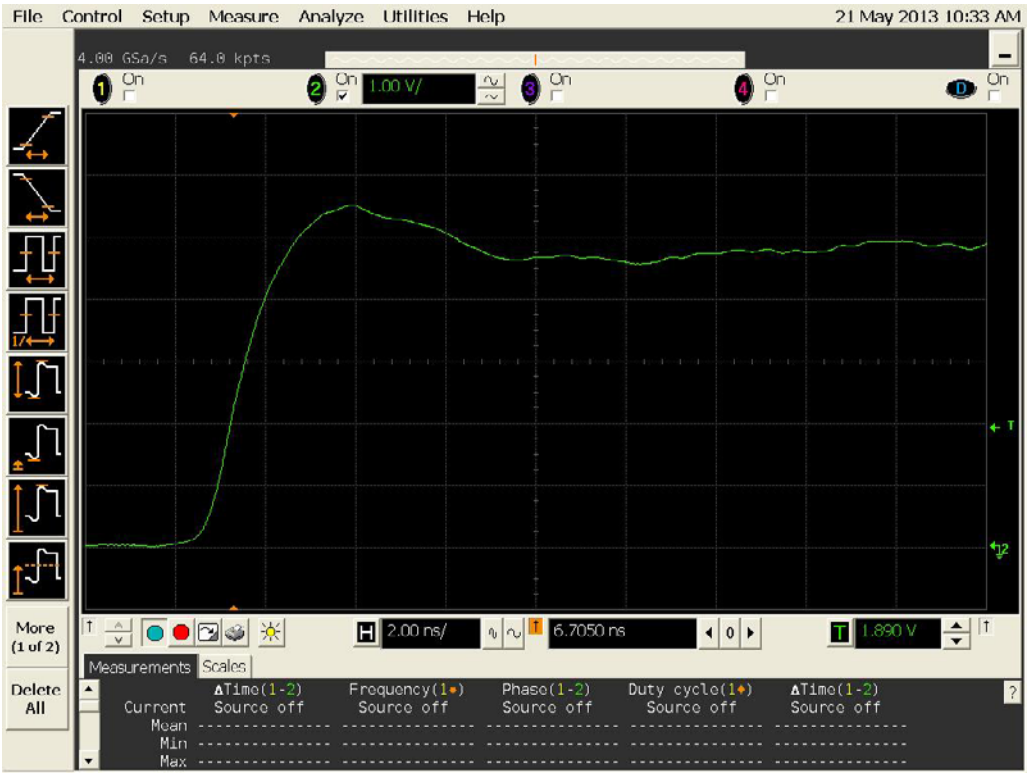


Figure 13b DUT 577 Post-Annealing Rising Edge

Figure 14a DUT 583 Pre-Irradiation Rising Edge

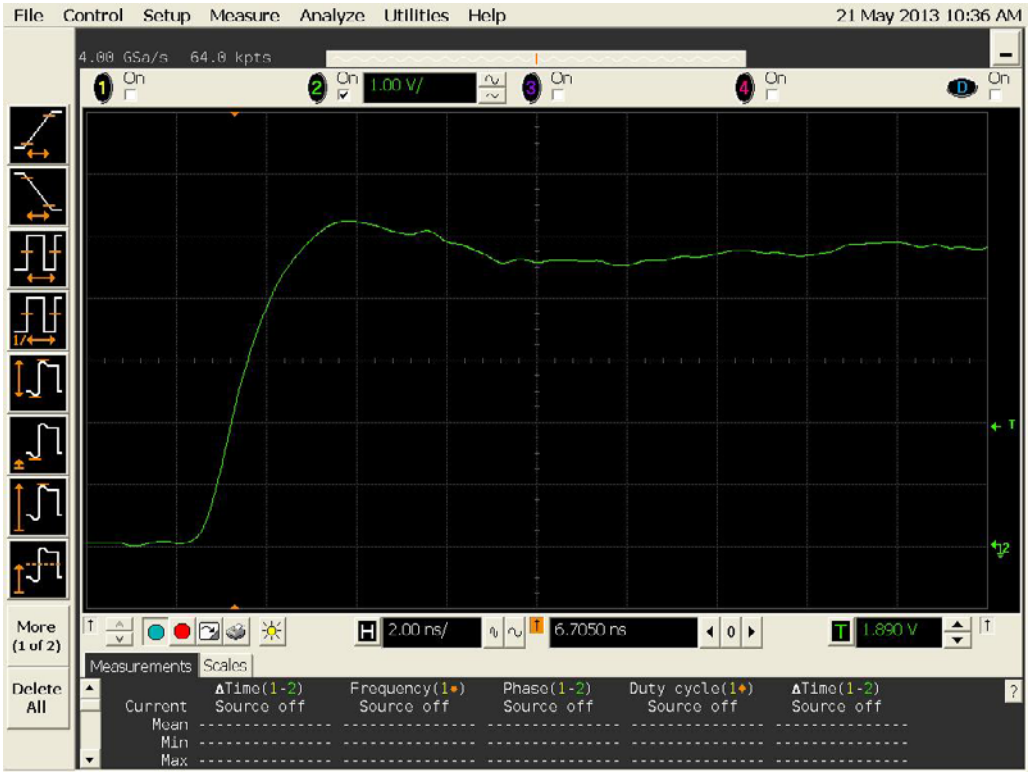


Figure 14b DUT 583 Post-Annealing Rising Edge

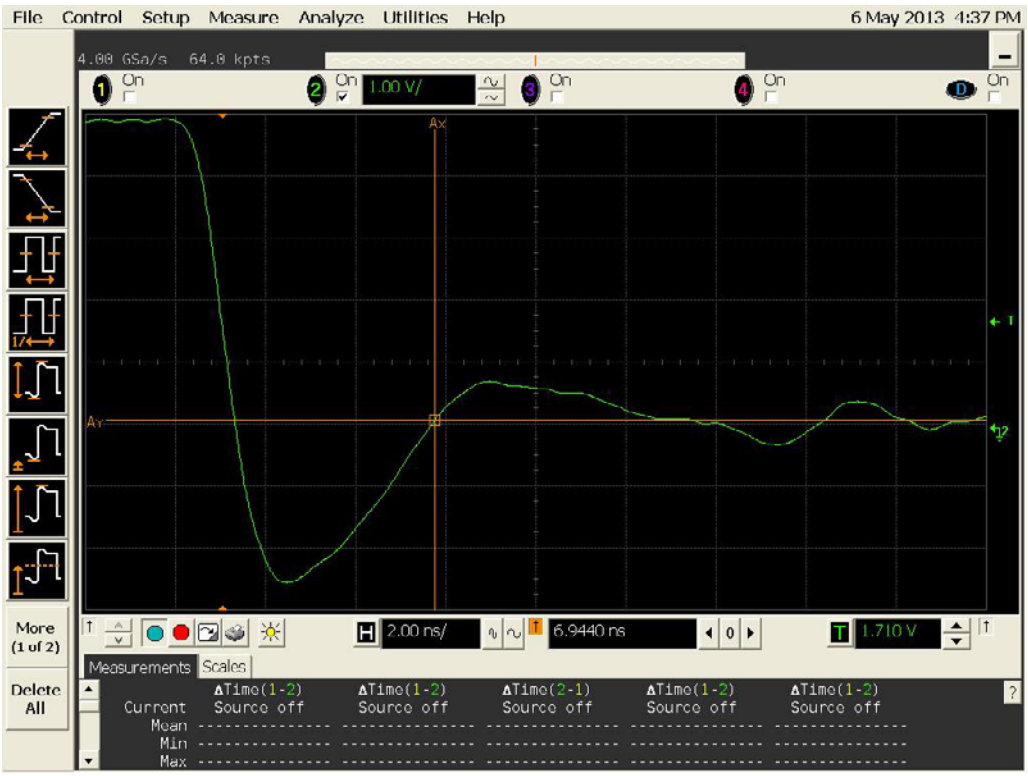


Figure 15a DUT 380 Pre-Radiation Falling Edge

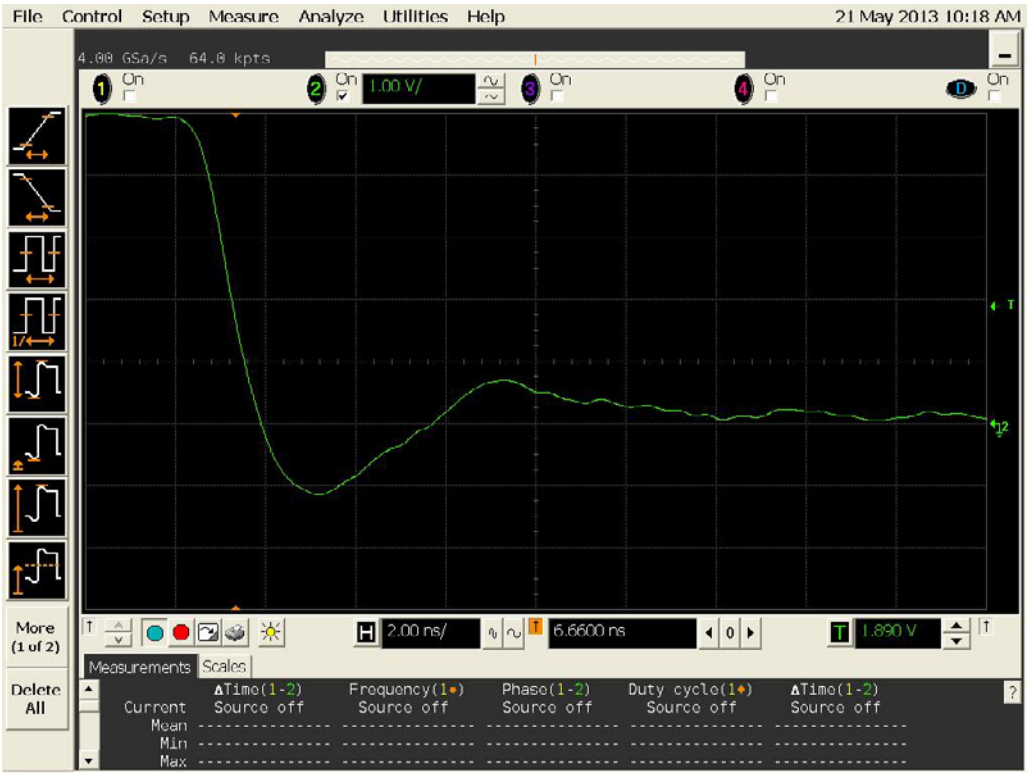


Figure 15b DUT 380 Post-Annealing Falling Edge

Figure 16a DUT 518 Pre-Irradiation Falling Edge

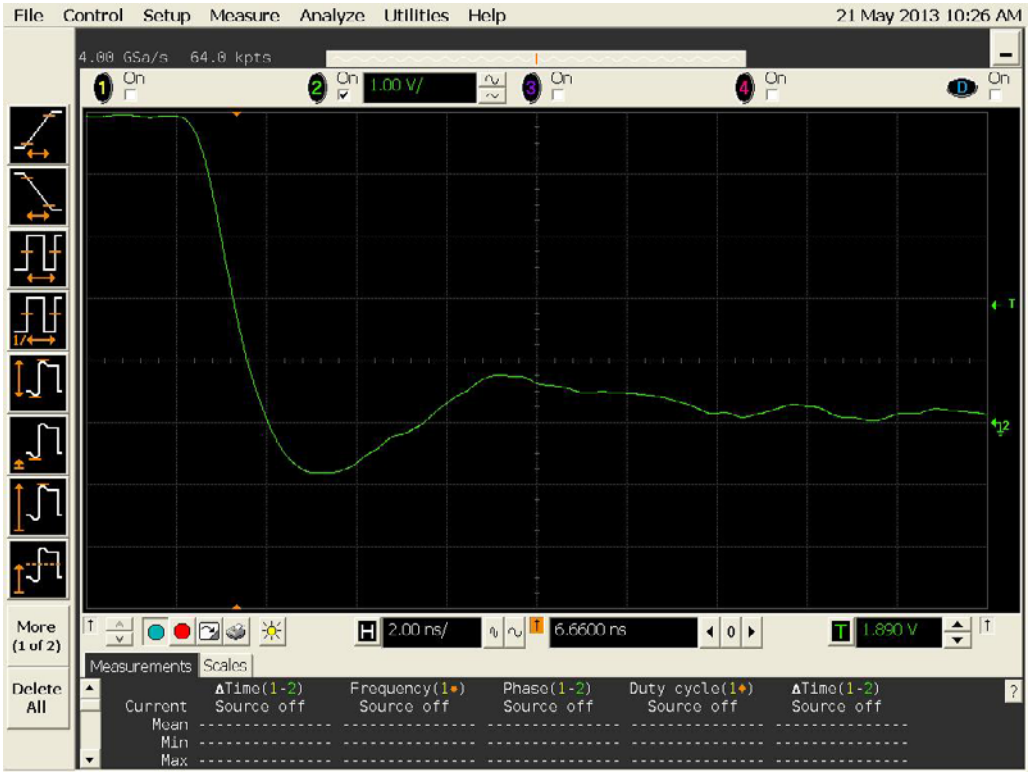


Figure 16b DUT 518 Post-Annealing Falling Edge

Figure 17a DUT 536 Pre-Irradiation Falling Edge

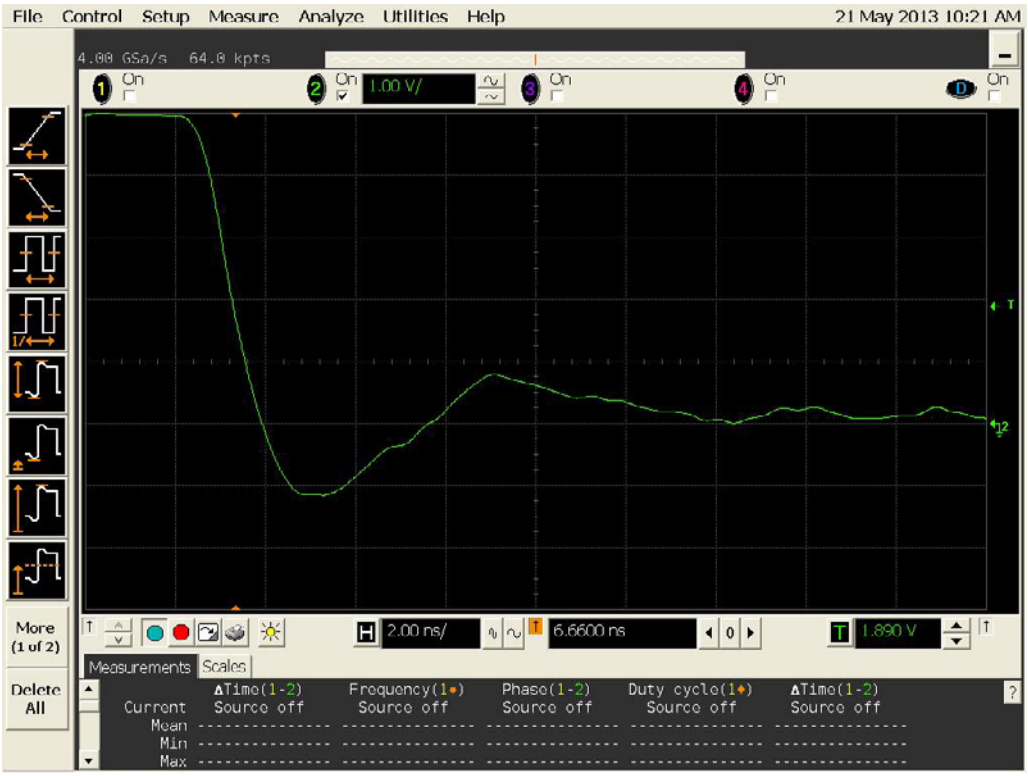


Figure 17b DUT 536 Post-Annealing Falling Edge

Figure 18a DUT 552 Pre-Irradiation Falling Edge

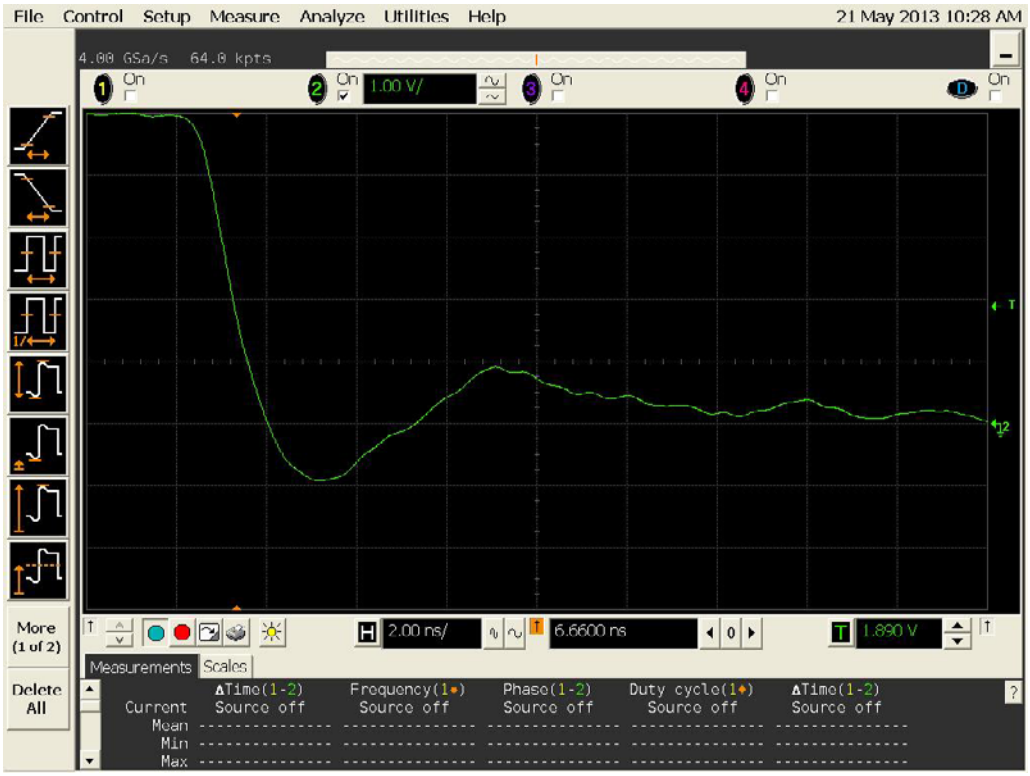


Figure 18b DUT 552 Post-Annealing Falling Edge

Figure 19a DUT 577 Pre-Irradiation Falling Edge

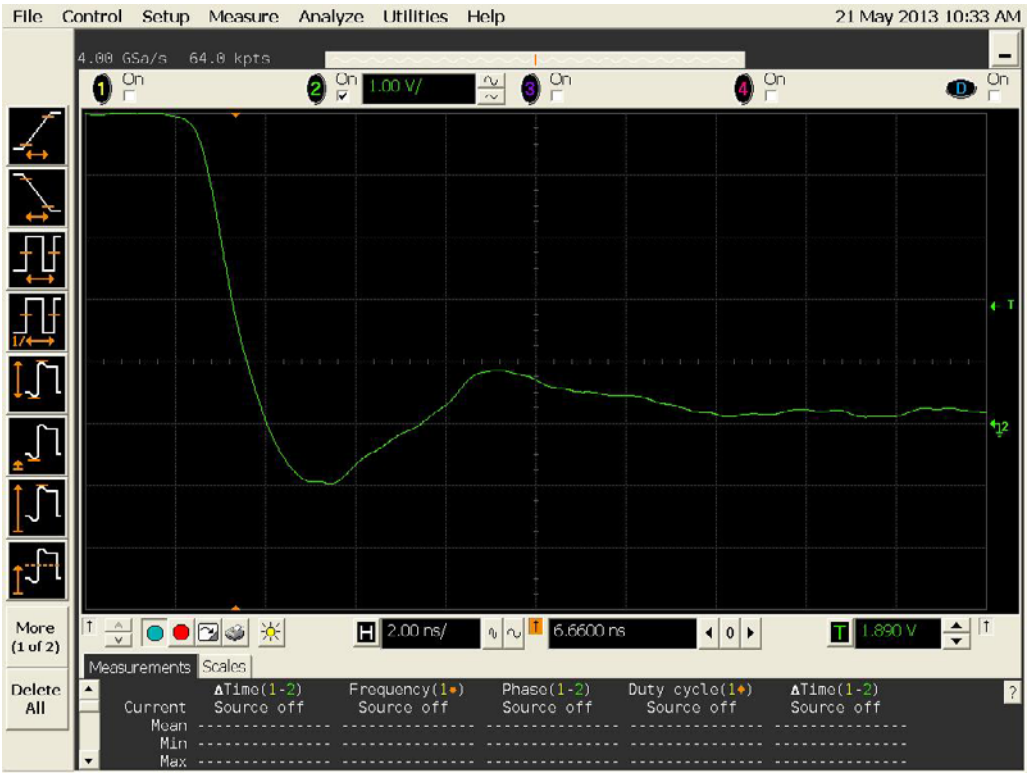


Figure 19b DUT 577 Post-Annealing Falling Edge

Figure 20a DUT 583 Pre-Irradiation Falling Edge

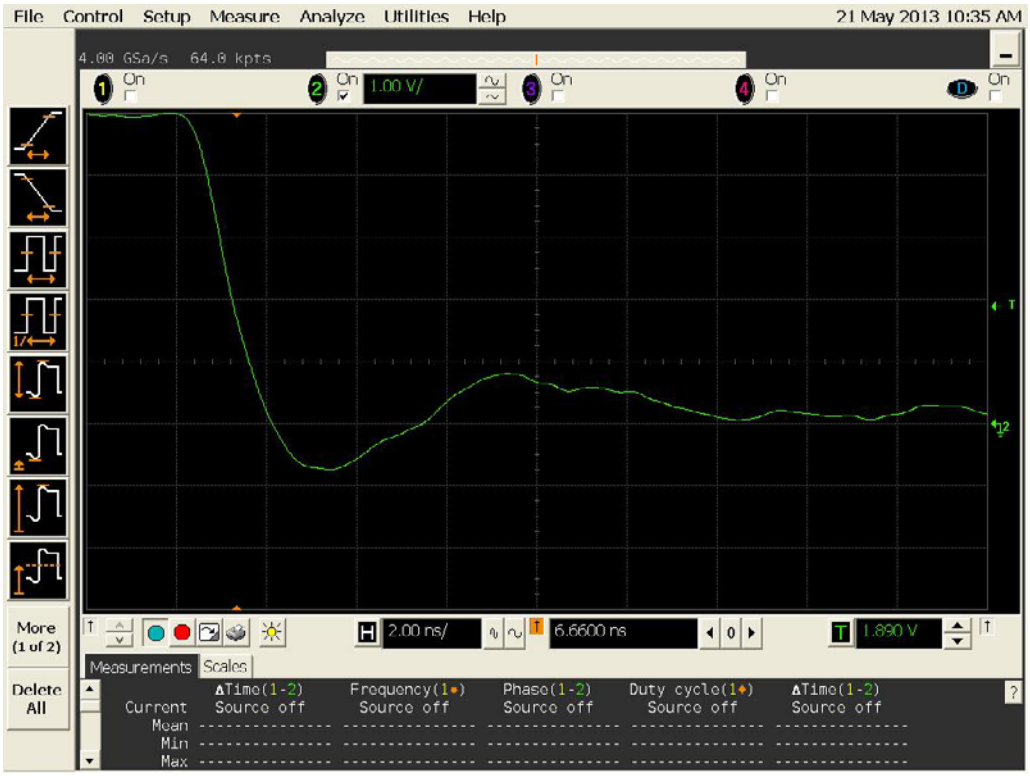
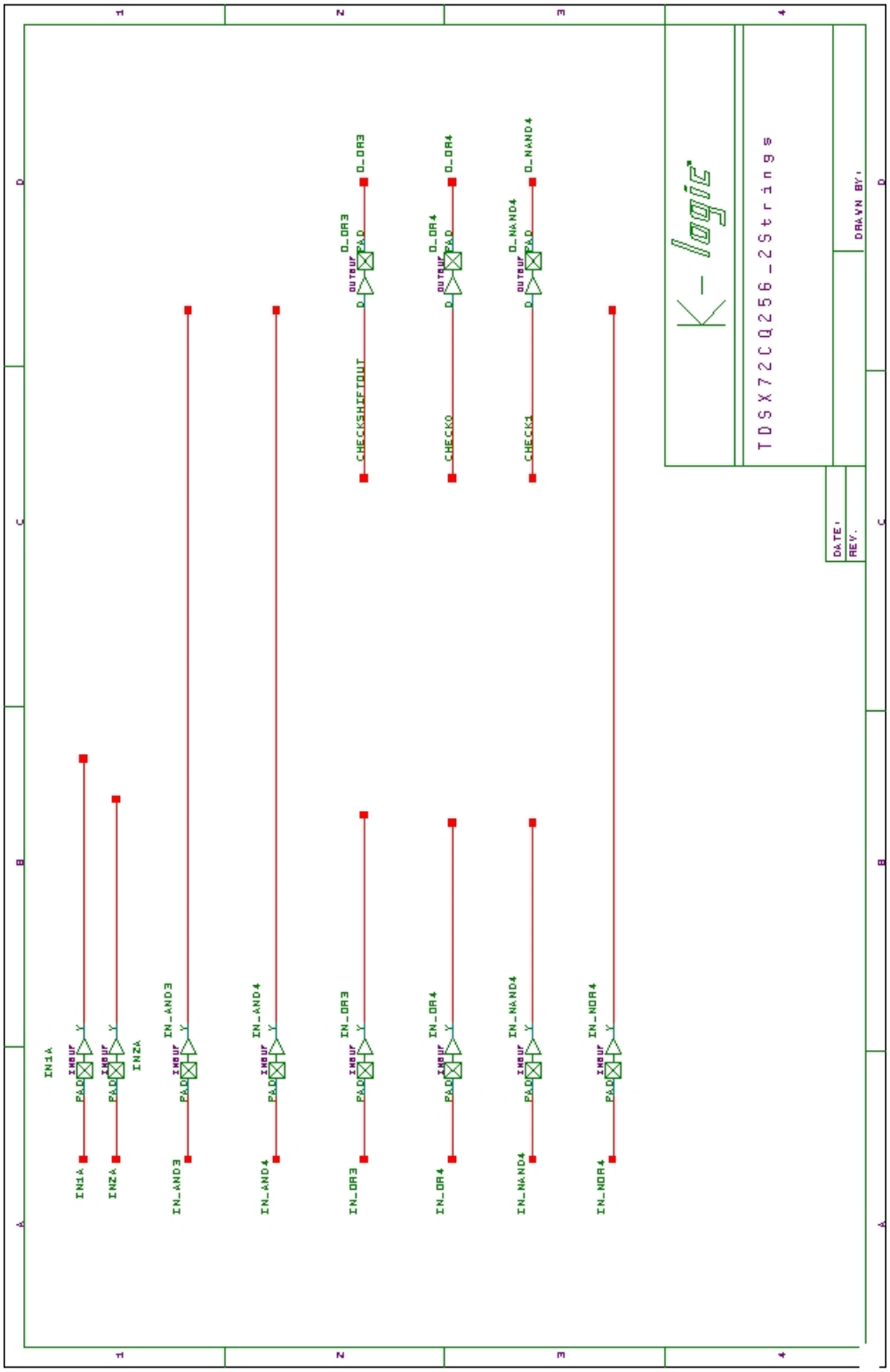
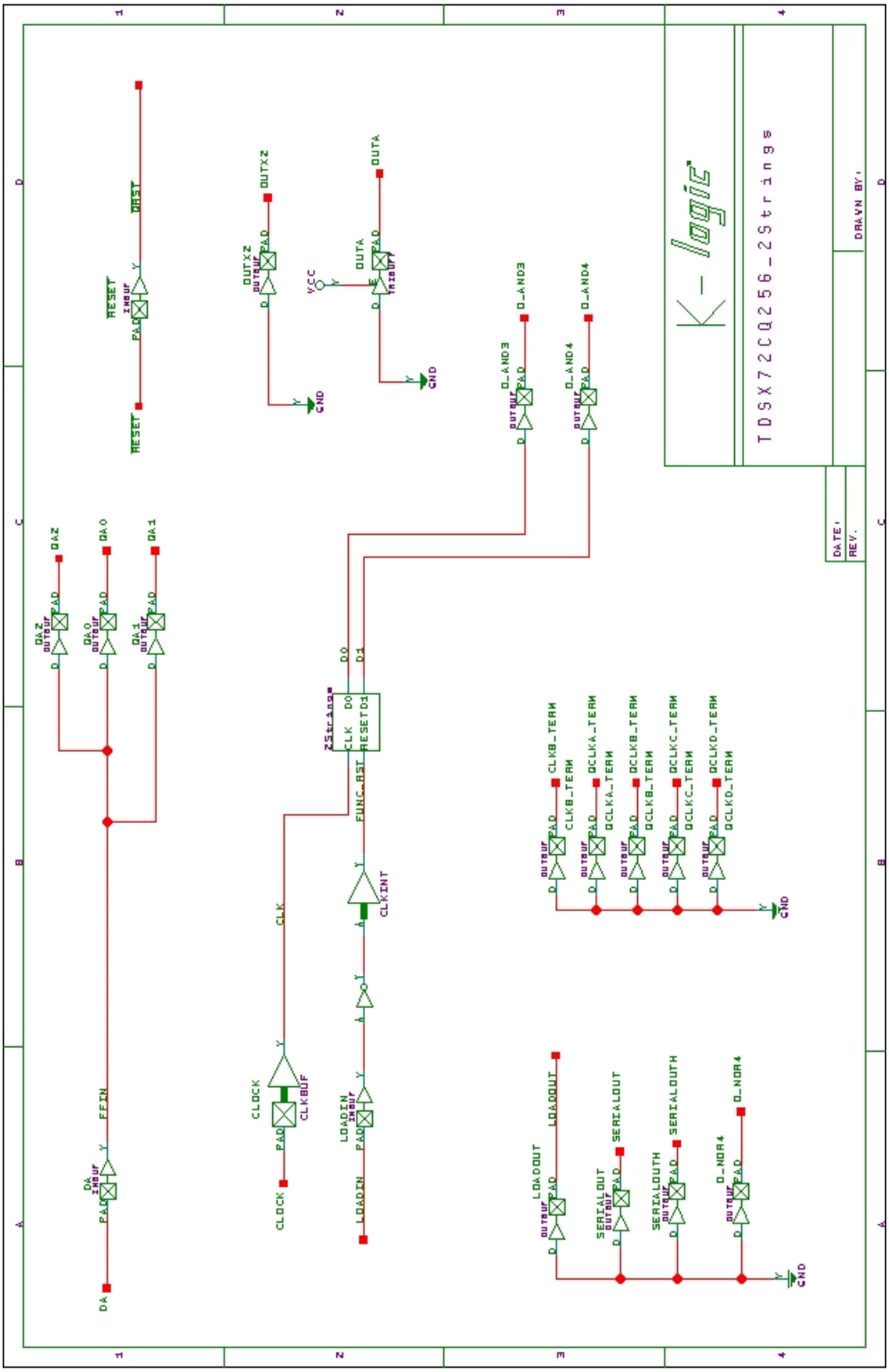


Figure 20b DUT 583 Post-Annealing Falling Edge

Appendix A: DUT Design Schematics

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D0
D1
RESET01
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CLKINT
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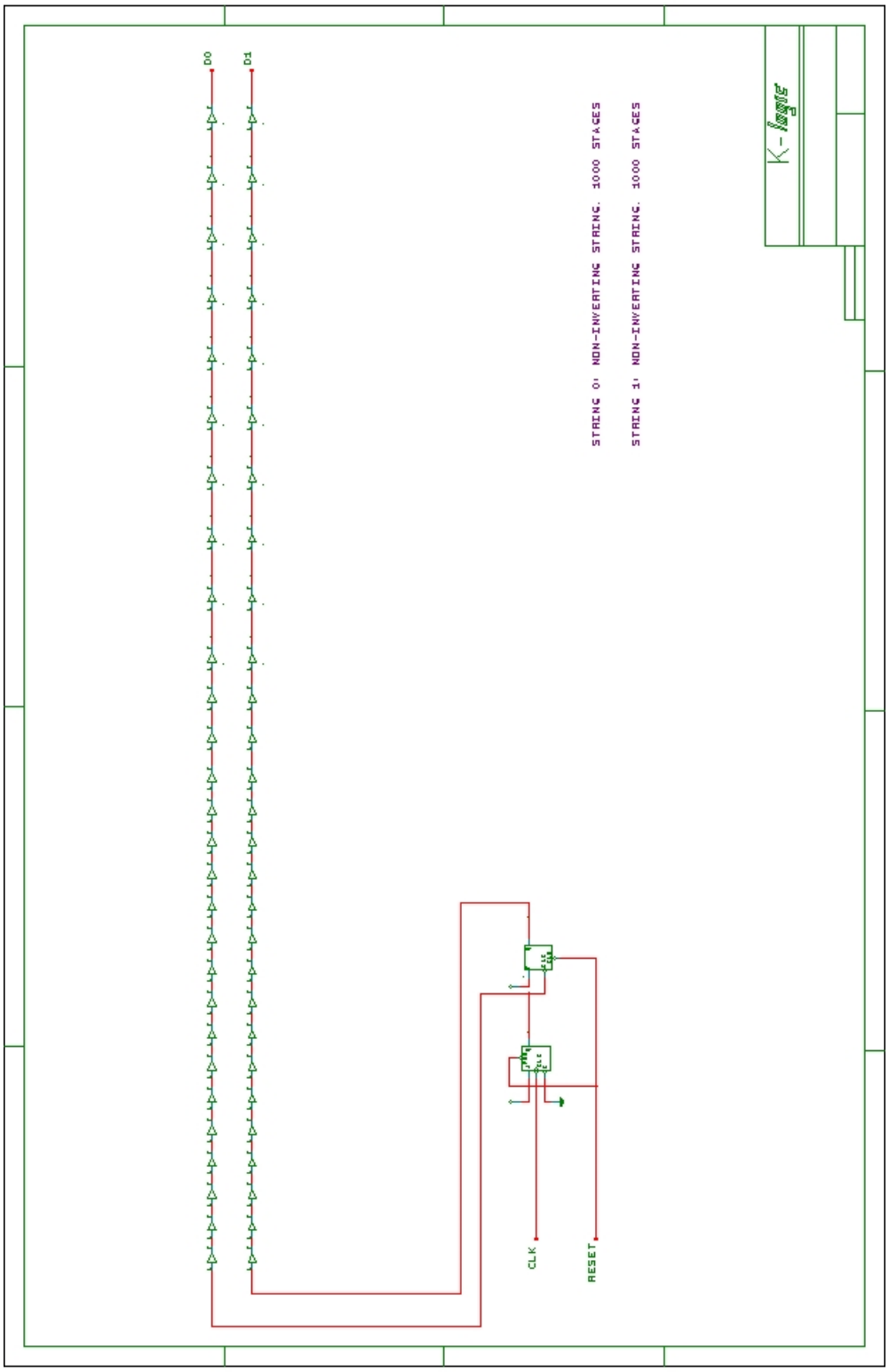
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D1
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STRING 1: NON-INVERTING STRING, 1000 STAGES
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RESET


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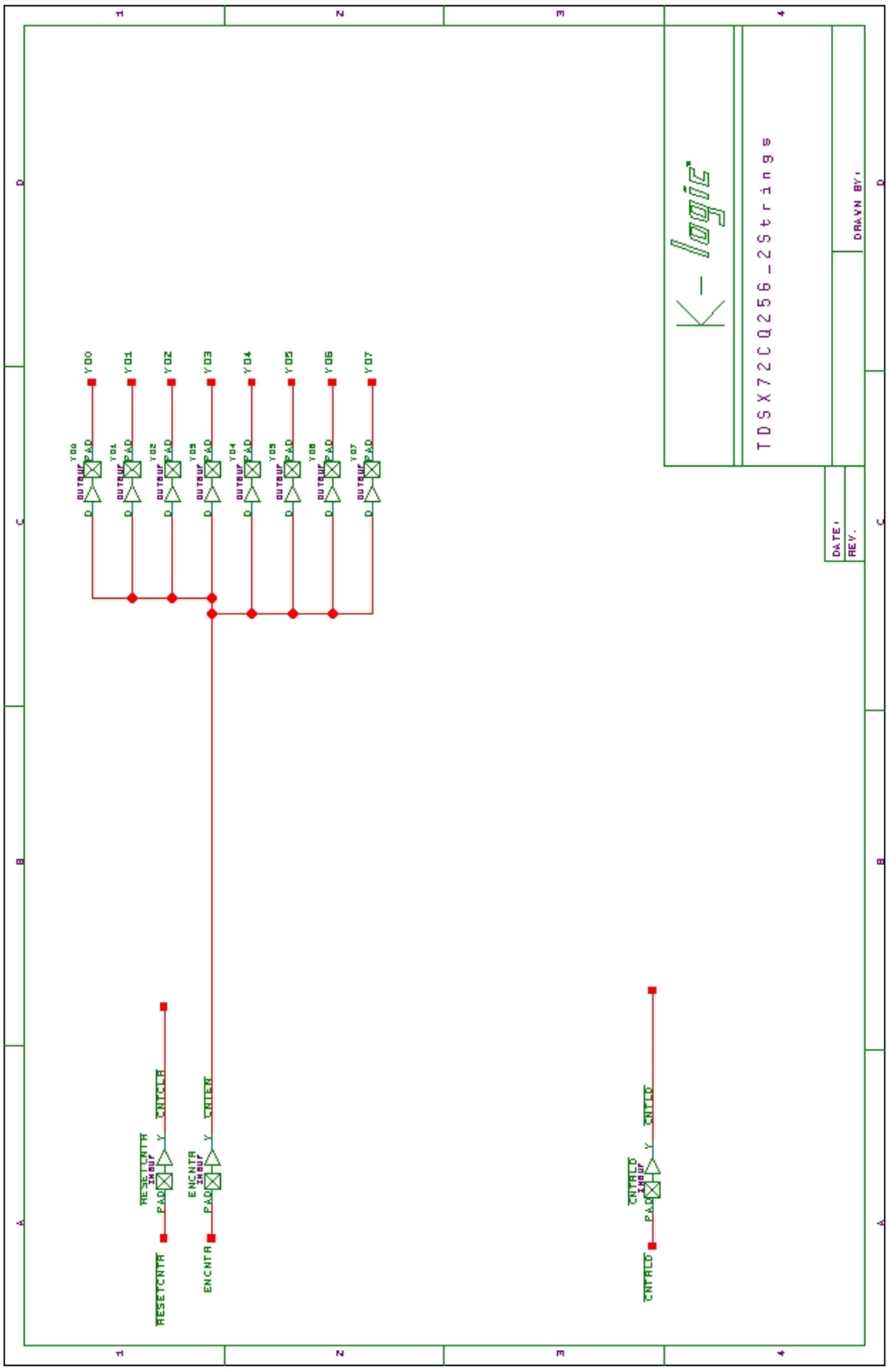
DATE:
REV.
YPRESERVE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Y07
OUTBUF
PAD
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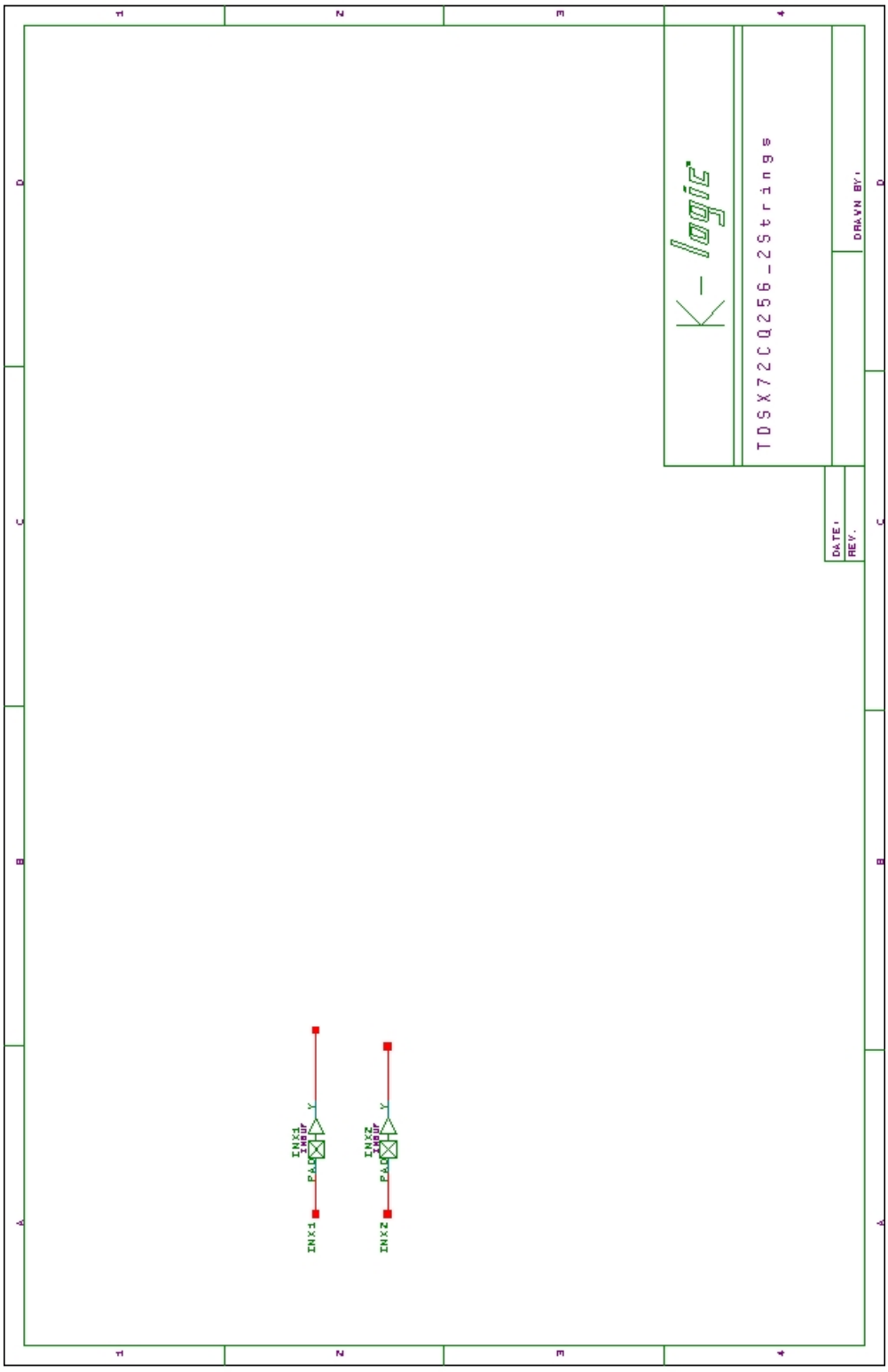
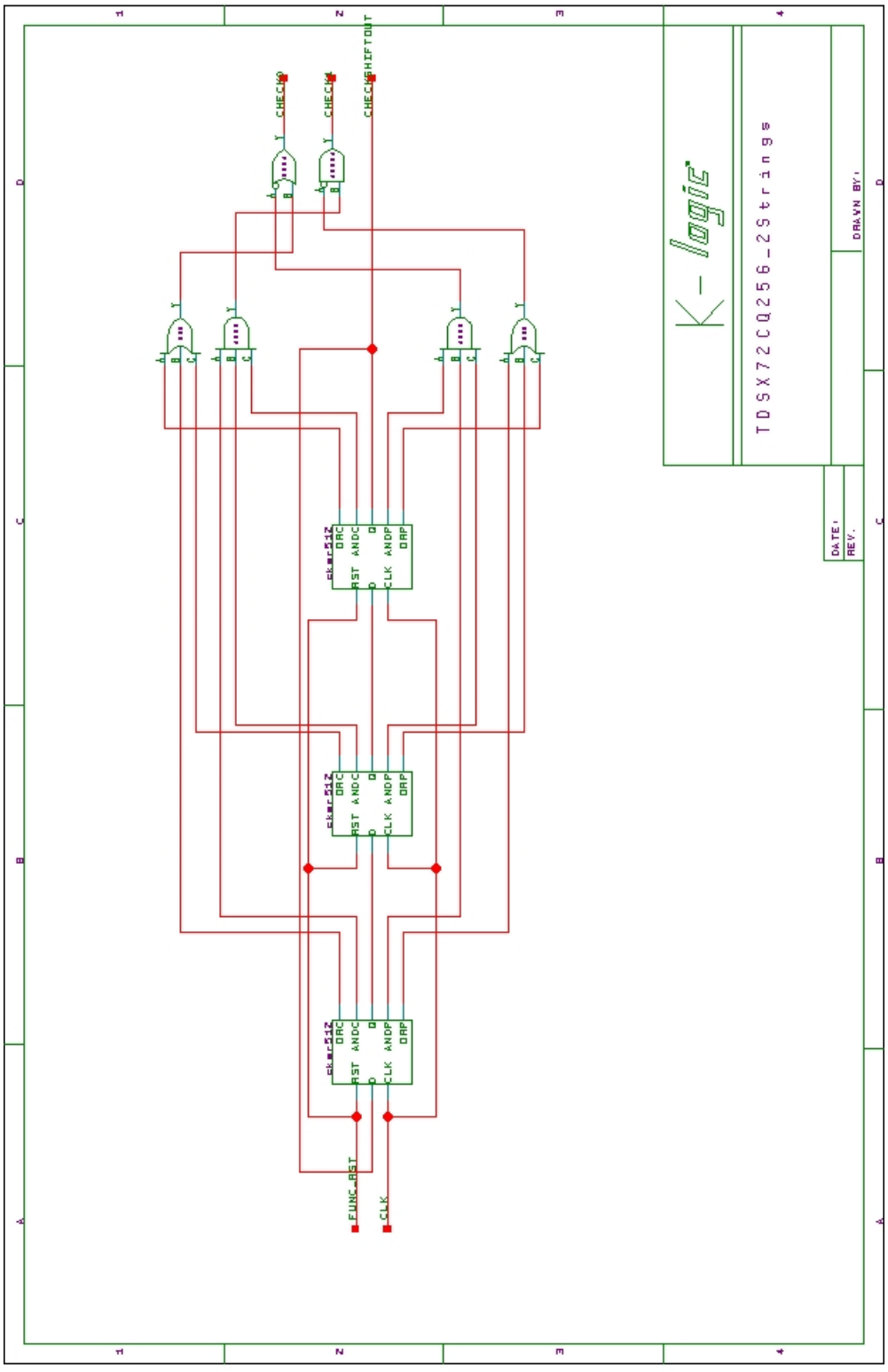
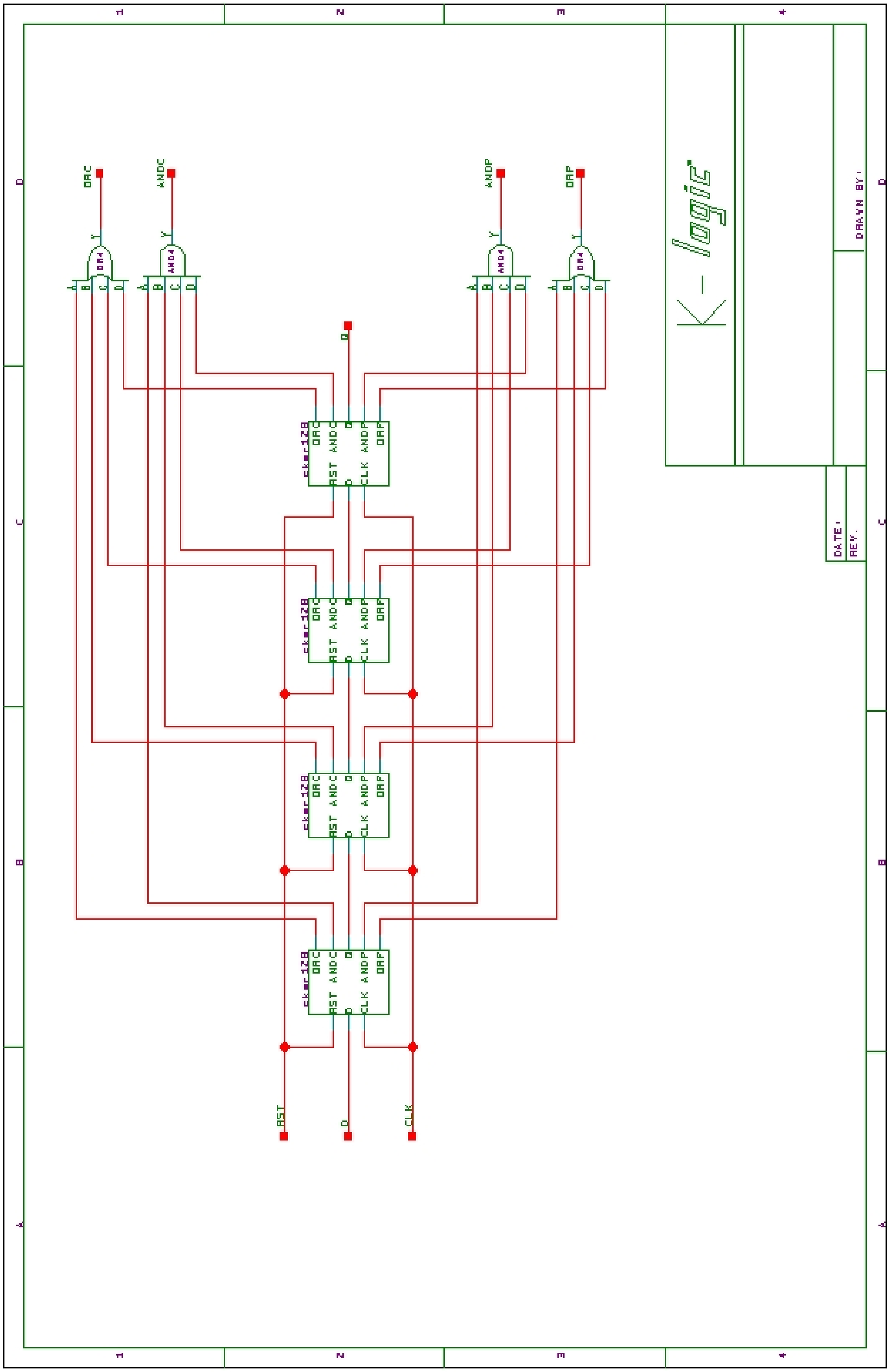
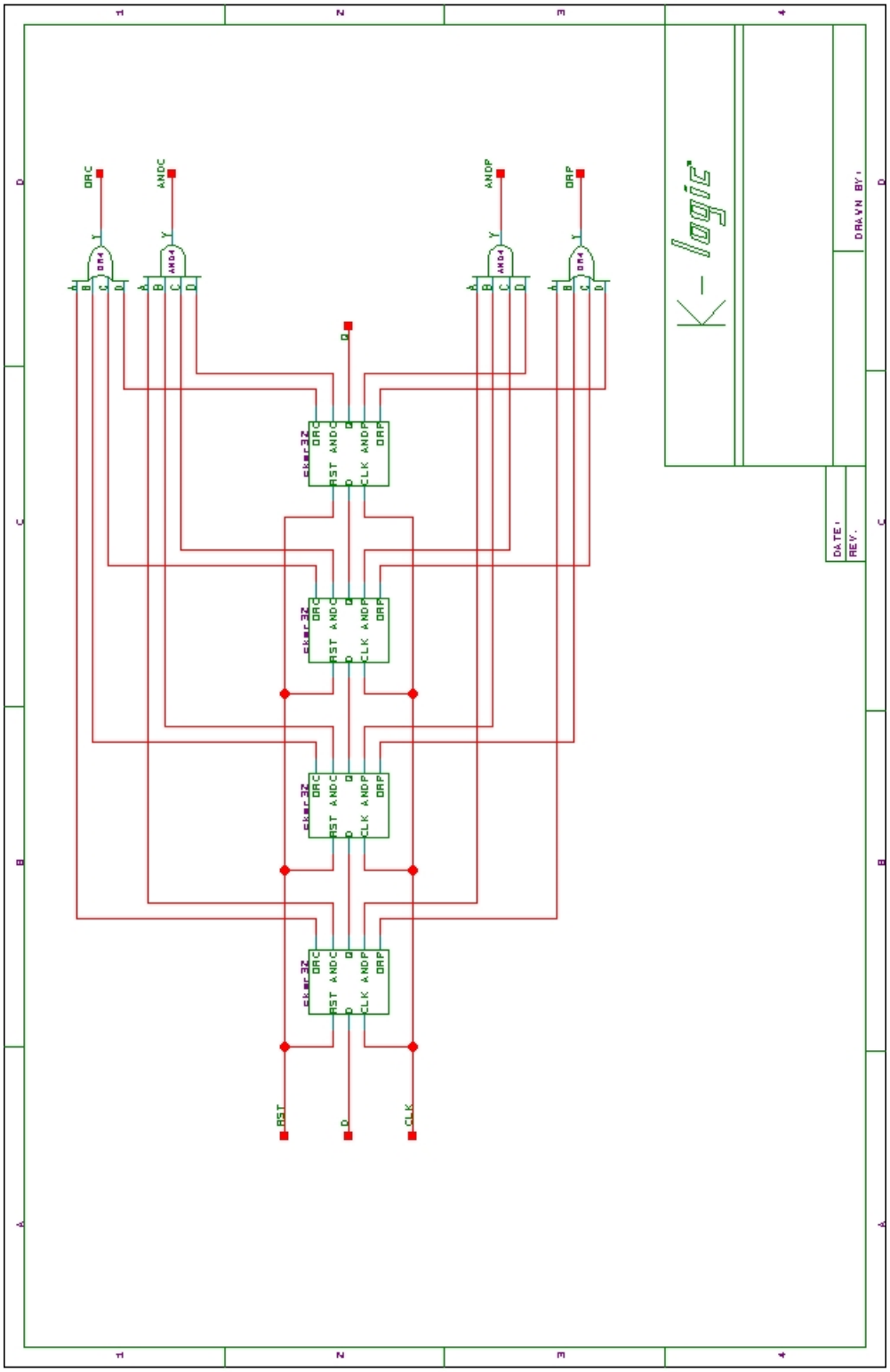
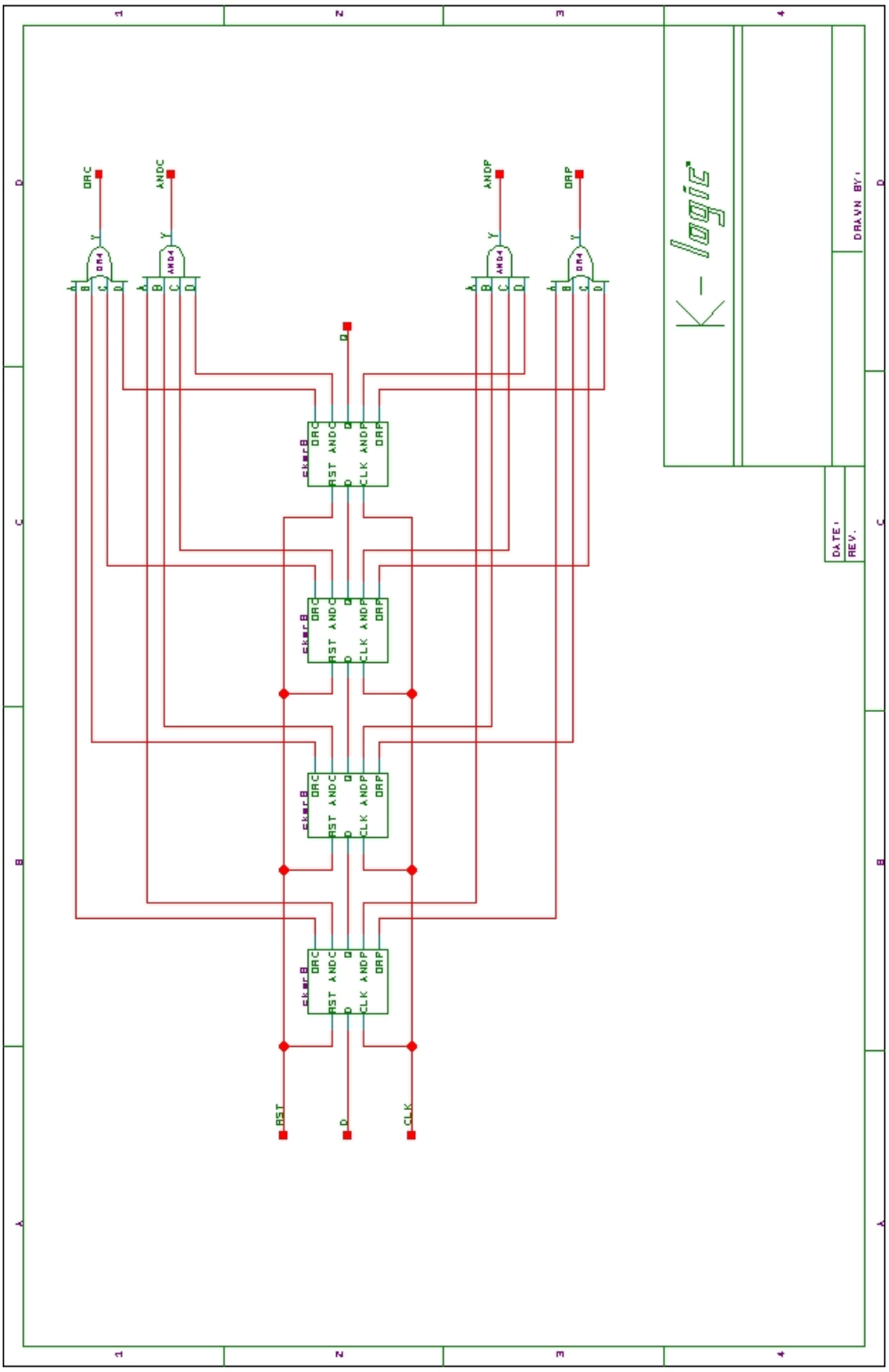
ENCNTR
CNTRCLR
CNTRCLD

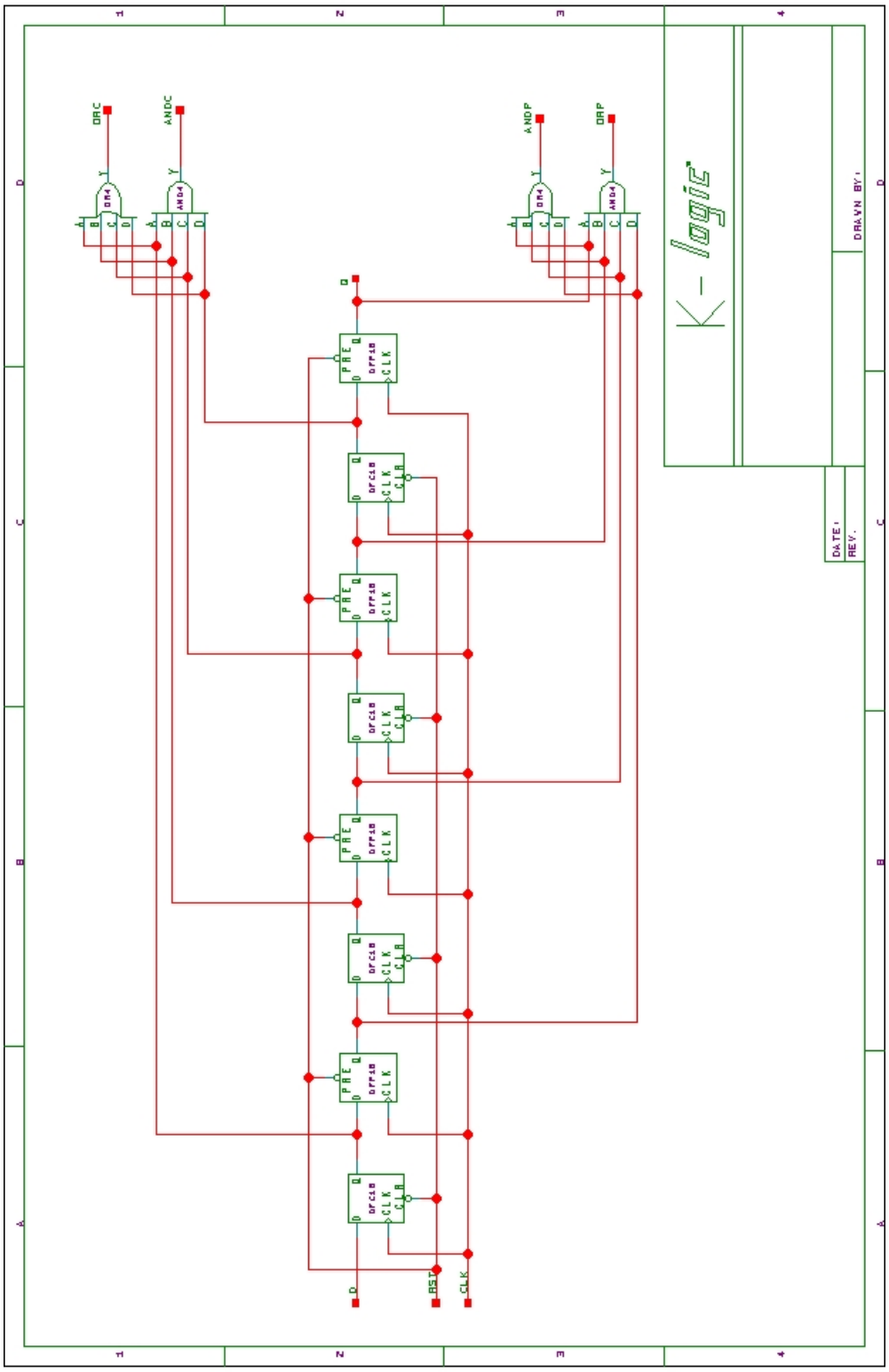

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV:
INX1
INX2

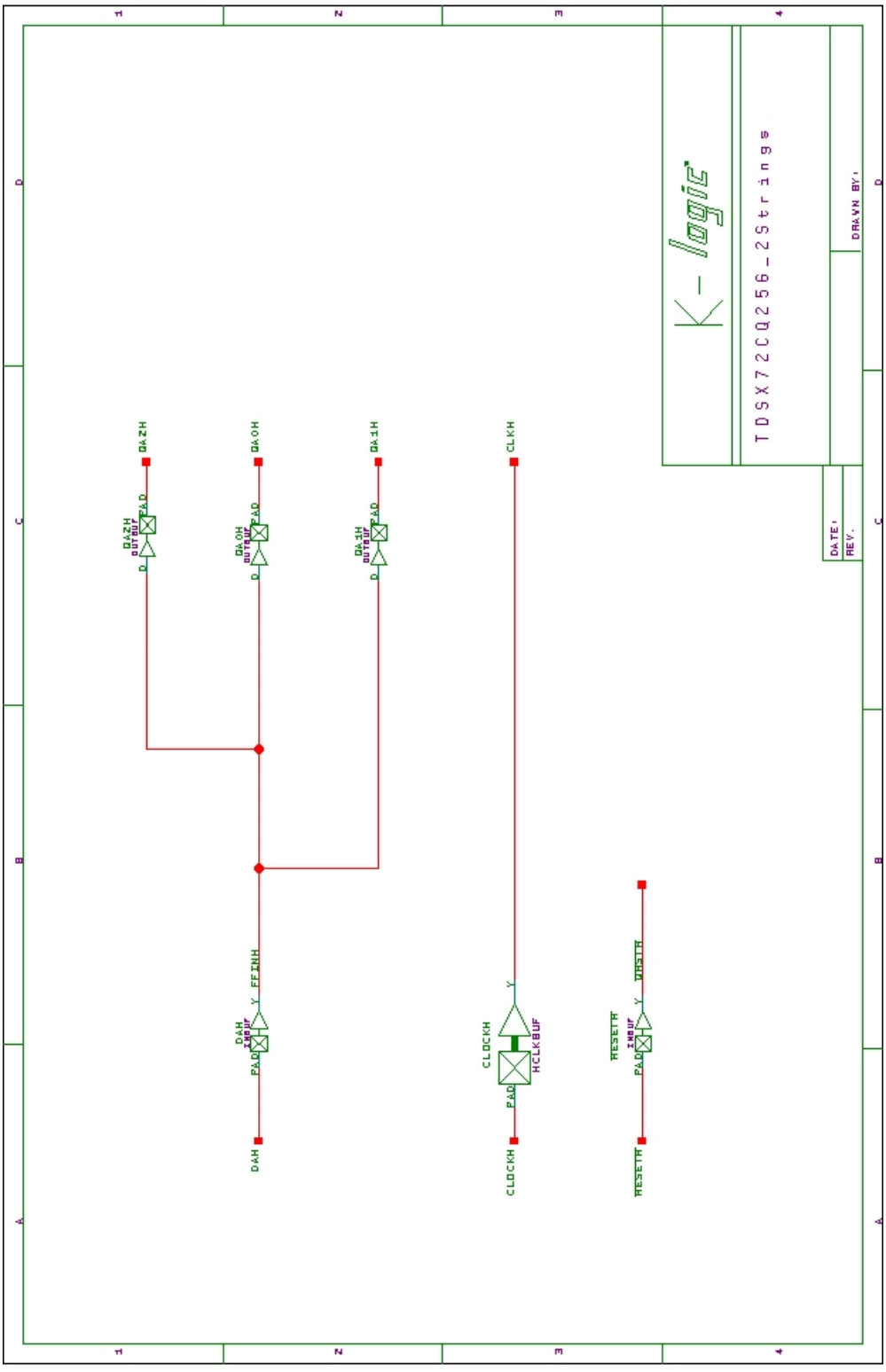

CHECK0
CHECK1
CHECKSHIFTOUT
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
FUNC_RST
CLK

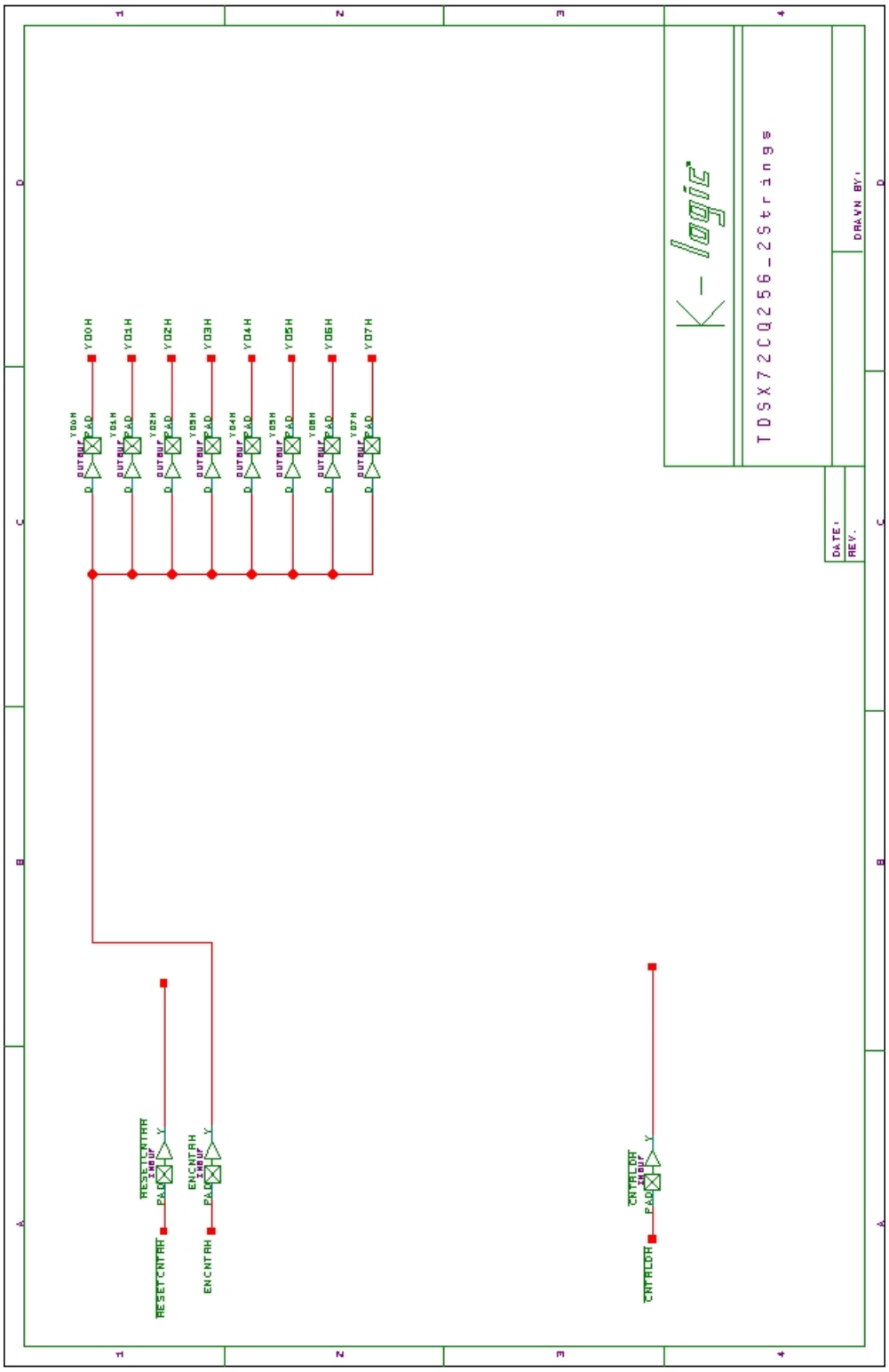

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
skmr128
K - logic
DRAWN BY:
DATE:
REV.

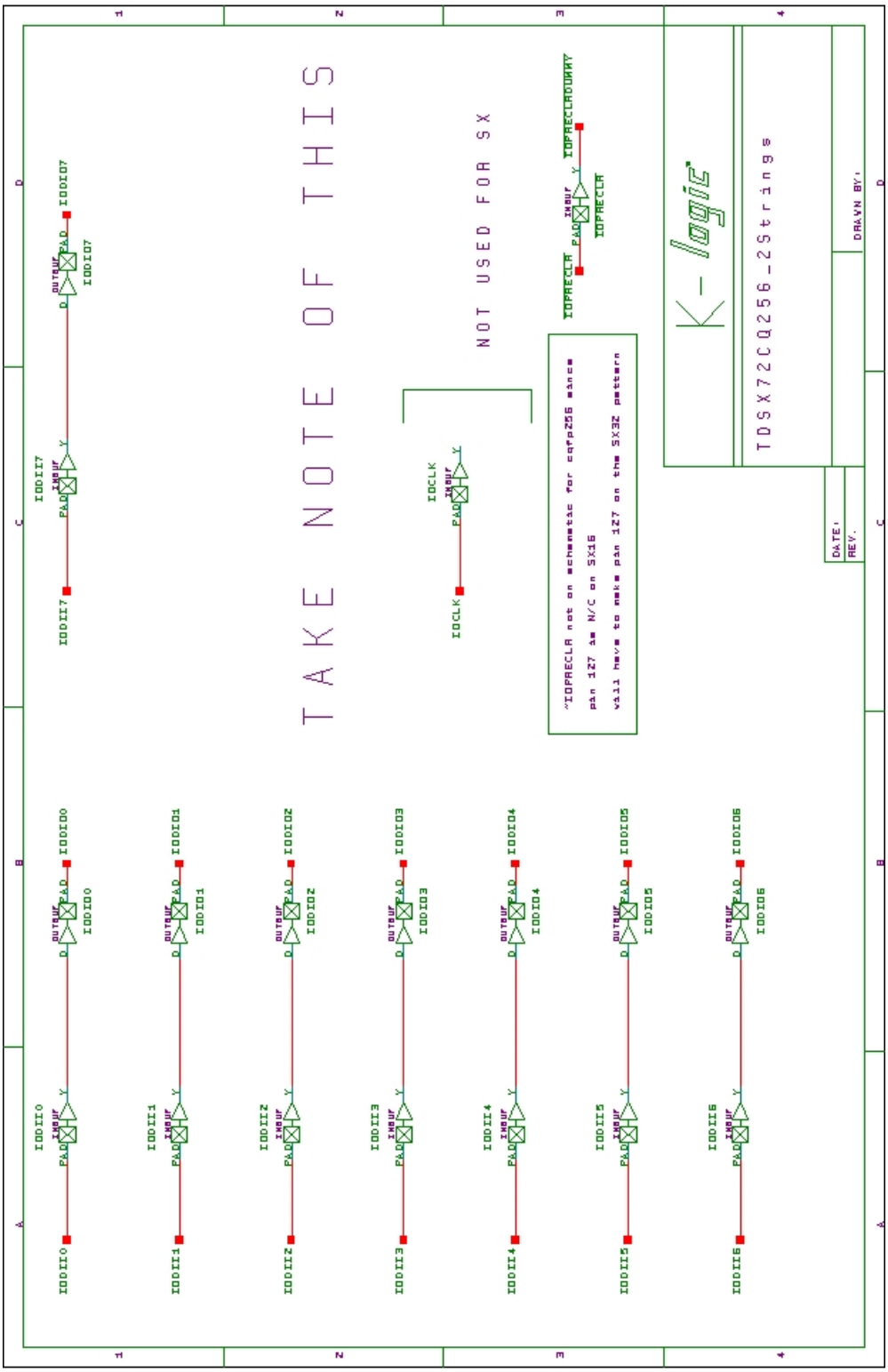

DRC
ANDC
ANDP
DRP
K-logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

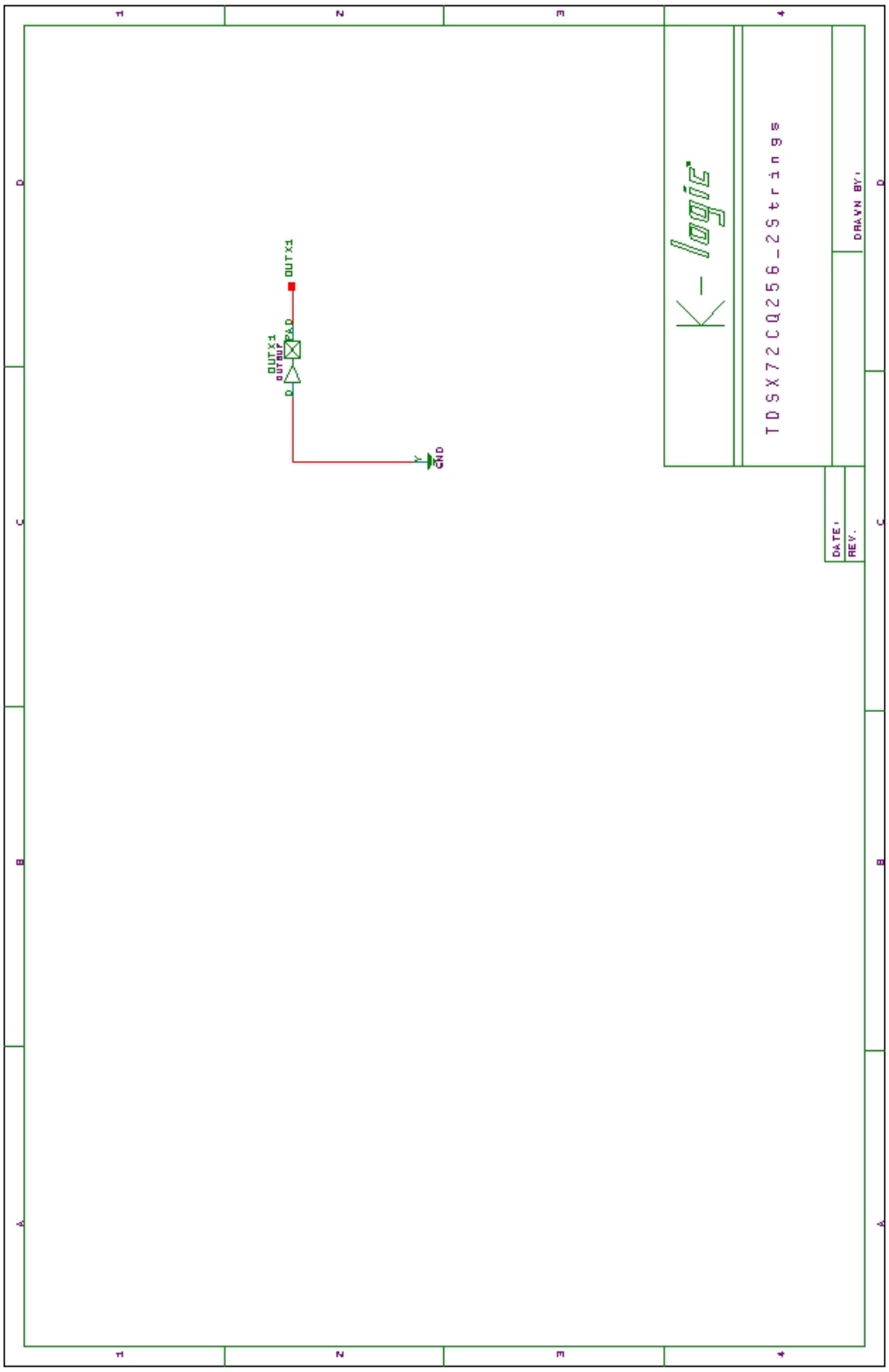

DRC
ANDC
ANDP
DRP
AND4
DFF
RST
CLK
D
Q
BST
CLK
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDF
ORF
OR4
AND4
DFF1S
DFC1S
PRE
CLR
CLK
D
Q
RST
CLK
Logic
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH TMUF
Y FFINH
CLOCKH HCLKBUF
RESETH TMUF
Y TRSTH
DAH
CLOCKH
RESETH


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTRH
ENCNTRH
CNTRLOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256_2Strings
IOPRECLR
IOPRECLRBUFMAY
IOPRECLRBUF
IOCLK
IOCLKBUF
IOOII7
IOOII0
IOOII1
IOOII2
IOOII3
IOOII4
IOOII5
IOOII6
IOOIO7
IOOIO0
IOOIO1
IOOIO2
IOOIO3
IOOIO4
IOOIO5
IOOIO6
DATE:
REV.
DRAWN BY:


OUTX1
OUTBUF
PAD
I
O
Y
GND
TDSX72CQ256_25strings
DRAWN BY:
DATE:
REV.

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