Designing an 8 Port PoE System With PD39100 & PD69108 (802.3af/802.3at Compliant)

APPLICATION NOTE

Introduction

This application note provides detailed information and circuitry design guidelines for implementing an 8-port Power over Ethernet (PoE) system, based on Microsemi's™ PD69108 8-channel PoE manager and PD39100 PoE Controller.

For communicating with the hosting system either an UART or an I^2C interface is optional (not included in this application note).

This document enables designers to integrate PoE capabilities into an Ethernet switch, as specified in IEEE802.3af and IEEE802.3at standards.

PD69108, 8 port PoE manager implements real time functions as specified in IEEE 802.3af and IEEE802.3at standards, including detection, classification, port-status monitoring, and system level activities such as power management and MIB (Management Information Base) support for system management. PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using DC disconnection methods as specified in the standard.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69108 datasheet, catalogue number 06-0057-058
- PD39100 datasheet

Features

- IEEE802.3af-2003 compliant
- IEEE802.3at-2009 compliant, including two-event classification
- Controls up to 8 PoE ports (one PD69108)
- Pre-Standard / Capacitor Detection
- Detection of Cisco devices
- Supports both UART and I2C interfaces to Host CPU
- Backwards compatible with PD69000, PD63000, PD62000 and PDIC66000
- Supports 2 pair RJ
- 16 emergency power banks support using four discrete lines connected directly to PD69108
- Power management for up to 8 ports
- Programmable over-voltage and under-voltage
- 16 predefined power budget control
- Direct LED driving for up to 8 ports (LED 0 to7)
- PoE Max System LED direct driving (LED8)
- Software download via I^2C or UART
- System and port measurements
- Detailed port status
- Thermal protection and monitoring
- Programmable temperature alarm limit
- Forced power for system testing
- System reset
- Port power limit setting
- Port matrix and priority
- Automatic detection of PoE device type
- RoHS compliant

PoE System

The system described here is designed to support a low cost 8-port PoE switch.

The following figure demonstrates a PoE system board which can be easily integrated on top of a switch, providing the capability to add any PoE application while using a daughter board applications (refer to Figure 1).

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

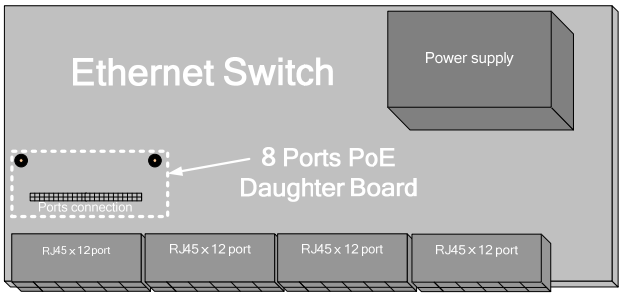


Figure 1: PoE Daughter Board Example

General Description

The circuit includes the following blocks (Figure 2):

- PoE circuit for 8 ports based on one PD69108
- PD39100 Controller circuit, used to initialize, control and monitor PD69108 via an internal ESPI (non isolated) bus.
- Note: In this application note PoE controller is NOT designed to communicate with Host CPU.

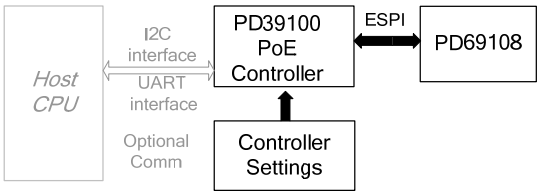


Figure 2: 8-port Configuration

General Circuit Description

The 8-port configuration for the PoE system shown in Figure 2, comprises one PoE managers circuits (PD69108) functioning as a slave with a PoE controller (PD39100).

PoE controller utilizes ESPI bus to control PD69108. PoE operations are automatically performed by PoE manager circuits, while PoE controller performs power management and other tasks. Operation mode and power management are set through R-mode (see PD39100 datasheet).

Communication Interfaces

Communication between Host CPU and local PoE controller is optional (not included in this application note) and may be based on UART or I^2C interface. For more information, refer to *Serial Communication Protocol User Guide, catalogue number 06-0032-056*.

ESPI Bus

The Enhanced Serial Peripheral Interface (ESPI) bus used for internal communication includes the following lines:

- MOSI (Master Out/Slave In) allows PoE Controller to communicate with PD69108s.
- MISO (Master In/Slave Out) allows PD69108s to communicate with PoE controller.
- SCK is a serial clock generated by the controller.
- CS (Chip Select) is utilized by PoE controller to transmit data to all PD69108s simultaneously, while only the chosen PoE manager responds back.

Controls Signals

- **Hardware Version control** – used for configuring PD39100 to different operation modes (see PD39100 datasheet).
- **Power Management control** - PD69108 PG 0 to 3 Input Signals – used for configuring Total PoE Power Budget

Indications

- LED 0 to 7 – Direct LED drive is included per port, to indicate port PoE status (see PD39100 datasheet)
- LED 8 – Direct LED drive for System Power status indication is included, to indicate PoE power status (see PD39100 datasheet)

Communication Flow (Optional)

- Host CPU may optionally use a Serial Communication protocol to PoE controller (PD39100) – Not Included in this application note.
- PoE Controller converts Serial Communication Protocol to ESPI Communication and sends it via isolated ESPI lines to PD69108.

Main Supply

The PoE system operates within a range of 44 to 57 V_{DC} (802.3at port's range is 50 to 57 V_{DC}). To comply with UL SELV regulations, maximum output voltage **should not** exceed 60V_{DC}.

Grounds

Several grounds are used in the system.

- PoE Domain Analog
- PoE Domain Digital
- Chassis
- Host Domain Floating

Digital and analog grounds are electrically same ground. However, to reduce noise coupling, grounds are

physically separated and connected only at a single point.

Chassis ground is connected to switch's chassis ground. This ground plane should be 1500 V_{rms} isolated from the PoE circuitry.

PoE controller relates to Host domain floating ground which is isolated for PoE domain grounds. It contains a small local ground for analog signals (A_cpu) that is connected using a single connection to F_cpu ground (which is the host domain floating ground) to protect sensitive signals from noise.

Grounding is further detailed in *Application Note 186, catalogue number 06-0081-080 for Layout Design Guidelines*.

5 V_{DC} and 3.3 V_{DC} Regulators

PD69108 has a $5V_{DC}$ regulator and a $3.3V_{DC}$ regulator providing up to 6mA each. This current is used for powering other external components in the PoE domain; those components must also be isolated by $1500V_{rms}$ from switch circuitry.

An external boost transistor (Q1) and additional 12 serial resistors (R1 to R12) are included in this application.

It is used to increase $5V_{DC}$ regulated output current.

This 5V Regulation circuitry is used to provide a total of 60mA to PoE controller and Direct LED Drivers.

Note that the 12 resistors (R1 to R12, each of 7.5KΩ / 1206) – are designed to dissipate about 2W. These resistors should be located (spread) over PCB, placed away from Q1 and from other high thermal sources such as PD69108 and 360mHom sense resistors, as illustrated in Layout Design Guidelines.

Additional Circuit Description

PoE Controller Circuitry

1.2 Mb/s ESPI communication interface used between PD39100 and PD69108.

UART Debug Signals are used – See "Tx_Debug" and "Rx_Debug" Signals

PoE controller runs at 8MHz, facilitated by an external Crystal XT1.

For its operation, PoE controller requires stable, filtered power that comes from the host (3_3V_Aux and 3_3V_cpu); hence, a number of components are included in the design:

- **R38, C17, C18, C19, C30**: are used for filtering these power sources.
- **HW_VER (Hardware Version)**: This analog input signal provides hardware configuration indication to PoE Controller. This line is factory controlled and should not be changed.

LED Drive Support

Direct LED drive is included to support PoE port status indication (see LED0 to LED7 signals)

Additional Direct LED drive is included for System Power status indication (see LED8 system signal in PD39100 datasheet)

PoE Manager Circuitry

PD69108 performs a variety of internal operations and PoE functions, requiring a minimum of external components.

PD69108 Front End Circuitry includes several external components, for handling up to 8 PoE ports.

Reference Current Source

Reference for internal voltages within PD69108 is set by a precision resistor (R46).

Sense Resistors

A 360 mΩ, ±1% sense resistor is connected to each PORT_SENSE pin (R180-R187). This resistor is used to measure port current.

Recommended trace resistance of each sense resistor should be close to 12mΩ. For more information, refer to *Application Note 186, catalogue number 06-0081-080 for Layout Design Guidelines*.

Front End and Protection

Each output port includes internal protection circuitry against external discharges that may damage the PD69108.

When any IC experiences input voltage above its absolute maximum rating, it is exposed to damage. Since the PoE manager is connected to a high current source, best design practice is to use a protection fuse (See F1 to F8) to avoid high current path during PSU over voltage faults. F1 to F8 are also utilized as a current limiting device, operating as specified in IEC 60950-1:2001.

Note: According to IEC 60950-1:2001 these fuses may be avoided in PoE systems with power supply of less than 100W.

Serial Communication Host – Controller (Optional)

PoE controller can communicate with hosting system using UART or I^2C communication. UART or I^2C communication between Host CPU and PoE controller is managed by setting PoE controller's address. This is done by setting Pin #16, as specified in PD39100 datasheet.

This Application Note includes non-isolated UART Debug Communication option only.

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

UART Debug Port

An Rx Debug and Tx Debug signals are connected to pins #9 and #10 of PoE controller, for optional system debug. It is recommended to prepare simple test points for those signals as illustrated in this AN.

Power Management

Total power consumption of all 8 ports is being controlled and monitored through PD69108 and PD39100.

Default Power limits are determined according to PD69108's Power Good pins (Digital Input pins "PG 0 to 3").

Users can configure the total maximum power available for PoE Ports – by connecting each of PG Input pins to DGND or DVDD

"0" – Connected to DGND

"1" – Connected to DVDD

This Application Note illustrates a scenario in which all PG pins are grounded (See R81, R80, R85, R84).

In this specific case, when all PG pins are grounded,– max. system power would be set to 270W.

See table below:

16 predefined power levels are listed below:

Total Power level	PG[3:0]
270W	0000
40W	0001
55W	0010
70W	0011
85W	0100
100W	0101
115W	0110
130W	0111
145W	1000
160W	1001
175W	1010
190W	1011
205W	1100
220W	1101
235W	1110
250W	1111

Ground Interface Connection (AGND)

Power supplies ground connector enables for the current a path back to the power supply. Ground connection should be capable of carrying all strings currents back to power supplies.

Thermal Design

Design for 802.3at PoE standard should take into account power dissipation of PoE manager and of associated circuitry, and switch's maximal ambient operating temperature. Adequate ventilation and airflow should be part of the design to avoid thermal over-stress on the following issues.

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

Ambient Temperature

Application's thermal design should take into account the temperature derived from switch's power dissipation and from PoE daughter board powered at maximum load.

PD69108

PoE design should ensure PD69108's maximal operating junction temperature (150° C) **is not** exceeded under worst case conditions. Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at 802.3at power and all other unit functions fully operational. *PD69108 datasheet, catalogue number 06-0057-058* contains additional thermal characteristics details.

PD39100

Layout considerations should ensure that:

- PD39100 is placed away from potential high temperature spots.
- Maximal case temperature **does not** exceed 85°C under worst case conditions.

Sense Resistors

Each port's front-end circuit has a single sense resistor. Resistor's value should be 360mΩ and should dissipate about 0.19W at 720mA (802.3at maximum load) and 44 mW at 350mA (802.3af maximum load). Resistors traces' resistance needs to be controlled to achieve maximum current accuracy. Heat generated from these resistors contributes to a higher ambient temperature near PD69108. For 802.3at ports, use these sense resistors types:

Description	SIZE	Mnf.	MAN. PART #
0.360R 1% 0.5 W 200 PPM	1210	Rohm	MCR25JZHFLR360

Note Sense resistor's temperature coefficient of resistance (ppm) should be less than or equal to $\pm 200\ [10^{-6}/^{\circ}C]$.

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

Schematics

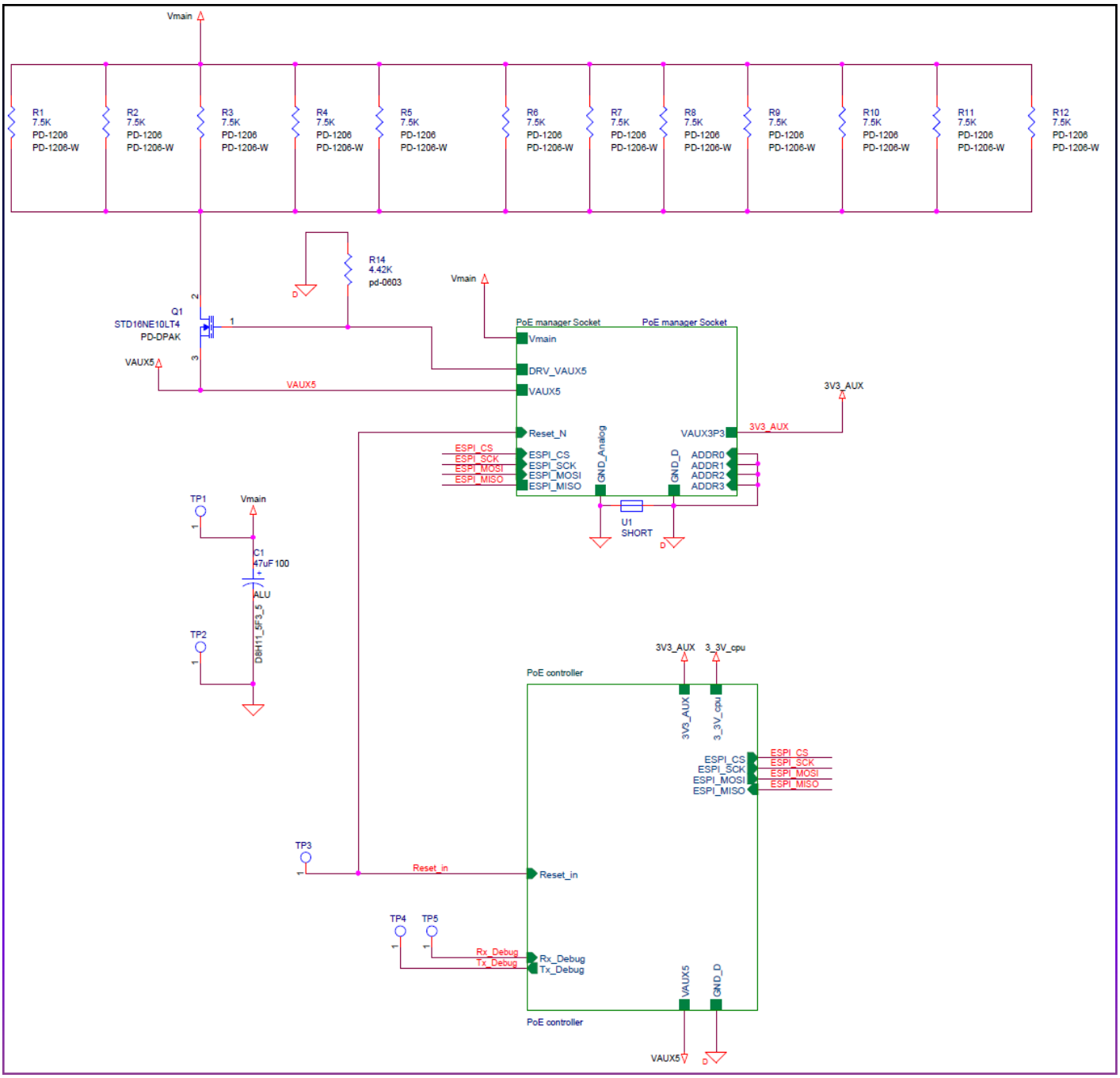


Figure 3: Top Level Blocks

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

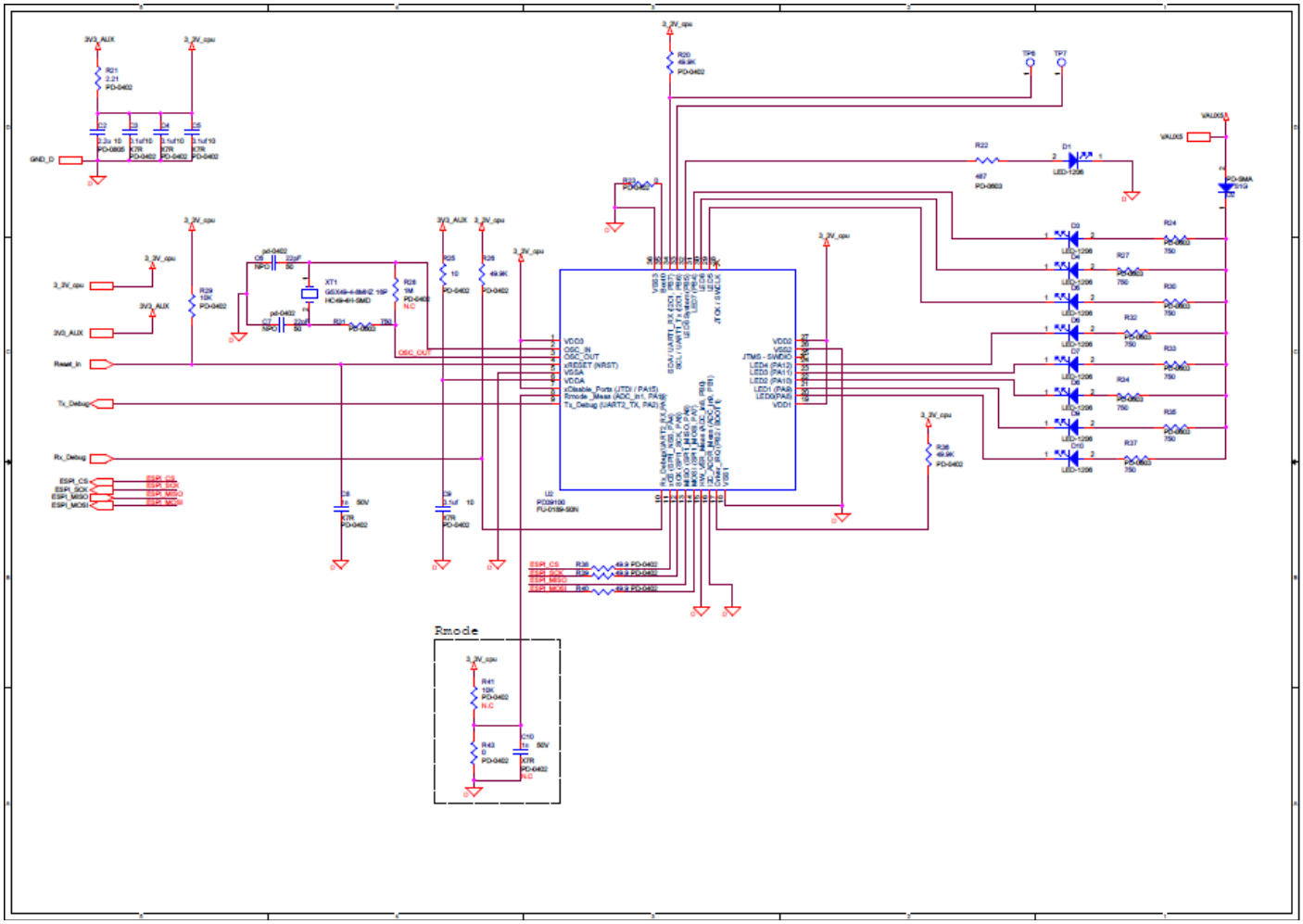
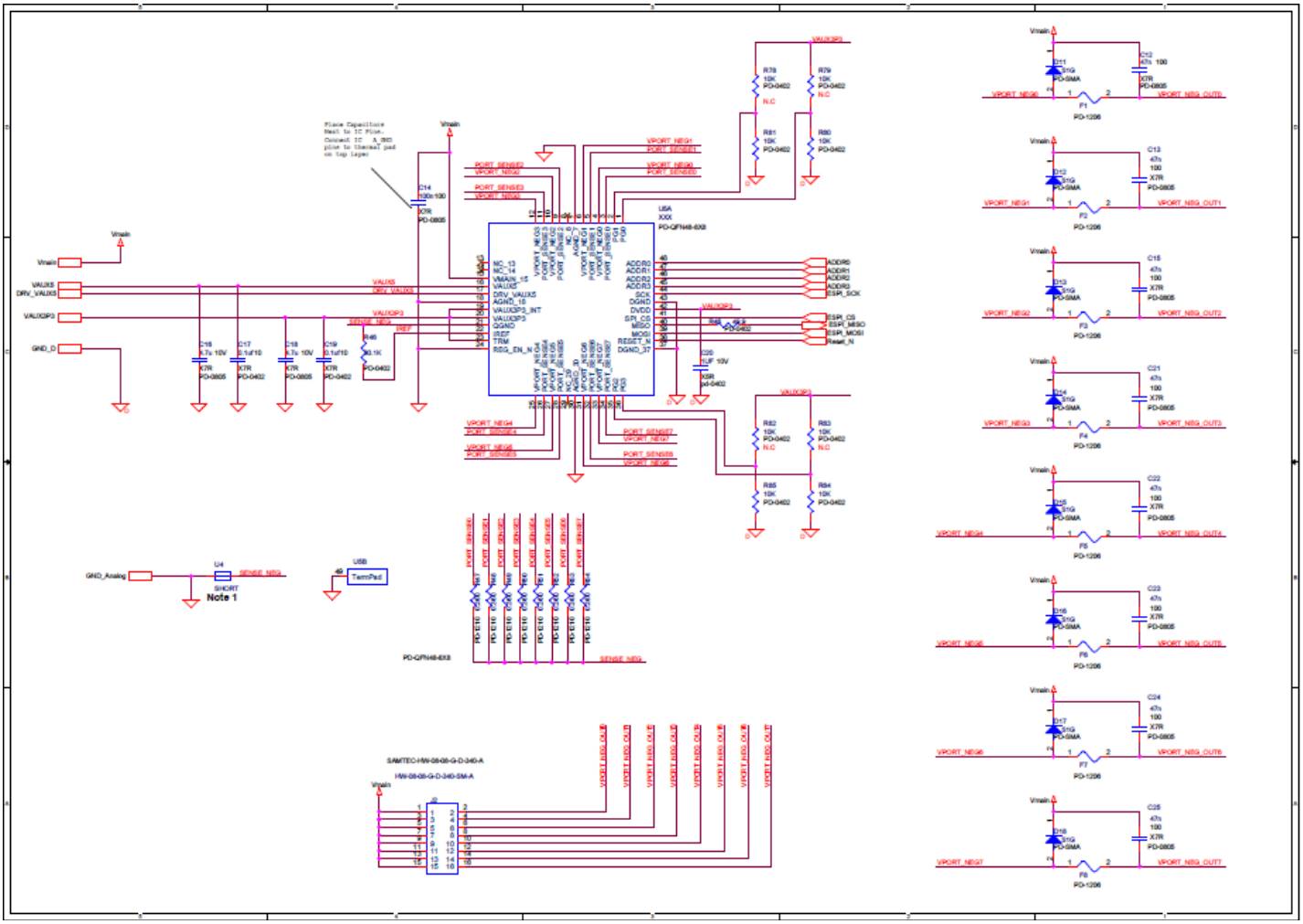


Figure 4: PD39100 PoE Controller Circuitry

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570



PD69108 Circuitry for PoE Manager

Microsemi
Analog Mixed Signal Group
11861 Western Avenue, Garden Grove, CA. 92841, 714-898-8121, Fax: 714-893-2570

Bill of Materials

Reference	Quantity	Part / Value	PCB Footprint	Notes / Remarks
C1	1	47µF / 100v	D8H11_5F3_5	Main PoE Filter Cap
C2	1	2.2µ	0805	
C3,C4,C5,C9,C17,C19	6	0.1µf	0402	
C6,C7	2	22pF	0402	
C8	1	1n	0402	
C12,C13,C15,C21,C22,C23, C24,C25	8	47n	0805	
C14	1	100n	0805	
C16,C18	2	4.7µ	0805	
C20	1	1UF	0402	
D1,D3,D4,D5,D6,D7,D8,D9, D10	9	11-21 SYGC/S530-E1/TR8	LED-1206	3.5mA Single Color LED **See Note 2**
D2,D11,D12,D13,D14,D15, D16,D17,D18	9	S1G	SMA	
F1,F2,F3,F4,F5,F6,F7,F8	8	F1206B1R50FW-TR	1206	**See Note 1**
J2 (Optional)	1	HW-08-08-G-D-340-SM-A	SAMTEC-HW-08-08-G-D-340-A	Optional – PoE Terminals Connection to Mother Board
Q1	1	STD16NE10LT4	DPAK	5V Regulator MOSFET Designed to support up to 55mA
R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12 R13,R15, R16,R17,R18	17	7.5K	1206	R1 to R12 – Power Dissipation Resistors Refer to 5V Regulation
R14	1	4.42K	0603	
R19	1	5.36K	1206	
R20,R26,R36	3	49.9K	0402	
R21	1	2.21	0402	
R22	1	487	0603	
R23,R43	2	0	0402	Soft Connection to DGND
R24,R27,R30,R31,R32,R33, R34,R35,R37	9	750	0603	Serial LED Resistors – Designed for 3.5mA **See Note 2**
R25	1	10	0402	
R29,R80,R81,R84,R85	5	10K	0402	
R38,R39,R40,R45	4	49.9	0402	
R46	1	30.1K	0402	
R47,R48,R49,R50,R51,R52, R53,R54	8	0.36	1210	
TP1,TP2,TP3,TP4,TP5,TP6, TP7	7	TP60	TP60	
U2	1	PD39100	QFN36-6X6	CPU - PoE Controller
U5	1	PD69108	QFN48-8X8	MSCC – 8 Ports PoE Manager
XT1	1	GSX49-4-8MHZ 16P	HC49-4H-SMD	CPU 8MHz Clock Osc.

Note 1: In PoE systems with power supply of Less than 100W these fuses may be avoided

Note 2: Avoide using LED current higher than 3.5mA. In case a higher LED current is needed, contact MSCC sales support.

APPLICATION NOTE

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 01 Dec 2010	-	Initial Release – Preliminary version

For support contact: sales_AMSG@microsemi.com

Visit our web site at: www.microsemi.com

Catalog Number: PD39100_AN_199