Designing a PD69108/PD69104 48-port PoE System 802.3af/802.3at Compliant

APPLICATION NOTE

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's™ PD69108 8-channel PoE manager and PD69100 PoE Controller. UART interface or I^2C interface is available for communication with the hosting system.

This document enables designers to integrate PoE capabilities, as specified in IEEE802.3af and IEEE802.3at standards, into an Ethernet switch.

PD69108 8 port PoE manager implements real time functions as specified in IEEE 802.3af and IEEE802.3at standards, including detection, classification, port-status monitoring, and system level activities such as power management and MIB (Management Information Base) support for system management. The PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using DC disconnection methods, as specified in the standards.

This application note should be used in conjunction with *Application Note 186, Catalogue Number 06-0081-080 for Layout Design Guidelines*. For easy design and development, an Evaluation board (P/N PD-IM-7548) can be ordered.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69108 datasheet, catalogue number 06-0057-058
- PD69104 datasheet, catalogue number 06-0131-058
- PD69100 datasheet, catalogue number 06-0076-058
- Application Note 186, catalogue number 06-0081-080 for layout design guidelines.
- PD-IM-7548 Evaluation Board user guide catalogue number 06-0047-056
- Serial Communication Protocol user guide catalogue number 06-0032-056
- Technical Note 134, Emergency Power Management catalogue number 06-0014-081

Features

- IEEE 802.3af-2003 standard compliant
- IEEE802.3at-2009 standard compliant
- Configurable AT/AF modes
- Configurable standard and legacy detection mode
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 – 57V_{DC})
- Two-event classification
- Voltage monitoring/protection
- Low power dissipation (0.36Ω sense resistor)
- Low R_{ds} on internal MOSFET
- Internal power on reset
- Includes Reset input from hosting system
- Four direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- On-chip thermal protection
- Built in 3.3V_{DC} and 5V_{DC} regulators
- Emergency power management supporting sixteen configurable power banks
- Can be cascaded to up to 12 PoE devices (96 ports)
- Supports 4 pair connection
- Wide temperature range: -40° to +85°C
- RoHS compliant

Integration

The system described is destined for a 48-port switch. Any combination between PD69108 and PD69104 can be implemented with up to 12 chips. Same design can be applied to 1 to 12 PoE managers controlling four/eight ports each (from 4 ports to 96 ports in multiples of 4/8). Designs contain up to 8 PoE ports can use PD39100 PoE Controller (instead of PD69100) for cost reduction (for 8 port design using PD39100 refer to Application note 199, catalog number PD39100_AN_199).

PoE system board can be easily integrated on top of a switch, providing the capability to add any PoE application while using different daughter applications (refer to Figure 1).

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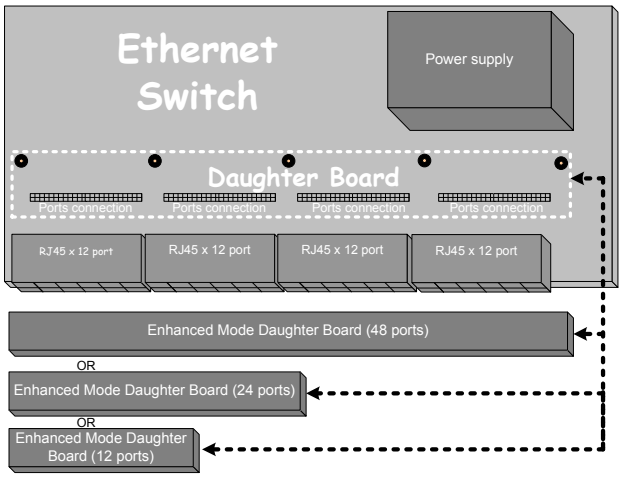

Figure 1: PoE Daughter Board Integration

Overall Description

The circuit includes the following blocks (Figure 2):

- PoE circuit for 48 ports based on six PD69108s.
- Controller circuit, used to initialize, control and monitor each of the PD69108s via an internal ESPI isolated bus. The PoE Controller communicates with the Host CPU via a non-isolated UART or an I^2C interface.
- Isolation Circuit for ESPI bus.

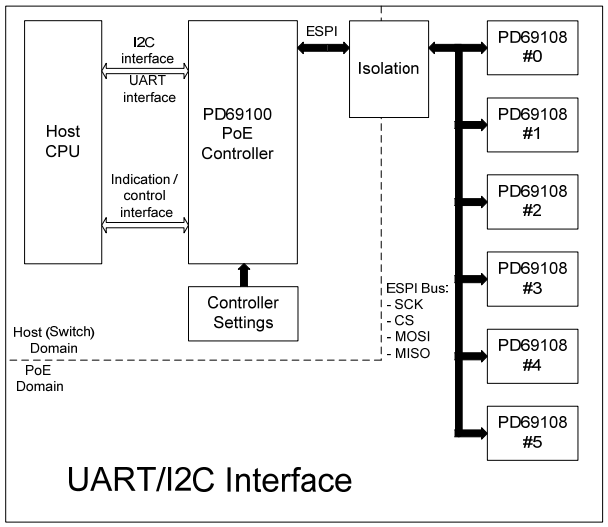

Figure 2: 48-port Configuration

For 96 ports system detailed information please contact Microsemi.

APPLICATION NOTE

General Circuit Description

The 48-port configuration for a PoE system shown in Figure 2, comprises six PoE managers circuits (PD69108) functioning as slaves to a PoE Controller (PD69100). The PoE Controller utilizes the ESPI bus to control PD69108s. PoE operations are automatically performed by PoE manager circuits, while PoE Controller performs power management and other tasks. A configuration with 96 ports is made up of 12 PoE managers circuits (PD69108) functioning as slaves to a PoE Controller (PD69100).

Communication Interfaces

Communication between Host CPU and local PoE Controller is performed via an UART interface or an I^2C interface. For more information, refer to the *Serial Communication Protocol User Guide, catalogue number 06-0032-056*.

ESPI Bus

The Enhanced Serial Peripheral Interface (ESPI) bus, used for internal communication, includes the following lines:

- MOSI (Master Out/Slave In) provides communication from PoE Controller to PD69108s.
- MISO (Master In/Slave Out) provides communication from PD69108s to PoE Controller.
- SCK is the serial clock generated by the Controller.
- CS (Chip Select) is utilized by PoE Controller to transmit data simultaneously to all PD69108s, while only chosen PoE manager responds back.

Note: PoE Managers ESPI addresses must be set in incremental order for proper operation of the system and start from 0.

Control

Refer to Figure 3.

- An **xReset_IN** control signal driven by Host CPU is used to reset PoE system.
- An **xDisable_ports** control signal driven by Host CPU is used to disable all PoE ports at once.

Indications

The PoE Controller produces an **xSystem_ok** signal, indicates that the input main voltage is within range, **xInt_out** interrupt signal, utilized to indicate PoE events and an **I2C_Message_Ready** that indicates signals message is ready to be read by Host.

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Communication Flow

Host CPU issues commands, utilizing a dedicated Serial Communication Protocol to the PoE Controller.

PoE Controller converts Serial Communication Protocol to ESPI Communication and sends it via isolated ESPI lines to appropriate PD69108. This isolation is a basic requirement of IEEE PoE standards.

Main Supply

PoE system operates within a range of 44 to 57V_{DC} (802.3at port's range is 50 to 57V_{DC}). To comply with UL SELV regulations, maximum output voltage **should not** exceed 60V_{DC}.

Grounds

Several grounds are utilized in the system.

- PoE Domain Analog
- PoE Domain Digital
- Chassis
- Host Domain Floating

Digital and analog grounds are electrically same ground, however, to reduce noise coupling, grounds are physically separated and connected only at a single point.

Chassis ground is connected to switch's chassis ground. This ground plane should be 1500V_{rms} isolated from PoE circuitry.

PoE controller relates to Host domain floating ground which is isolated for PoE domain grounds. It contains a small local ground for analog signals (A_cpu) that is connected with a single connection to F_cpu ground (which is the Host domain floating ground) to protect sensitive signals from noise.

Grounding is further detailed in *Application Note 186, catalogue number 06-0081-080 for Layout Design Guidelines*.

5V_{DC} and 3.3 V_{DC} Regulators

Each PD69108 has a 5V_{DC} and a 3.3V_{DC} regulators providing up to 6mA each. These currents are utilized for powering components in the PoE domain; those components must also be isolated from the switch circuitry by 1500V_{rms}.

An external boost transistor can be added to the 5V_{DC} regulator's output to increase the current (see Figure 9). The transistor can provide a total of 30mA to the PoE Controller and to the isolation circuits. This total current is the sum of the 5V and 3.3V currents.

Detailed Circuit Description

Block Diagram/Main

Refer to **Error! Reference source not found.**.

Communication Interfaces/Isolation

There are two communication interfaces in this circuitry:

- An interface between the Ethernet switch and the PoE Controller; this interface is an I^2C or an UART interface and does not require isolation.
- An interface between PoE Controller and PoE managers with 1500V_{rms} isolation; this interface is a standard ESPI.

Isolation circuit comprises of U9 (ADUM1411 by Analog Devices) and two filter capacitors; C5 and C6. Note that each side of the circuitry is fed by a separate power supply.

Control and Indication Signals

Control/Indication signals are of the single H/W lines type running between Host CPU and PoE Controller (Refer to Figure 3).

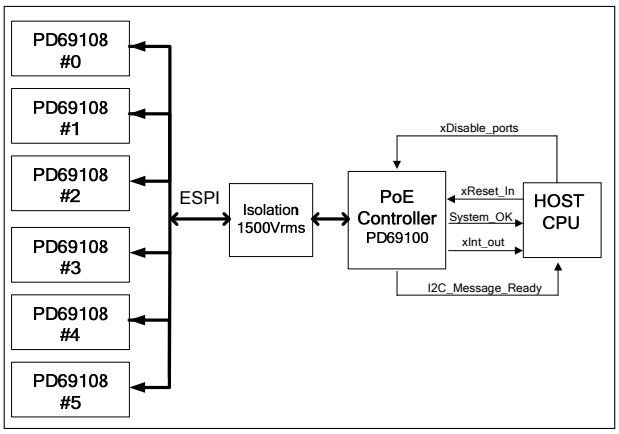

Figure 3: Control and Indication Signals

Control Signals

There are two control lines driven by Host CPU to PoE Controller:

- **xDisable_ports**: Disables all PoE ports. When PoE Controller detects low level voltage at pin #29, it sends a disable command via ESPI to PoE manager's ports.
- **xReset_In:** Resets PoE Controller and all PoE managers. When PoE Controller detects low level voltage at pin #4, it enters Reset mode and all its output pins switch to Tri-state mode. When xReset_In line returns to 'high', PoE Controller initializes

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and sends RESET command to PoE managers via the ESPI bus. xReset_In is also used by the PoE Controller to reset itself, and therefore when used, it must be connected on host side to open drain output.

Indication Signals

Three signals are utilized to provide the Host CPU with the following event indications.

- **System_OK**: Indicates that main voltage is within desired range.
- **xint_out:** Interrupt signal coming from PoE Controller; indicates events such as Port On, Port Off, Port Fault, PoE manager Fault, Voltage out of range etc.
- **I2C_Message_Ready:** Indicates I^2C message is ready to be read by Host.

For full list of interrupt events, refer to *PD63000 & PD69000/G Serial Communication Protocol User Guide, catalogue number 06-0032-056*.

PoE Controller Circuitry

Refer to Figure 7.

PoE Controller features 1.2Mb/s ESPI for each of the PoE managers, and a communication interface with Host CPU via UART or I^2C protocol.

UART or I^2C communication between Host CPU and PoE Controller are managed by setting PoE Controller's address, pin #16 (I^2C_ADDR). For UART and I^2C communication address table, refer to Serial Communication Host-Controller on page 5.

The PoE Controller runs at 8MHz, facilitated by an external Crystal XT1.

Note: XT1 should be Crystal type oscillator only.

Supply: PoE Controller requires stable, filtered power for its operation coming from the Host (3_3V_iso); hence, a number of components are included in the design:

- **R6, C7, C8, C9, C10**: Used for filtering of 3_3V_iso.
- **R12 and C11**: Used for filtering analog voltage VDDA.
- **R15:** Crystal oscillator series resistor – should be 5 to 6 times the crystal Rs (Rs is defined in the crystal oscillator datasheet)

SELF_RESET: As required by the application, the PoE Controller can reset itself. This reset can also be performed by an external source utilizing the **xReset_In** signal (usually by Host Controller). If this option is used PoE Controller must be connected to open drain output.

HW_VER (Hardware Version): This input line provides hardware configuration indication to PoE Controller. This line is factory controlled and cannot be changed.

LED Support

Refer to Figure 4.

LED support for port status indication is accomplished by utilizing the **ESPI bus** (SCK and MOSI), **xLED_CS, xLED_OE**, and **xLED_Latch** signals. Bus behavior is 100kb/s synchronous serial communication (clock, data) in one direction (write only) that transmits the status of up to 96 ports. Packet is transmitted with Start header and End header bytes. For more details, refer to *Technical Note-118, catalogue number 06-0008-081*.

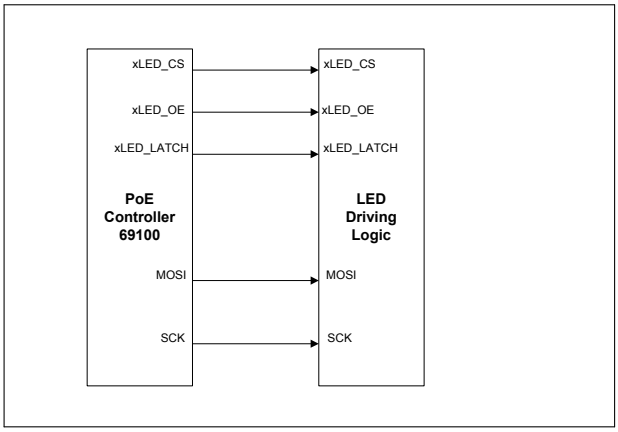

Figure 4: SPI Bus and LED Support

Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended each power supply will be capable of generating a logic signal, indicating its operate/fail status. Refer to Figure 5.

The used pins are as follows:

PD69108 PIN NUMBER	SIGNAL	REMARKS
#1	PG0	Power Good 0
#2	PG1	Power Good 1
#35	PG2	Power Good 2
#36	PG3	Power Good 3

PoE circuit allocates power to the system in 16 power levels (power banks) programmed by users. Power bank values are based on each supply's available power and on the state of the logic signals PG[0..3] coming from power supplies. If PG pin is not used, the pin must be connected to GND. Figure 5 illustrates the connections between power supplies' logic signals and PoE Manager.

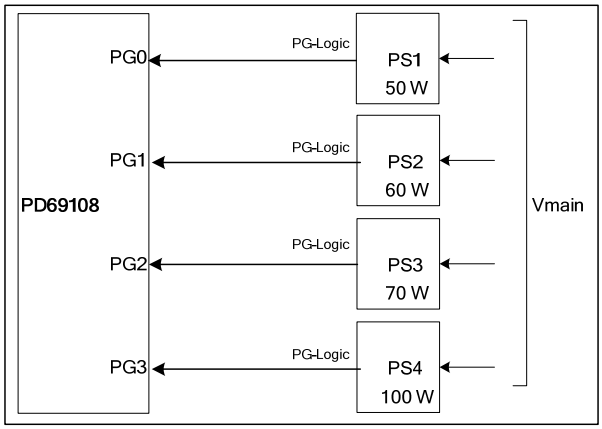

Figure 5: Power Good

For isolation requirements destined for Emergency Power Management, refer to *Technical Note-134, catalogue number 06-0014-081*, section "Isolation Requirements".

PoE Manager Circuitry

PD69108 performs a variety of internal operations and PoE functions, requiring a minimum of external components. Each PD69108 handles up to 8 ports. Figure 8: shows PoE Manager #0 with its related components for an 8-port configuration. What's being presented in Figure 8: is duplicated 6 times for 48 ports.

Reference Current Source

Reference for internal voltages within PD69108 is set by a precision resistor (R29).

Sense Resistors

A 360mΩ, 1% sense resistor is connected to each PORT_SENSE pin (R30-R37). This resistor is utilized to measure port current.

Recommended trace resistance of each sense resistor should be close to 12mΩ. For more information, refer to *Application Note-186, catalogue number 06-0081-080 for Layout Design Guidelines*.

Front End and Protection

Each output port includes internal protection circuitry against external discharges that may damage PD69108.

Fuses per port are not required for use in circuits with total power level of up to 3kW. That's because PD69108 is UL 2367 (category QVRQ2) recognized component and fulfills limited power source (LPS) requirements of latest editions of IEC60950-1 and EN60950-1.

Other components are used in port #0 for the following purposes:

- D4 (port #0) may be required for protection against damaging potentials, depending on layout and construction of the PoE system.
- C18 forms a noise suppression component.
- D3 presents a non-valid PD detection signature for a reversed voltage PSE to PSE connection. It is mandatory per IEEE802.3at-2009 standard.

Serial Communication Host-Controller

PoE Controller can communicate with the hosting system using UART or I^2C communication. UART or I^2C communication between Host CPU and PoE Controller is managed by setting the address of PoE Controller. This is done by selecting a value for R24. This resistor sets the analog level into pin #16 (I2C_ADDR), as specified in the following table.

I^2C Address	Address (hex)	R24 (ohms)	I^2C Address	Address (hex)	R24 (ohms)
#0	UART	NA	#8	0x20	8870
#1	0x4	97600	#9	0x24	6810
#2	0x8	53600	#10	0x28	5230
#3	0xC	35700	#11	0x2C	3920
#4	0x10	25500	#12	0x30	2800
#5	0x14	19100	#13	0x34	1870
#6	0x18	14700	#14	0x38	1020
#7	0x1C	11300	#15	0x3C	324

A weak pull up resistor is recommended on pins 33 and 34.

UART

An Rx signal should be connected to pin #34 of PoE Controller.

A Tx signal should be connected to pin #33 of PoE Controller.

I^2C

An SDA signal should be connected to pin #34 of PoE Controller.

An SCL signal should be connected to pin #33 of PoE Controller.

Ground Interface Connection (AGND)

Power supplies ground connector enables the a current path back to power supply. Ground connection should be capable of carrying all strings current back to power supplies.

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Four Pair Connectivity

Designing a PoE port delivering power over RJ45 four pairs of wires is quite easy by utilizing PD69108/4. Just connect any two ports of the PD69108/4 to a single RJ45 connector and configure the PD69100 accordingly. The two ports utilized for the four pair output terminal can be taken from the same PD69108/4 or from any two PD69108/4 ICs. PD69100 configuration process is further explained in the *Serial Communication Protocol User Guide, catalogue number 06-0032-056*.

Thermal Design

The design for 802.3at PoE standard should take into account power dissipation of PoE manager and associated circuitry and the maximum ambient operating temperature of the switch. Adequate ventilation and airflow should be part of the design to avoid thermal over-stress on the following issues.

Ambient Temperature

Application's thermal design should take into account the temperature derived from Switch's power dissipation and from PoE daughter board powered at maximum load.

PD69108

PoE design should ensure that PD69108's maximum operating junction temperature (150°C) **is not** exceeded under worst case conditions. Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at 802.3at power, and all other unit functions fully operational. *PD69108 datasheet, catalogue number 06-0057-058* contains additional thermal characteristics details.

PD69100

Layout considerations should ensure that:

- PD69100 is placed away from potential high temperature spots.
- Maximum case temperature **does not** exceed 85°C under worst case conditions.
- PD69100 thermal pad should not be connected to the PD69100 analog ground plan.

Sense Resistors

Each port's front-end circuit has a single sense resistor. Resistor's value should be 360mΩ and should dissipate about 0.19W at 720mA (802.3at maximum load) and 44mW at 350mA (802.3af maximum load). The resistors traces' resistance needs to be controlled to achieve maximum current accuracy. Heat generated from these resistors contributes to a higher ambient temperature near PD69108. For 802.3at ports, use these sense resistors types:

Description	SIZE	Mnf.	MAN. PART #
0.360R 1% 0.5 W 200 PPM	1210	Rohm	MCR25JZHFLR360

Note Sense resistor's temperature coefficient of resistance (ppm) must be less than or equal to ± 200 $[10^{-6}/^{\circ}C]$.

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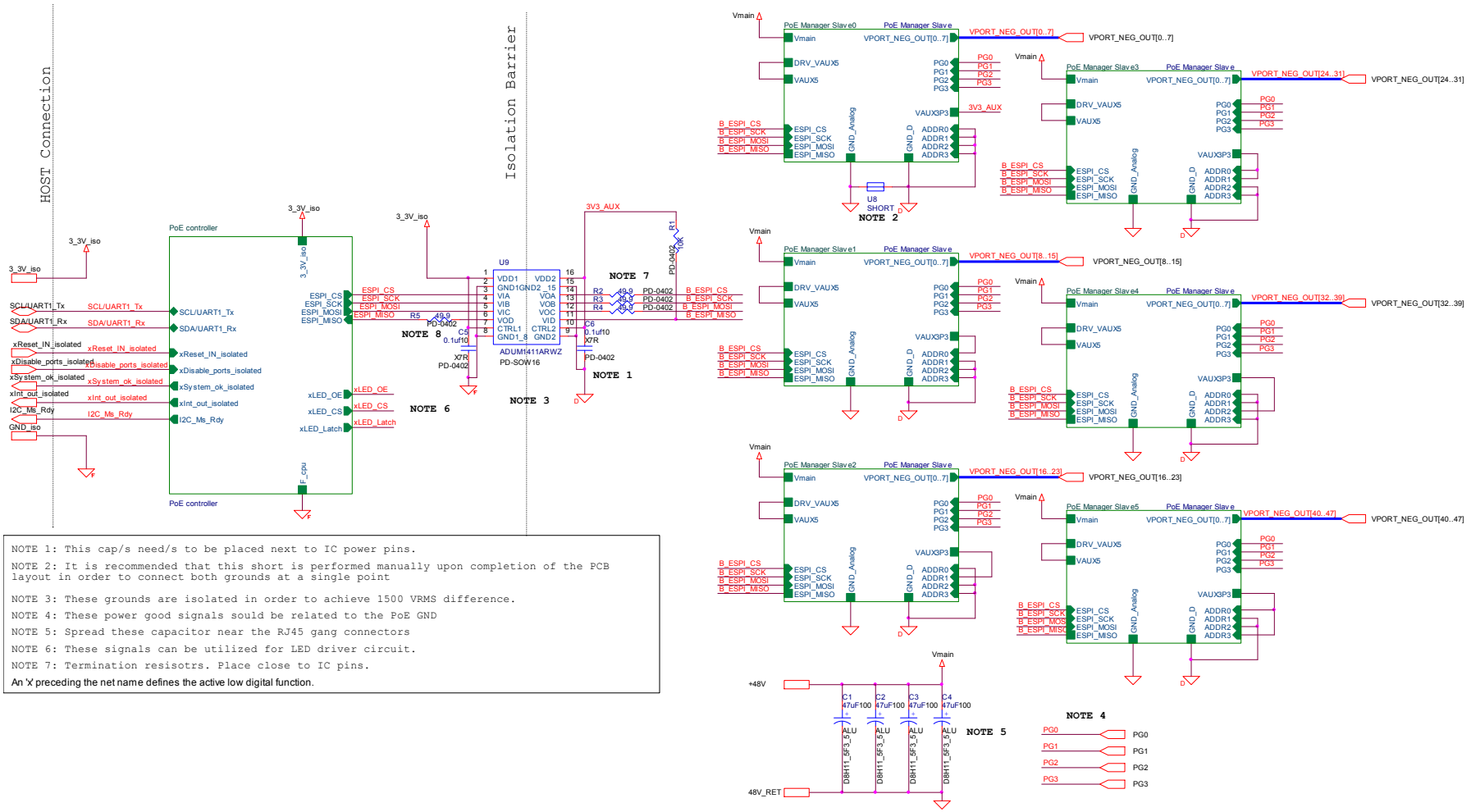

Figure 6: Block Diagram/Main for 48-port System

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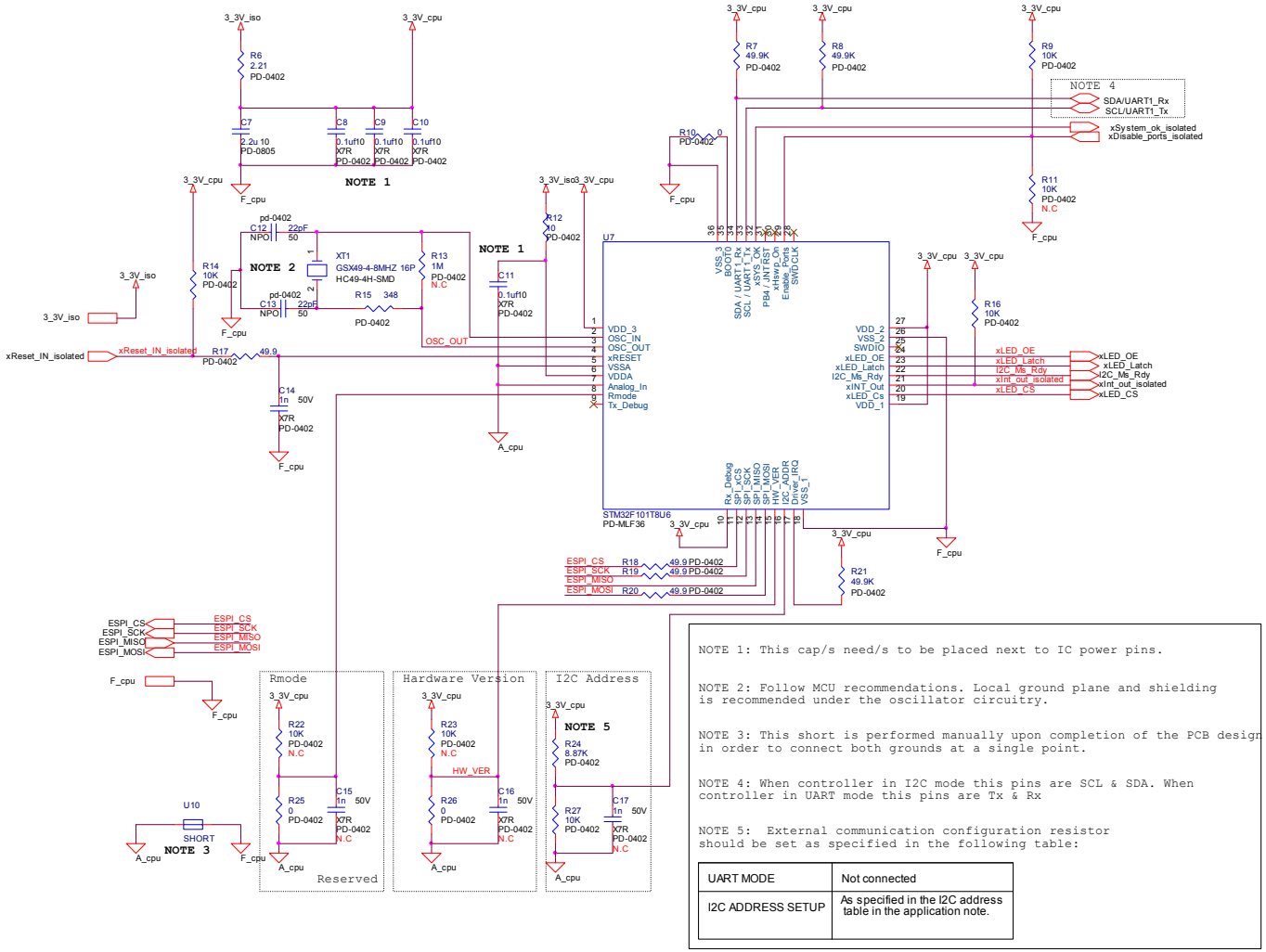

Figure 7: PD69100 PoE Controller Circuitry

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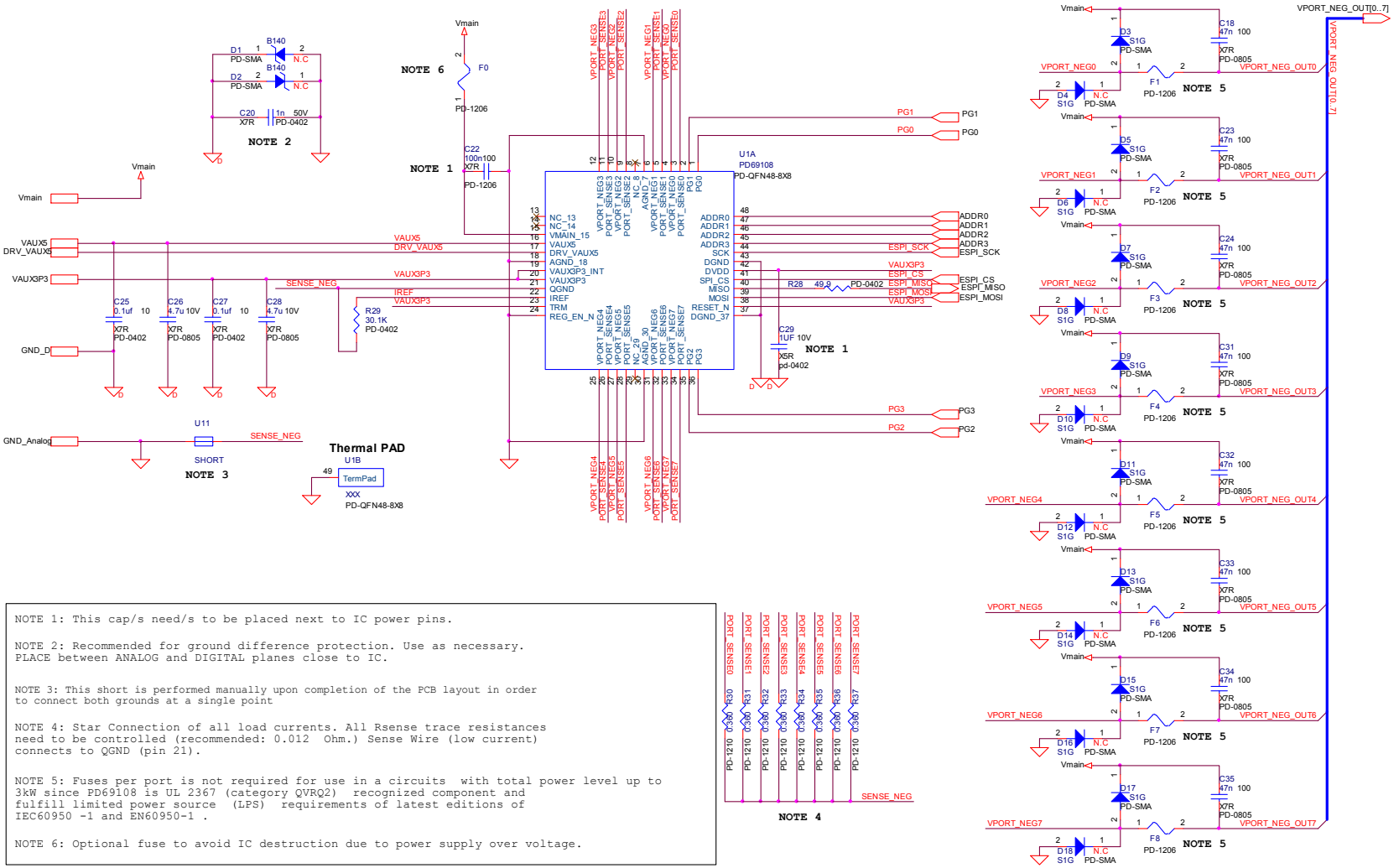

Figure 8: PD69108 Circuitry for PoE Manager #0 (6 PL)

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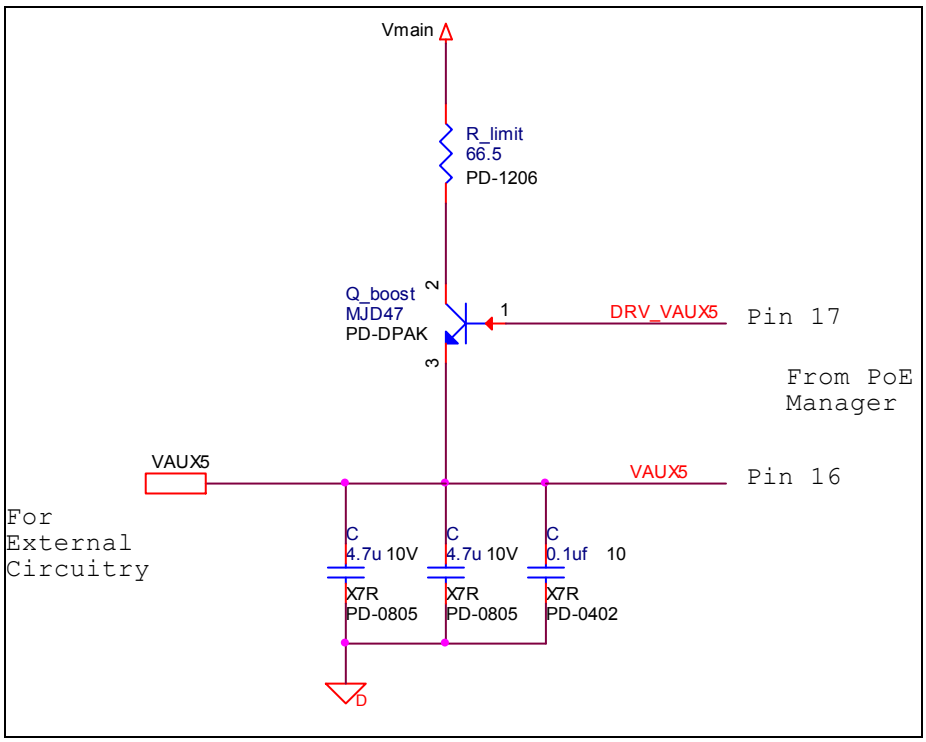

Figure 9: Optional Boost Transistor Circuitry

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Bill of Materials for a PoE System

Table 1: Main Block Components

Block	Qty	Reference	Description	PCB Foot Print	Manufacturer	Manufacturer's Part Number
Main	4	C1-C4	CAP ALU 47 uF 100 V 20% 8X11.5 105C P = 3.5 mm	D8H11_5F3_5	Rubycon	100PX47M T7 8X11.5
	2	C5,C6	CAP CER 0.1 uF 10 V X7R 10% SMT	PD-0402	Murata	GRM155R71C104KA88D
	1	R1	RES TCK FLM 10K 1% SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	4	R2-R5	RES TCK FLM 49.9R 1% SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF
	1	U9	IC Dig.Isol	PD-SOW16	Analog Devices	AD80273ARWZ-RL**

Table 2: PoE Controller Components

Block	Qty	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Controller	1	C7	CAP CRM 2.2µF 10V 10% X7R SMT	PD-0805	Samsung	CL21B225KPFNNNC
	4	C8-C11	CAP CER 0.1µF 10V X7R 10% SMT	PD-0402	Murata	GRM155R71C104KA88D
	2	C12,C13	CAP CER 22pF 50V 5% NPO SMT	pd-0402	Kemet	C0402C220J5GAC
	1	C14	CAP CER 1nF 50V X7R 10% SMT	PD-0402	Murata	GRM36R71H102KA01L
	3	R7,R8,R21	Resistor,SMT 49.9K, 1%, 1/16W 0402	PD-0402	ASJ	CR10-4992FK
	4	R9,R14,R16, R27	RES TCK FLM 10K 1% SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	3	R10, R25, R26	RES 0R 5% SMT MTL FLM	PD-0402	Vishay	CRCW0402-0R0 5% ET1 E3
	1	R6	RES 2.21R 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW04022R21FKED
	1	R12	RES TCK FLM 10R 1% SMT	PD-0402	Bourns	CR0402-FX-0100-ELF
	1	R15	RES TCK FLM 348R 1% SMT	PD-0402	Rohm	MCR01MZPF3480
	4	R17-R20	RES TCK FLM 49.9R 1% SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF
	1	R24	RES TCK FLM 8.87K 1% SMT	PD-0402	Yageo	RC0402FR-078K87L
	1	U7	PoE Controller	VFQFPN36	Microsemi	PD69100
	1	XT1	0SC CRISTAL SMT 8MHz 16pF	HC49-4H-SMD	Golledge Electronics	GSX49-4-8MHZ 16P

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Table 3: PoE Manager Components

Block	QTY*	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Manager	1	C20	CAP CER 1nF 50V X7R 10% SMT	PD-0402	Murata	GRM36R71H102KA01L
	1	C22	CAP CRM 100nF 10 0V 10% X7R SMT	PD-1206	AVX	12061C104KAT2A
	8	C18,C23,C24, C31-C35	CAP CRM 47nF 100 V 10% X7R SMT	PD-0805	Murata	GRM40X7R473K100
	2	C25,C27	CAP CER 0.1µF 10 V X7R 10% SMT	PD-0402	Murata	GRM155R71C104KA88D
	2	C26,C28	CAP CRM 4.7µF 10 V 10%^^X5R SMT	PD-0805	Murata	GRM219R61A475KE19D
	1	C29	CAP CER 1.0µF 10 V X5R 10%	pd-0402	Panasonic	ECJ-0EB1A105M
	8	D3,D5,D7,D9, D11,D13,D15, D17	DIO RECOV. REC 400V 1A++SMA SILICON SMT	PD-SMA	Diodes Inc.	S1G
	8	F1-F8 ***	FUSE 1.5A 63V V. FST BLO SMT	PD-1206	Bussmann	TR1/CC12PD-1.5A -R**
	1	R28	RES TCK FLM 49.9R 1% SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF
	1	R29	RES TCK FLM 30.1K 1% SMT	PD-0402	Panasonic	ERJ2RKF3012X
	8	R30-R37	RES TCK FLM 0.360R 1% 0.5W 200PPM^1210 SMT	PD-1210	Rohm	MCR25JZHFLR360
	1	U1	PD69108ILQ, 8 Ports PSE IC	PD-QFN48-8X8	Microsemi	PD69108ILQ

*These quantities should be multiplied by the number of PD69108 (six managers in this paper)

**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.
***Fuses per port are not required for use in circuits with total power level of up to 3kW. That's because PD69108 is UL 2367 (category QVRQ2) recognized component and fulfills limited power source (LPS) requirements of latest editions of IEC60950-1 and EN60950-1.

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 4 Feb 2010	-	Initial Release – Preliminary version
0.9 / March 2010		Release
0.91 / March 2011		Update BOM
1.0 / Agust 2011		
1.1 / Dec 2011		Add 4-pairs functionality
1.2 / Jan 2012		
1.3 / Mar 2012		General update
1.5 / Sep 2012		Fuse per port is mandatiry only for systems suppling more then 3KW+ General update

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