
Migrating from ACT1 to 40MX Family FPGAs

Table of Contents

Purpose	1
Introduction	1
References	1
Comparison	2
Pin-to-Pin Comparison.	2
Power-Up Recommendation.	2
Configuring Unused I/Os	3
Design Migration Procedure.	3
Manual Migration Procedure.	5
Timing Validation	8
Programming	8
Summary	8
Conclusion.	8
Appendix.	9
List of Changes	10

Purpose

This application note provides the information needed for migration of a design from the ACT1 family to the 40MX family.

Introduction

The 40MX device architecture is based on the ACT1 family and shares the same library of device macro cells. There is a direct one-to-one mapping of ACT1 cells to 40MX cells and therefore, does not require a re-synthesis of the design for migration. The 40MX uses 0.45 μm triple-metal CMOS process, enabling significant improvements in performance. Similar to the ACT1 devices, the 40MX FPGAs are Oxide-Nitride-Oxide (ONO) antifuse-based, single-chip solutions. The 40MX devices are 5 V compliant. The 40MX devices are footprint compatible with equivalent ACT1 devices, eliminating the need for any board level modifications.

References

- [ACT 1 Series FPGAs](#)
- [40MX and 42MX FPGA Families](#)
- [Static Timing Analysis Using Designer's Timer](#)
- [Default Settings for Unused I/O and Clocks](#)
- [Libero IDE Design Flow](#)

Comparison

Table 1 shows the recommended migration path for architecturally compatible devices. For a given ACT1 device, the recommended 40MX device is shown in the same colored grouping. All die-package combinations of ACT1 devices have direct die-package compatible 40MX devices.

As shown in Table 1, any design from the ACT1 family can be directly converted to the 40MX family by using a TCL script, which is described later in the "Migrating Using TCL Script `migrate_to_mx.tcl`" section on page 3. The logic placement and I/O assignments remain exactly the same as the original design.

Table 1 • Device Comparison Between ACT1 and 40MX

Devices	A1010B/A10V10B	A40MX02	A1020B/A10V20B	A40MX04
System Gates	3000	3000	6000	6000
Logic Modules				
Seq	—	—	—	—
Comb	295	295	547	547
Flip-Flops (maximum)	147	147	273	273
Clocks	1	1	1	1
User I/Os (maximum)	57	57	69	69
Packages (by pin counts)				
CPGA	84	84	84	84
CQFP	—	—	84	84
PLCC	44, 68	44, 68	44, 68, 84	44, 68, 84
PQFP	100	100	100	100
VQFP	80	80	80	80

Pin-to-Pin Comparison

Power Supply Pin Comparison

The supply voltage pins (VCC & GND) of the 40MX family are fully compatible with the ACT1 device. There are some NC (No Connect) pins which are not connected to any circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

Both ACT1 and 40MX devices can operate with a 5.0 V or 3.3 V input supply voltage.

I/O Comparison

All I/Os are at the same physical location for compatible devices that have the same package.

Special Pins Comparison

MODE, PROBEA and PROBE B, SDI, SDO, and DCLK pins are fully compatible in terms of location, default configuration, and functionality.

Power-Up Recommendation

Both 40MX and ACT1 devices operate with one power supply (VCC). Refer to *40MX and 42MX FPGA Families Datasheet* for the Transient current requirement during power-up.

Configuring Unused I/Os

By default, unused I/Os in ACT1 and 40MX devices are configured as low drivers by the Microsemi Designer software, as shown in Figure 1. Unused I/Os should be terminated to GND or left floating. Do not drive an unused I/O to any value other than GND.

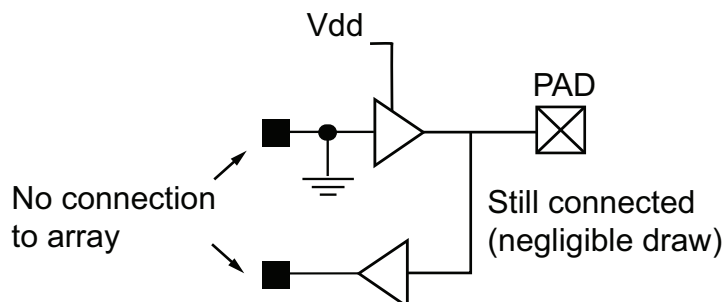


Figure 1 • Configuration for Unused I/Os in ACT1 and 40MX

Design Migration Procedure

The ACT1 and 40MX families are fully supported by Microsemi Libero® IDE (Integrated Design Environment) and Microsemi Designer FPGA development software. This section provides instructions for using the Microsemi Libero IDE / Designer tool suite to migrate from ACT1 to the 40MX family. Design files, such as an ADB file or ADL, EDN, and PIN files, are required to complete the process. An independent TCL script is provided for an automated migration flow to generate a 40MX ADB file without manual intervention. This script automatically manages all conversion steps, such as timing constraints, compatible package selection, setting operating conditions, and others. Microsemi strongly recommends using the script flow as the primary method of design migration to the 40MX family.

Migrating Using TCL Script `migrate_to_mx.tcl`

Download `migrate_to_mx.tcl` script file at:

http://www.microsemi.com/soc/download/rsc/?f=migrate_to_mx_1_12

This script automatically finds the compatible die and package in the 40MX family. This TCL script can be run in batch mode or the Designer GUI.

Running TCL Script in Batch Mode

File(s) required: Original.adb and migration tcl

Usage:

```
<command prompt>><path to Designer software installation "bin" directory>/Designer
script:<path to tcl script file>/migrate_to_mx.tcl+<path to original adb file>/original.adb+<path to
new adb file>/newname.adb logfile:<path to log file>/newname.log
```

Refer to Figure 2 for an example.

To specify the path to your files, use a forward slash (/).



```
Administrator: C:\Windows\system32\cmd.exe
C:\Users\ugginis>I:\9_2_2_1_prod9\Designer\bin\designer script:D:/act_mx_migrate/migrate_to_mx.tcl+D:/act_mx_migrate/top.adb+D:/act_mx_migrate/migrated.adb logfile:D:/act_mx_migrate/migration_log.log
```

Figure 2 • Example TCL Script

After running this command, the new ADB, ADL, and LOG file are generated in the specified directory.

Running TCL Script in Designer GUI

Original design files required: design.adb

Open the ACT1 ADB file in Designer and select **File > Execute Script**. Enter the destination where you want to save the new 40MX ADB file into **Arguments**. Click **Run**, as shown below in [Figure 3](#).

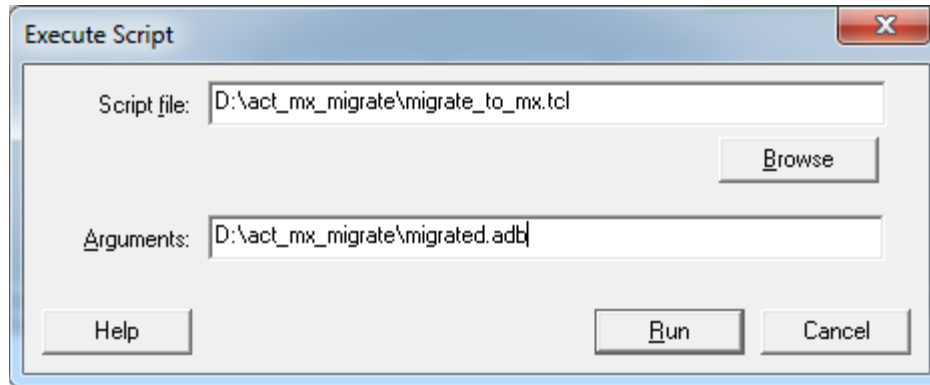


Figure 3 • Execute Script

Click **Save**, if the script succeeds with the migration procedure. Otherwise, the new ADB file will be at the original state of the design before the execution of the script.

Manual Migration Procedure

Original design files required: design.adl OR desing.edn, design.pin

The manual migration procedure is required when the ACT1 adb file is not available and the ADL or EDN (netlist), and PIN (pin location) files are available.

Step 1: Creating New 40MX Project in Designer

In Designer, choose **File > New**. Enter the design name and select the family **40MX**, as shown in Figure 4.

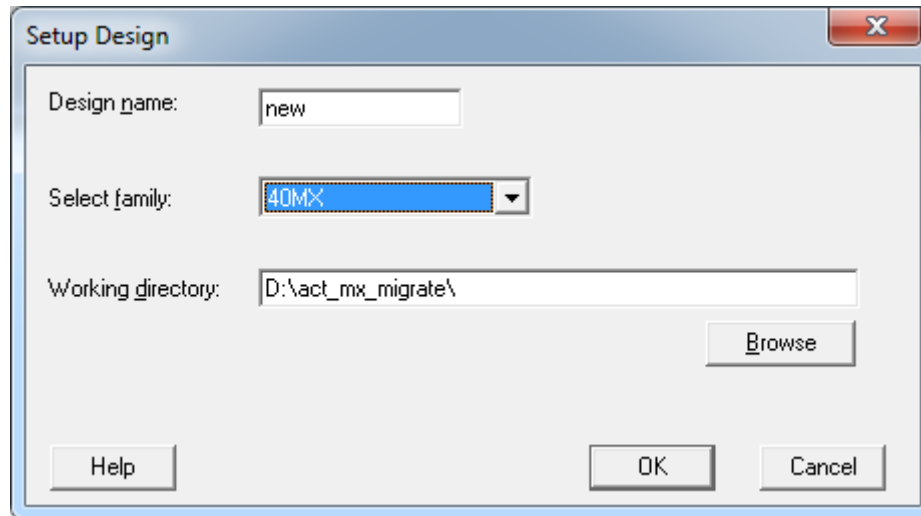


Figure 4 • Setup Design

Step 2: Importing Netlist and Pinout List into New 40MX Project

Choose **File > Import Source Files**. Add the ADL or EDN netlist and PIN files of the ACT1 design into the new 40MX project, as shown in Figure 5.

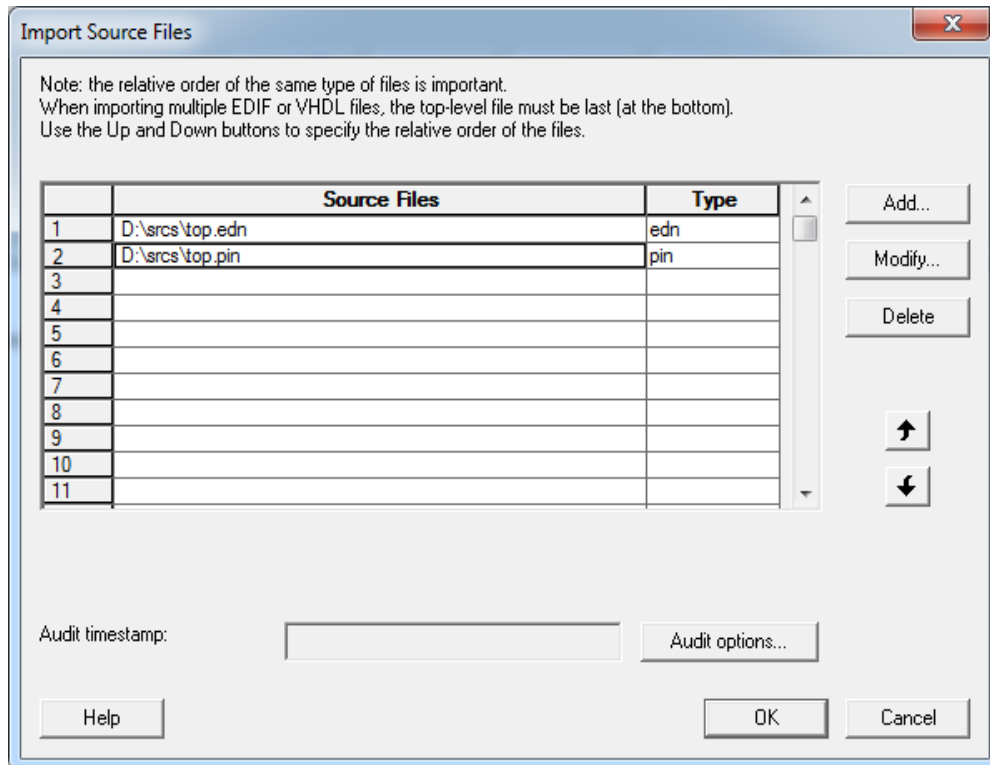


Figure 5 • Importing Source Files

Step 3: Following the Design Flow

Click the **Compile** button. **Device Selection Wizard** window opens. Choose the compatible 40MX die package from Table 1, as shown in Figure 6.

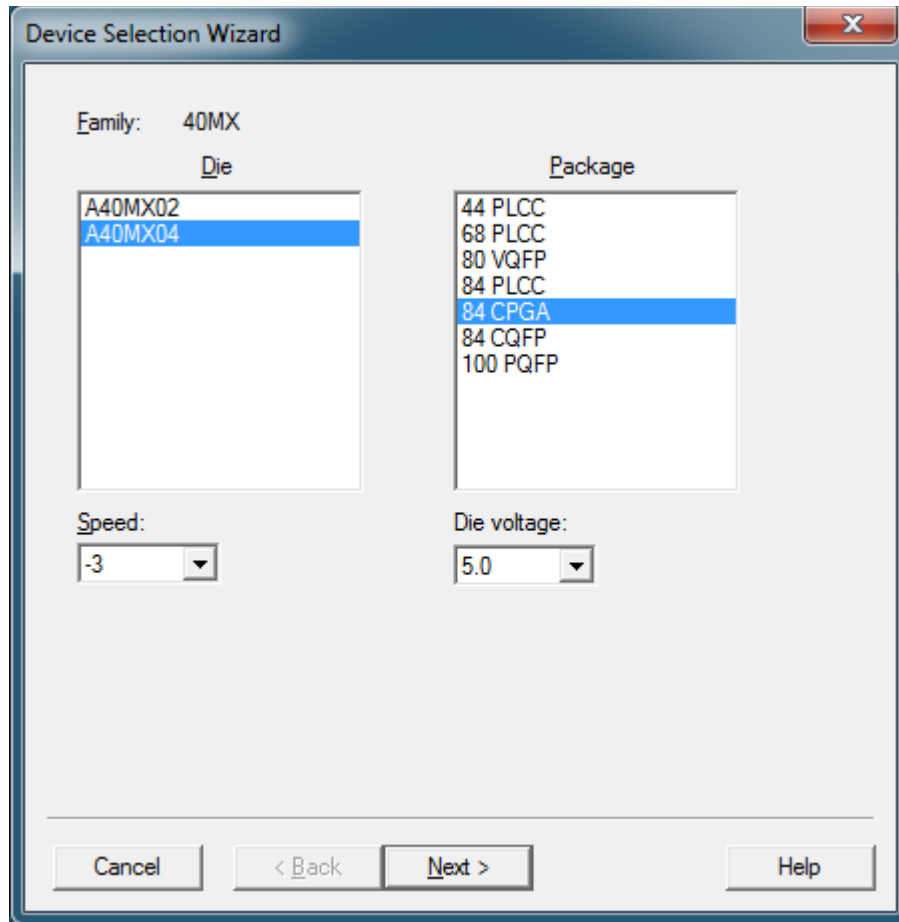


Figure 6 • Device Selection Wizard

Also, set identical operating conditions and carefully choose the device speed grade for the new 40MX design. Examples of operating conditions are die voltage, Restrict-Probe-pins, Junction temperature and Voltage range.

Timing Validation

None of the conversion flows described above perform timing analysis on the converted design. Manual timing validation is required.

The 40MX family is faster than the ACT1 family. Microsemi recommends that a new timing analysis be performed. Hold times, cross clock domain paths, clock-to-out, and multi-cycle paths should be carefully analyzed to ensure no timing problems exist in the converted design. Refer to the [Static Timing Analysis Using Designer's Timer](#) application note for more information on performing timing analysis using the Microsemi Timer tool. Also, verify the potential simultaneously switching outputs by checking whether various adjacent outputs have enough timing differences (staggered timing) to avoid negative effects. Refer to [Simultaneous Switching Noise and Signal Integrity](#) application note for details. 40MX I/Os have faster slew rate than ACT1 devices. Run board level signal integrity analysis before finalizing the board design. Refer to [Using Schmitt Triggers for Low Slew-Rate Input](#) application note for details. The manual migration procedure does not preserve all placements, even for compatible packages. To preserve the timing constraints, export the DCF, CRT files from the ACT1 design and import them as Auxiliary Files into the 40MX design after the Compile step. The `migrate_to_mx.tcl` script automatically preserves timing constraints as well as all placements if possible.

Programming

Programming Software

Programming files are not compatible between the two families. Generate a new programming file (AFM) from the migrated design.

Programming Hardware

Silicon Sculptor 3 uses the same module for both families. Refer to the Microsemi website for a list of [Silicon Sculptor modules](#).

Summary

The following steps describe how to migrate from ACT1 to 40MX:

1. Determine the compatible 40MX device and package from [Table 1](#)
2. Update to the latest version of Libero IDE software and follow the ["Design Migration Procedure" on page 3](#)
3. Confirm pin placement in the new adb
4. Perform timing analysis on the converted design
5. Generate a new 40MX programming file
6. Program 40MX using Silicon Sculpture 3 (use the latest revision of the adapter module) and the latest programming software version

Conclusion

The 40MX family shares numerous architectural features and the library of basic elements with the ACT1 family, and offers higher speed and special functionalities. Understanding the differences between the two families makes a seamless migration from ACT1 to the 40MX family possible.

Appendix

Table 2 • Migration Packages

ACT1 Die / Package	Suggested Migration
A1010B/A10V10B	A40MX02
PL44	PL44
PL68	PL68
PQ100	PQ100
VQ80	VQ80
PG84	PG84
A1020B/A10V20B	A40MX04
CQ84	CQ84
PG84	PG84
PL44	PL44
PL68	PL68
PL84	PL84
PQ100	PQ100
VQ80	VQ80

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 1 (November 2014)	Updated the document for SAR 62569.	NA
	Updates made to maintain the style and consistency of the document.	NA
Revision 0 (May 2013)	Initial Release.	NA
<i>Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.</i>		



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