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Layout Design Guidelines

for

PD69104B PoE Systems

User Guide

Revision 0.5

Catalog Number PD69104B_UG_LAYOUT

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Microsemi
Analog Mixed Signal Group
1 Enterprise, Aliso Viejo, CA 92656, USA; Within the USA: (800) 713-4113, Outside the USA: (949) 221-7100 Fax: (949) 756-0308

Introduction

This application note provides detailed information and PCB design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's™ 4-channel PoE Manager - the PD69104B. Using this application note, the PCB designer can integrate PoE capabilities into an Ethernet switch.

PD69104B device is a 4-port, mixed-signal, high-voltage PoE driver. It enables detection of IEEE802.3at-2009 compliant, Type 1 and Type 2 PDs (Powered Devices), ensuring safe power feeding and disconnection of ports with full digital control and a minimum of external components. The PD69104B is designed to implement all real time functions as specified in the IEEE 802.3af and IEEE802.3at standards including detection, classification and port status monitoring, as well as system level activities such as: power management and MIB support for system management. PD69104B is designed to detect and disable disconnected ports, using DC disconnection methods only.

This application note is to be used in conjunction with application note *AN-198, Catalog Number 06-0134-080*.

Applicable Documents

- IEEE802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69104B datasheet, catalog number 06-0057-058
- Microsemi Application Note AN-198 for Designing a 4-port Auto mode PoE System

Isolation and Termination

According to the IEEE 802.3af and the IEEE802.3at standards, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations.

These requirements are taken into account by PoE switch vendors, while designing the switch circuitry. However, when a PoE Manager is integrated into a switch, special design considerations must be met, due to the unique combination of data and power circuitries.

The following paragraphs define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating Microsemi's PoE Chip Set and daughter boards.

Isolation

As specified in the IEEE PoE standards, 1500 Vac rms isolation is required between switch's main board circuitry, including protective and frame ground, and the Media Dependent Interface (MDI). Figure 1 illustrates the overall isolation requirements.

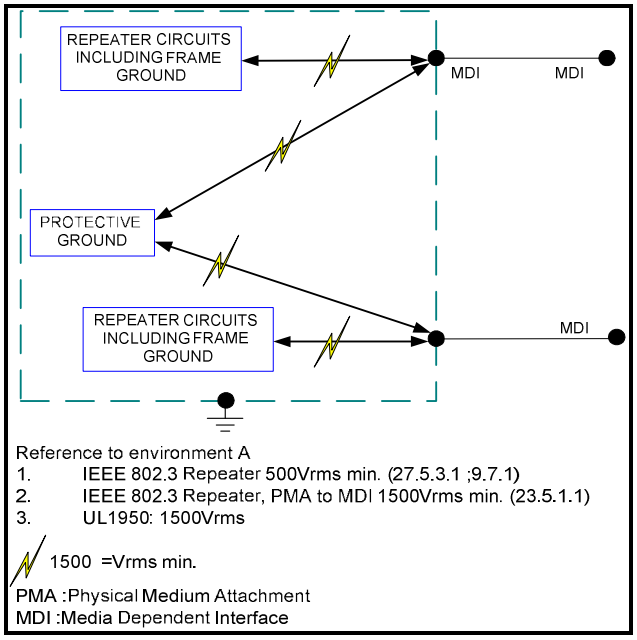

Figure 1: Isolation Requirements Scheme Meeting Requirements

High Voltage Isolation

- For a switch with no PoE circuitry: isolation requirements between the physical input terminals and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers (see Figure 2).
- When integrating a PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation, if the PoE ground or DC input is connected to the switch's circuitry/ground.

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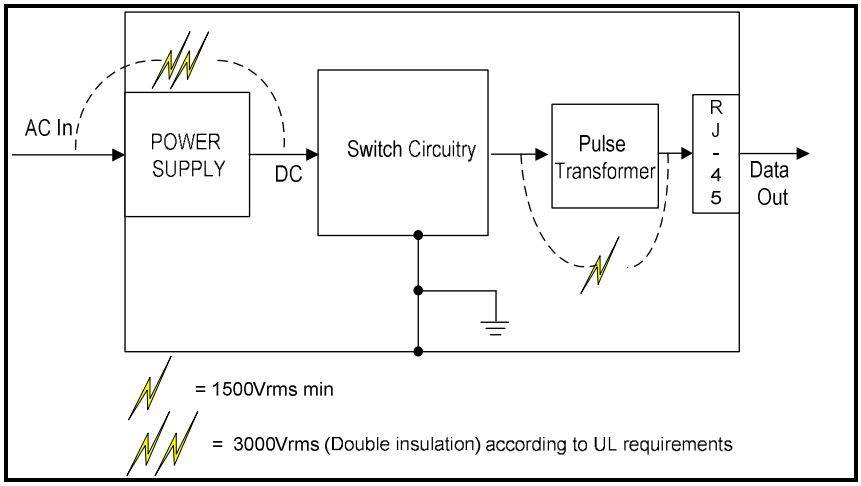

Figure 2: Standard Switch Circuitry

To comply with the above isolation requirements, the PoE managers must be isolated in regards to all other switch circuitries. Use one of the following methods:

- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry (see Figure 3).
- A single DC input (separate power supplies) for both the switch and PoE circuit as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry (see Figure 4).

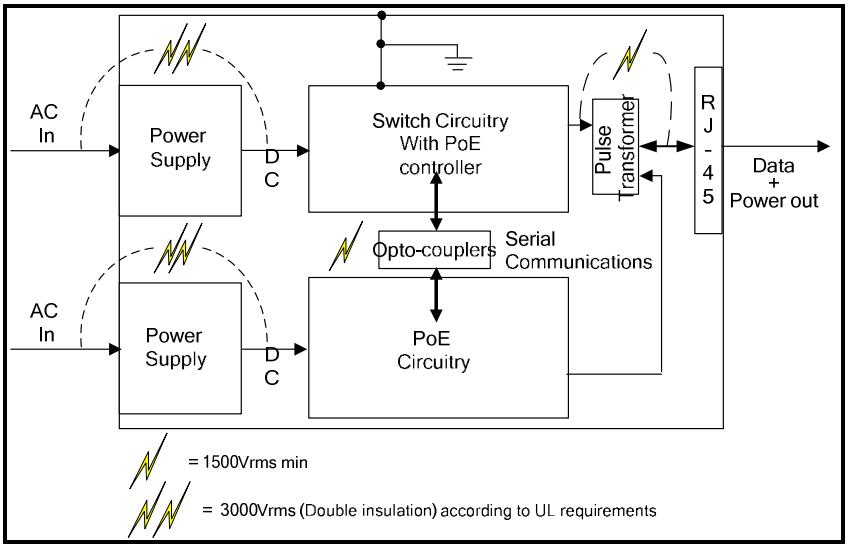

Figure 3: Switch Circuitry with Two DC Sources

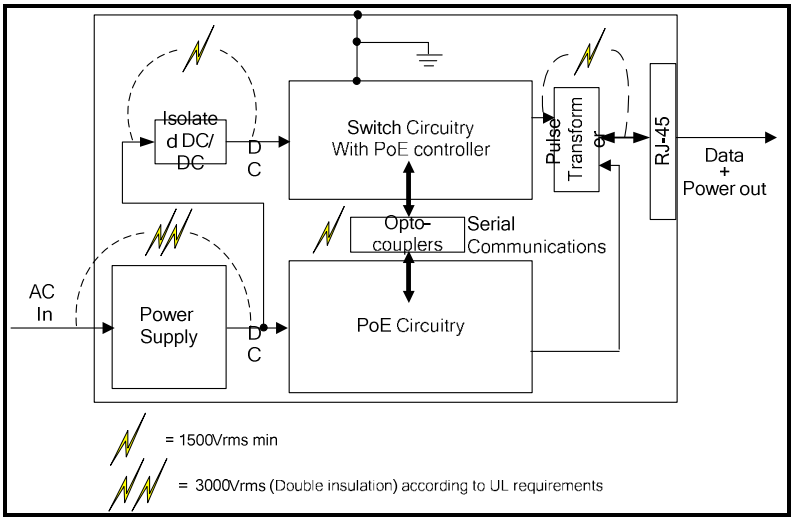

Figure 4: Switch Circuitry with a Single DC Source

To maintain 1500V_{rms} isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended. This provides a safe margin for hi-pot requirements.

PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit output terminals to the switch circuitry (see Figure 5). Note that in most PoE systems, it is recommended to use 0Ω resistors for R1 and R2. However, certain systems may benefit from 75Ω resistors. Filtering provisions should be made. Note that in quiet PoE systems the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes:

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note For best EMI performance and to avoid additional noise accumulated on the lines between filter and port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs or the spare pairs. Both methods are detailed in Figure 6 which illustrates an MDI-X (or Auto MDI-X) connection associated with the switch.

Isolating the Stacked Modular Jack Assembly

IEEE PoE standards require 1500V_{rms} isolation between PoE voltages and frame ground (EGND). Notice that RJ-45 jack assemblies have a metal cover of 80 mils that almost reaches the PCB surface.

Maintain an 80 mils traces clearance between EGND traces for RJ-45 modular jack assembly metal covering and for adjacent circuit paths and components. To prevent 1500V_{rms} isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE technology involves voltages as high as 57VDC. Thus, plan adjacent traces for 100VDC operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

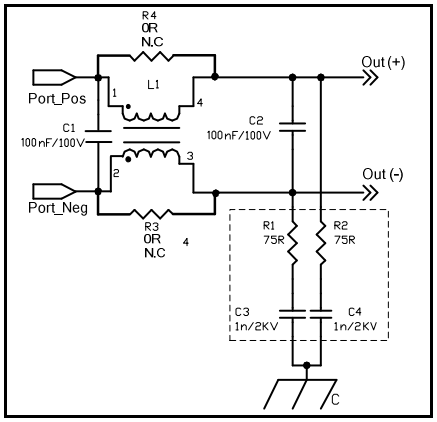

Figure 5: Recommended EMI Filter

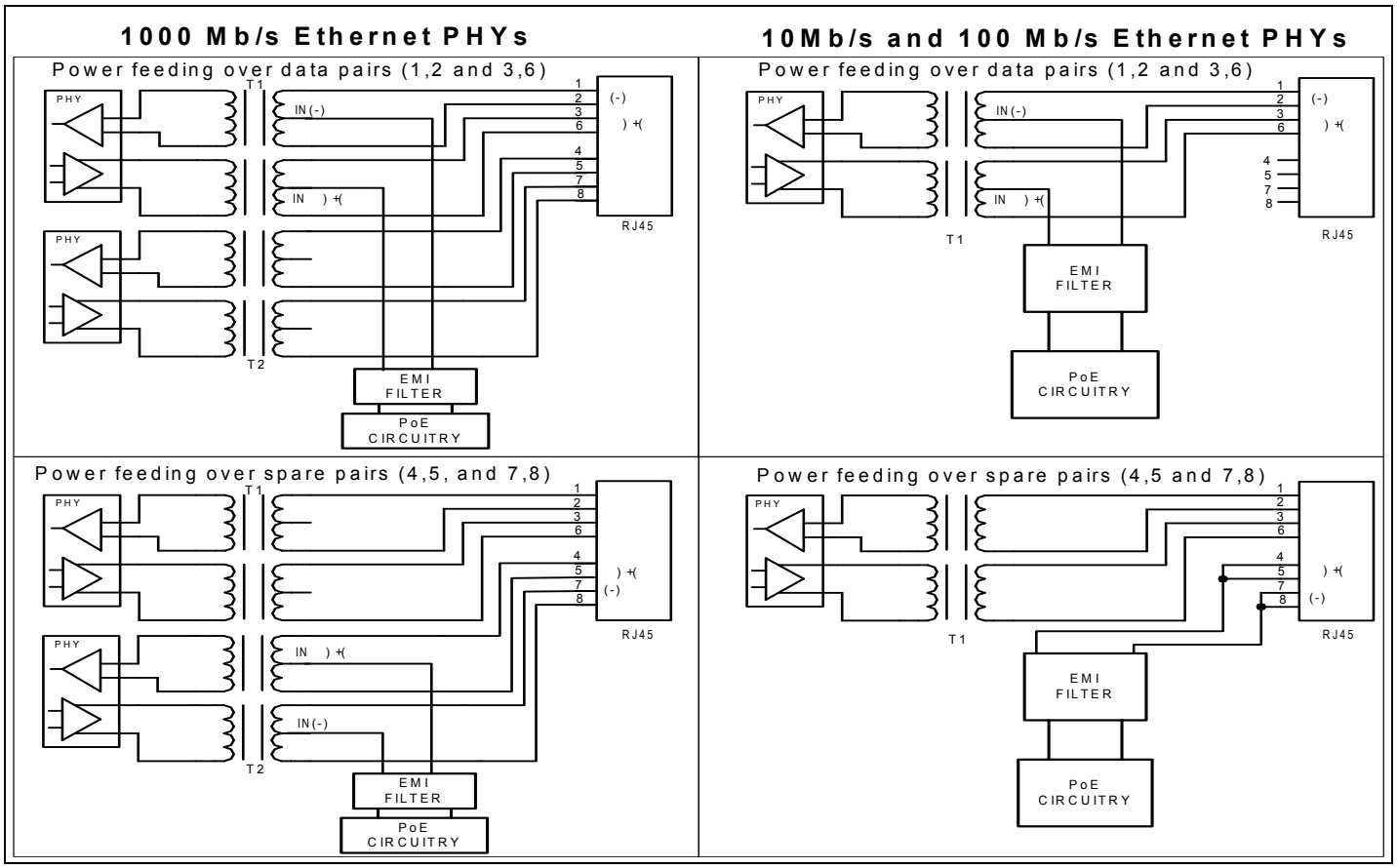

Figure 6: Output Ports Design Details

Layout Guidelines

Microsemi's PD69104B PoE Manager is designed to simplify the integration of PoE-circuitry into switches, based on the IEEE PoE standards. The pin-out arrangement has been configured for optimal PCB routing. Following are Microsemi's recommendations for proper PCB layout.

Figure 7 describes the various circuits and elements surrounding the PD69104B PoE Manager in the block diagram. This block diagram includes the following peripheral elements, identified by numbers:

- 5V voltage source (VAUX5) (1)
- 3.3V voltage source (VAUX3P3) (2)
- Sense resistor for current measurement (3)
- Output capacitor used for filtering (4)
- Protection fuse (5)
- Protection diode against reverse polarity (6)
- RESET, I2C bus, I2C address lines (7)
- Power good inputs (8)

Note The VAUX5 supply may include an external transistor connected to pin 16, destined to increase current drive for external circuitry. To prevent heat from being transferred to the PD69104B, place this transistor away from PoE managers.

For details on the interconnection circuitry of the PD69104B, refer to the application notes listed in the "Applicable Documents" section.

The provided circuitry is intended to facilitate the design of a switch when integrating a PoE capability into it.

Locating PoE Circuitry in a Switch

To minimize the length of high current traces, as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's pulse transformers. Circuit can be fully integrated into switch's PCB, or can be easily placed on top of the switch, using daughter board PoE application. Typical integration of PoE modules inside a switch is shown in Figure 9 and Figure 10

Ground and Power Planes

Since the Chip Set PoE solution (PD69104B) is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines.

Reference design assumes a four layer board: top, mid1, mid2, and bottom. The main planes are Vmain/AGND, DGND.

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Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines, as illustrated in Figure 11:

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69104B (see Thermal Pad Definition and Design). AGND should be the bottom layer.
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure Maintain an 80 mils traces clearance between EGND traces and all other traces.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds as shown in Figure 12 and Figure 13.
- Grounding layout is recommended to be implemented as described in Figure 13.
- To minimize noise effects from the heavy currents flowing to the ports, a number of separate grounding areas are essential in the design. Establish several separate ground areas to concentrate sensitive circuits, apart from the main grounding surfaces.
- To connect various DGND points and to enable stable impedance to the I2C bus traces, extend the digital ground (DGND) surface under pins 35–48 of the PD69104B managers.
- R_{sense} resistors for each PoE Manager are all connected to local "star point". The star center is connected to the analog ground (AGND) using four tied power via's of 6 mil diameter each (see Figure 12, Figure 13 and Figure 14).
- In addition, the R_{sense} resistors' "star point" connection to the PD69104B utilized as #0, is to be the focal interconnection point for the digital and analog grounds (see Figure 13).
- Leave spacing for a ceramic 1nF bypass capacitor near each PoE Manager (marked as "Cb" in Figure 13) between the analog and digital layers near each PoE Manager. The capacitors form low impedance paths for digital driving signals.
- Leave appropriate spacing (provision) for two parallel and inversed Schottky diodes (Da, Db, Figure 13) between analog and digital layers near each PoE Manager. The diodes form low impedance paths for highly energized signals running between analog and digital layers and enhance circuit immunity.
- The power and return (ground) planes for the 48V supply must be designed to carry 35A continuous current, based on full 48-port capacity. Minimize DC power losses on this plane by using a wide copper land. When implementing the PoE circuitry on a daughter board, the hi current does not have to be routed through the daughter board but only the return path as can be noted from Figure 8.

Current Flow through PoE Application

See Figure 8

Port's current flows in a DC disconnect application as follows:

1. Switch's power supply provides a positive line, reaching the center taps via a mother-board, on a wide trace (not through DB).

2. From the center tap of the line transformer via switch's RJ45 to the PD side.

3. The return current from the PD flows via RJ45 and line transformer to DB PoE circuitry.

4. From DB analog ground (AGND) the current flows back to switch's power supply negative, via a harness.

Note The positive port's heavy current flows directly to the PD side without going through PoE DB Managers.

Specific Component Placement

Peripheral Components

To prevent heat transfer among various components, the following gaps should be maintained:

- Minimum gap between PD69104Bs should be 45mm
- To prevent a hot spot on the PCB, do not group sense resistors together under full load conditions. It is recommended to leave at least 10mm between PD69104B and its sense resistors.

PD69104B PoE Manager and Peripherals

- The side of the PoE Manager that includes pins 37 to 48 should face the digital ground (DGND plane). The pins function as communication and control pins for the Manager (connect between PoE Manager and PoE controller via isolation circuitry).

- Locate the bypass capacitors for the PoE Manager supply input close to the relevant pin. In cases where two bypass capacitors are placed on the same line, locate the lower value capacitor closer to the pin on the same layer and place the higher value capacitor at a more distant location.
- Locate VAUX5 and VAUX3P3 0.1µF and 4.7µF filtering capacitors as close as possible to PoE Manager pins 16 and 20, respectively.

Conductor Routing

General Guidelines

Conductor (or printed lands) routing is to be performed as practiced in general layout guidelines, specifically:

- Conductors that deliver a digital signal are to be routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.
- The total resistance of all sense resistor traces (both sides) needs to be 6mΩ.

Specific Requirements for Clock and Sensitive Signals

Issues that require special design considerations:

- Each PD69104B's port incorporates a current sense resistor. For proper power management and control, layout these lines so that adjacent ports current flow or excessive path resistance doesn't impede measured current. To do this, use a single common point to aggregate the current flow of all 4 ports to the analog ground (AGND) layer. This point is referred to as the local PoE Manager "star point" (see Figure 11, Figure 12 and Figure 13). It is critical to design the total layout path (traces resistance from PORT_SENSEx pin to AGND star point) for an accurate resistance value, since a wrong resistance value results in a current measurement error and unreliable power management. Parasitic resistance added by the layout traces must be 6mΩ. Since routing requires narrow traces in some areas, wide traces in other areas are necessary for achieving a total trace resistance of 6mΩ.
- The local "star point" needs to carry high current from the sense resistors to AGND. To achieve this, use four tied power vias of 6 mil diameter each (see Figure 14). Avoid using plugged vias to preclude temperature rise.
- Route a senses trace (SENSE_NEG) from QGND (pin 21) to the local PoE Manager "star point".
- PD69104B's AGND (pins 6, 18, 31) must also be connected directly to the local PoE Manager "star point" through individual traces.
- The IREF resistor used for current reference (connects to pin 22), is directly connected to QGND (pin 21).
- Carefully route the I^2C/UART communication clock (SCL) line coming from the Host so that it will not disturb other lines. Two ground lines (connected to DGND) could be routed alongside the clock line to isolate it from the rest of the lines.

Port Outputs

For robust design, the ports output traces are to be 45 mils wide so as to handle maximum current and port power.

However, to obtain a 10°C (maximum) copper rise, set the minimum width for traces in accordance with the layer location and copper thickness:

- For two ounce copper, external layer should be 15 mils.
- For two ounce copper, internal layer should be 20 mils.
- For one ounce copper, external layer should be 25 mils.
- For one ounce copper, internal layer should be 30 mils.
- For 1/2 ounce copper, external layer should be 30 mils.
- For 1/2 ounce copper, internal layer should be 55 mils (20°C copper rise).
- The ports output traces must be short and parallel to each other, to reduce RFI coupling and to keep the series resistance low.
- The PoE output ports must be connected to the switch's pulse transformers as shown in Figure 6. The common mode choke is used to reduce RFI noise. A 'Bob-Smith' termination (resistor-capacitor) to chassis ground is optional. The circuit is to be located as close as possible to the pulse transformer.

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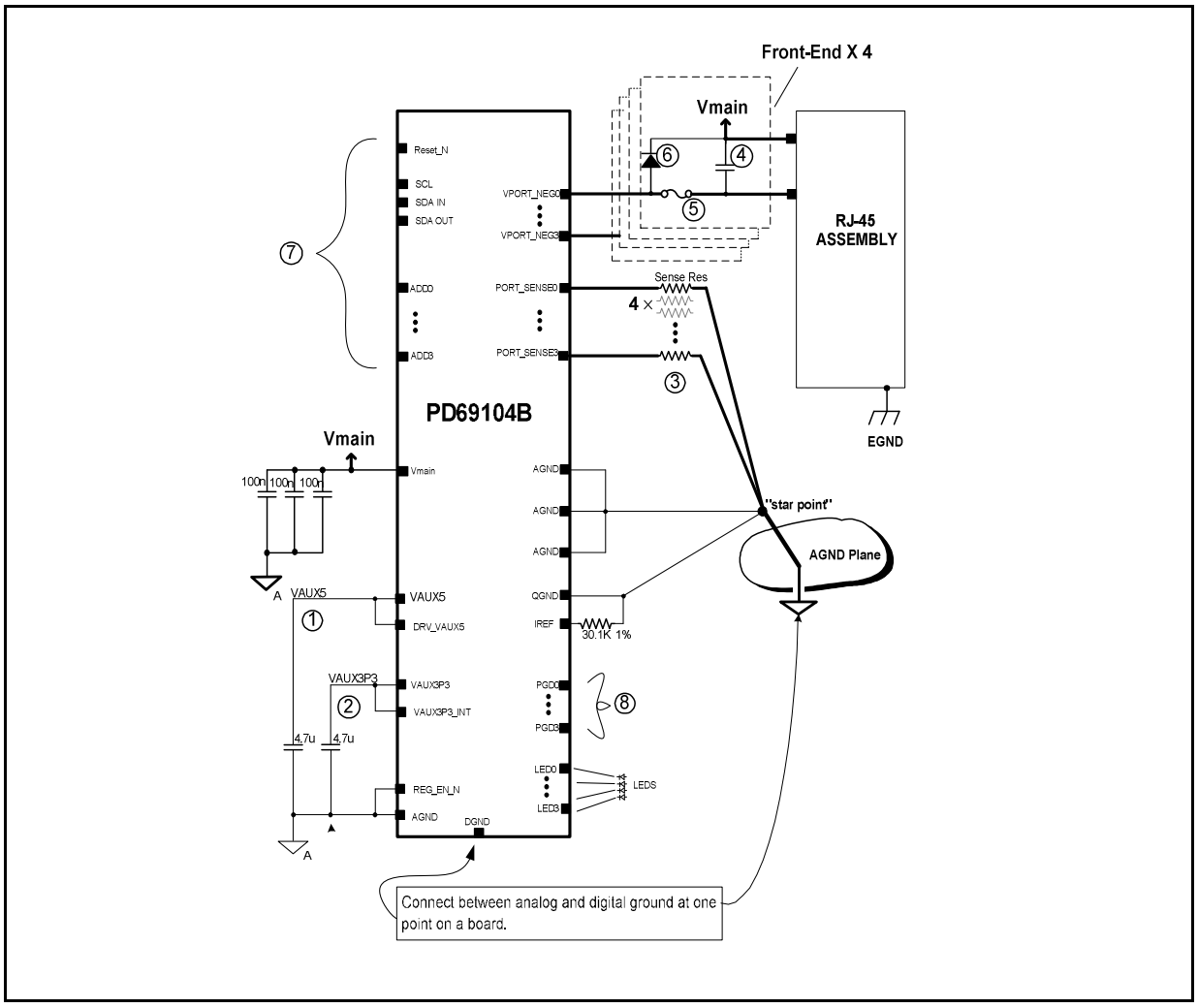

Figure 7: Component Identification for PD69104B Circuitry

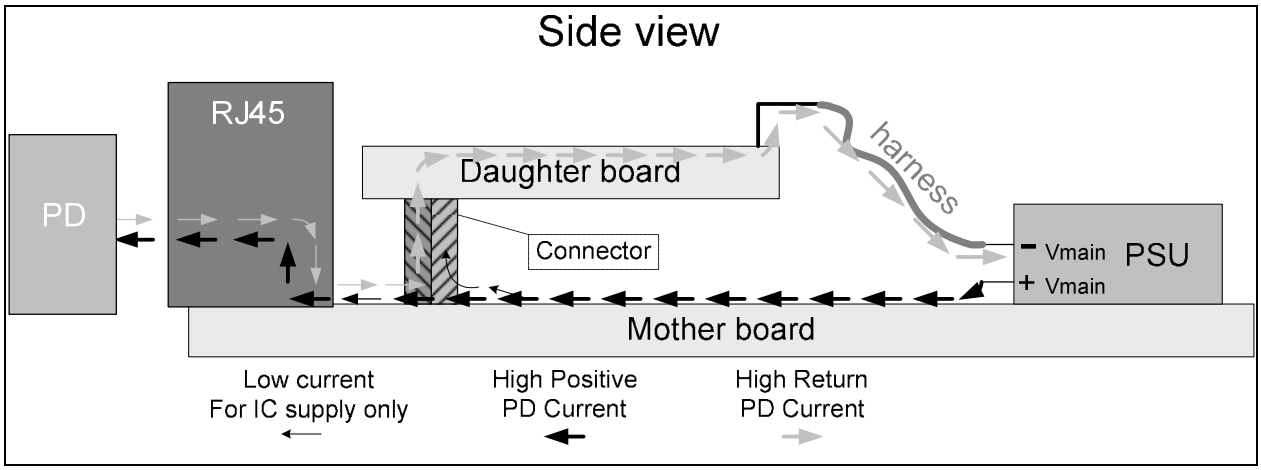

Figure 8: Component Identification for PD69104B Circuitry

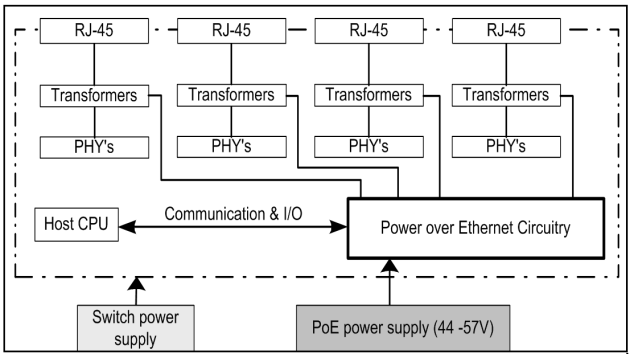

Figure 9: Block Diagram – PoE Circuitry inside the Switch

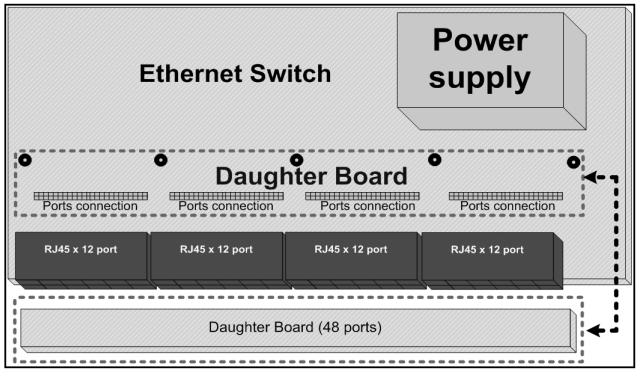

Figure 10: PoE DB Circuitry inside the Switch

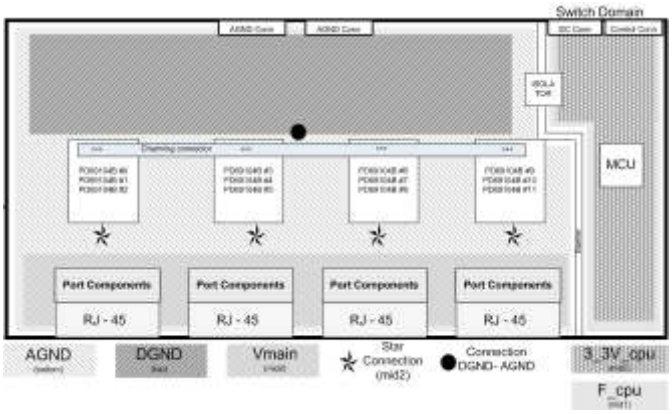

Figure 11: Ground and Power Planes

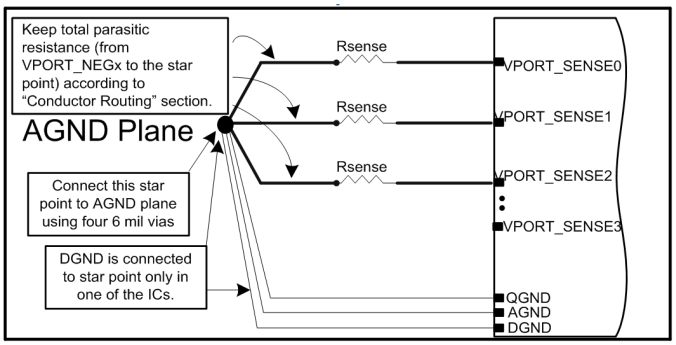

Figure 12: Star Point and Sense Resistors Design Criteria

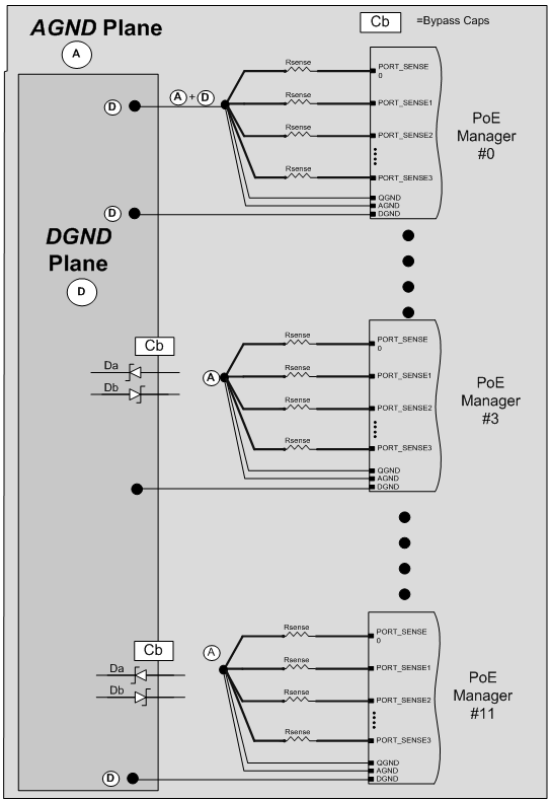

Figure 13: Overall Grounding Scheme

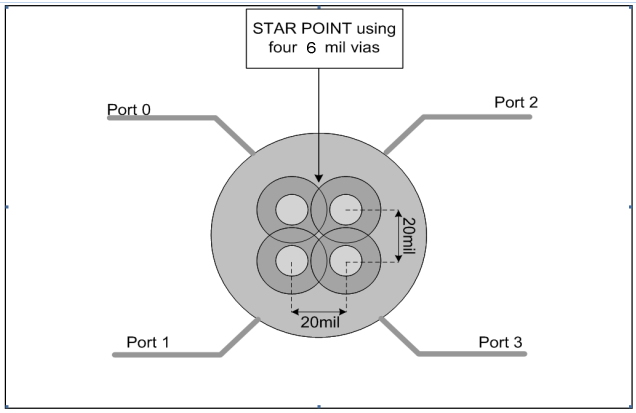

Figure 14: Star Point Layout

Thermal Pad Definition and Design

PD69104B utilizes a thermal dissipation exposed pad in a 48-pin 8x8 mm QFN package. The package is molded in such a way that the lead frame is exposed at the bottom surface of the package.

Direct soldering of the exposed pad to a copper land provides an efficient thermal path. In multilayer board designs, a matrix of 6x6 vias thermally connects the exposed pad to the copper planes.

Requirements

PCB design should consider the exposed pad of PD69104B. This pad is used for thermal cooling of the package. Basically, PCB should be designed as shown in Figure 16 - Figure 19.

In these figures the PD69104B pad is soldered to a dedicated area on the PCB. This contact area is composed of a 48-vias array, each penetrating and thermally connecting to large ground areas in the PCB at various planes, providing efficient heat dissipation.

To ensure optimum thermal transfer through thermal vias to internal planes or to reverse side of PCB, vias system **should not be used** as in web construction techniques. Web construction for PCB vias is a standard technique used to facilitate soldering, by designing via to achieve a high thermal resistance. This is not desirable for heat dissipation from PD69104B package. It is recommended that vias used under the PD69104B package will be internally connected to the planes, using continuous connection surrounding the whole diameter.

Thermal Pad Design

PD69104B's exposed pad is a metal substrate on the bottom of the package. The attachment process for the exposed pad package is equivalent to standard surface mount packages.

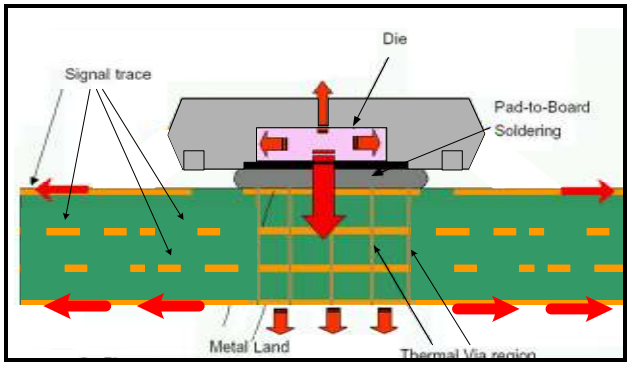

Figure 15: Heat Dissipation in PC

See Figure 16 and Figure 17 (CS & PS) for a design layout of the recommended contact pad.

For proper heat dissipation, the following footprint / layout guidelines must be followed:

- All thermal vias are to be connected to the AGND area under the PD69104B.
- Via diameter should be approximately 0.3mm with one ounce copper barrel plating. Solder flow into the vias from the component side can result in voids during the solder process and this must be avoided.
- If copper plating does not plug the vias, apply stencil print solder paste onto the printed circuit side. This provides sufficient solder paste, filling those vias to avoid the above mentioned voids. Figure 18 and Figure 19 show the associated, solder printing masks (CS & PS). The solder mask openings are lined-up in respect to the 6x6 thermal via array. Since large solder printing mask openings may result in poor release, the opening should be subdivided as shown in these figures.
- For a nominal package standoff of 0.1mm, a solder mask stencil thickness of 5 mils should be considered.

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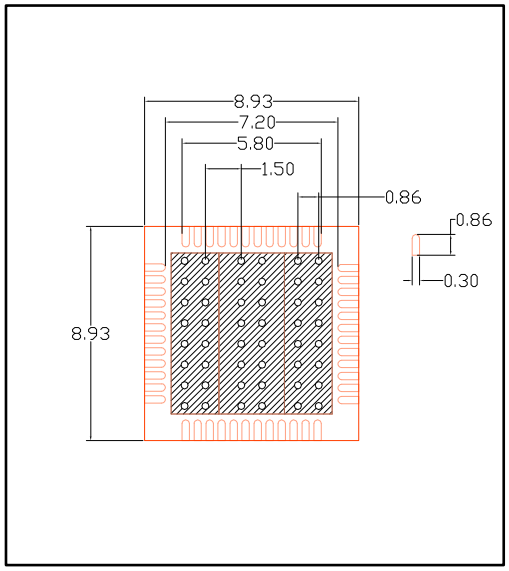

Figure 16: Thermal Pad Array Footprint (CS)

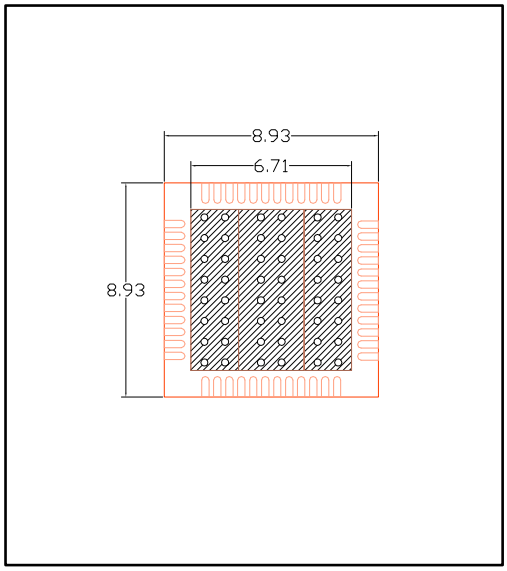

Figure 18: Solder Printing Mask (CS)

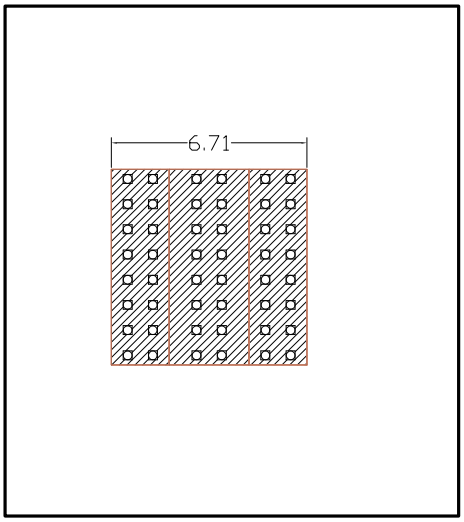

Figure 17: Thermal Pad Array Footprint (PS)

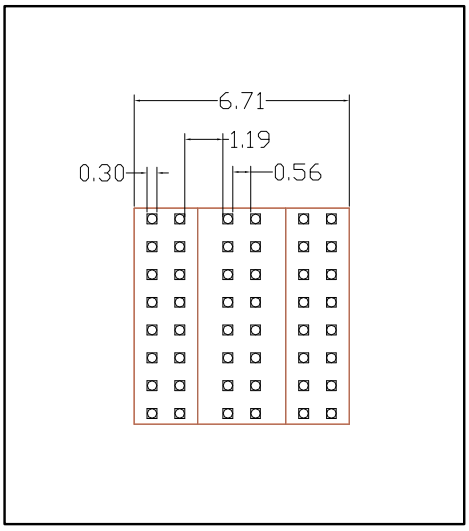

Figure 19: Solder Printing Mask (PS)

All sizes above are marked in millimeters.

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Revision History

Revision Level / Date	Para. Affected	Description
0.1/18 DEC 2011		Initial release
0.2/29 DEC 2012		General updates
0.3/30 JAN 2012		General updates
0.4/30 JAN 2012		General updates
0.5 / 24 March 2013	Figure 14	trace resistance update from 12mil to 6mil

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