

Migrating from ACT2 Devices to 42MX Family FPGAs

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Purpose

This application note provides the information needed for seamless migration of a design from the ACT2 device family to the 42MX family.

Introduction

The 42MX device architecture is based on the Microsemi ACT2 family and shares the same library of basic cells and does not require a re-synthesis of the design for migration. The 42MX FPGAs use a 0.45 μm triple-metal CMOS process, enabling significant improvements in performance. Similar to the ACT2 devices, the 42MX FPGAs are Oxide-Nitride-Oxide (ONO), antifuse-based, single-chip solutions. The 42MX devices are 5 V compliant.

References

- [ACT2 Series FPGAs](#)
- [40MX and 42MX FPGA Families](#)
- [42MX Family Devices Power-Up Behavior](#)
- [Static Timing Analysis Using Designer's Timer](#)
- [Default Settings for Unused I/O and Clocks](#)
- [Libero IDE Design Flow](#)

Comparison

Table 1 shows the recommended migration path for architecturally compatible devices. For a given ACT2 device, the recommended 42MX device is shown in the same colored grouping. In most cases, an equivalent package is available in the 42MX family. However, there are some packages in ACT2 that do not exist for the recommended 42MX device. In such scenarios, change to a different package. If the same package is available in 42MX, logic placement and I/O assignments can be preserved by using the TCL script, which is described later in the "Migrating Using TCL Script `migrate_to_mx.tcl`" on page 4. If the same package is not available in 42MX, logic placement and I/O assignments may need to be altered from the original design (refer to "Manual Migration Procedure" section of this document). In Table 1 the packages highlighted in black have no direct compatible packages in the 42MX family. Refer to "Appendix" on page 14 for a complete list of suggested migrations.

Table 1 • Device Comparison between ACT2 and 42MX

| Devices | A1225A | A1240A | A42MX09 | A1280A | A42MX16 |
|---|--------|--------|---------------|--------|---------------|
| System Gates | 6,250 | 10,000 | 14,000 | 20,000 | 24,000 |
| Logic Modules | | | | | |
| Seq | 231 | 348 | 348 | 624 | 624 |
| Comb | 220 | 336 | 336 | 608 | 608 |
| Flip-Flops (maximum) | 382 | 568 | 568 | 998 | 998 |
| Clocks | 2 | 2 | 2 | 2 | 2 |
| User I/Os (maximum) | 83 | 104 | 104 | 140 | 140 |
| Packages (by pin counts) | | | | | |
| CPGA | 100 | 132 | 132 | 176 | 176 |
| CQFP | — | — | — | 172 | 172 |
| PLCC | 84 | 84 | 84 | 84 | 84 |
| PQFP | 100 | 144 | 100, 144, 160 | 160 | 100, 160, 208 |
| VQFP | 100 | — | 100 | — | 100 |
| TQFP | — | 176 | 176 | 176 | 176 |
| <i>Note: There is no direct migration of the following ACT2 series package: CPGA100 to the 42MX family. Contact Microsemi sales to get the required help.</i> | | | | | |

Pin-to-Pin Comparison

Power Supply Pin Comparison

The supply voltage pins of the 42MX family are fully compatible with the ACT2 devices. There are several new pins in the 42MX devices that did not exist in the ACT2 devices:

- VCCA and VCCI: In the 42MX family, the supply voltage for the array is VCCA, and the supply voltage for I/Os is VCCI. The array and I/Os are supplied by the VCC in the ACT2 family. Connect the VCC pins of the ACT2 devices to the VCCA and VCCI pins of the 42MX devices. The 42MX devices can be operated in mixed mode (different VCCA and VCCI voltage). To operate in mixed mode, connect the VCC pins of the ACT2 devices to VCCA of the 42MX device and connect VCCI of 42MX to the supported mixed mode voltage. For more information about this, see [40MX and 42MX FPGA Families](#).

- LP: Low Power Mode pin is only available in the 42MX devices. When Low Power Mode is activated by pulling the LP pin HIGH, all I/Os are tristated, all input buffers are turned off, and the core of the device is turned off. This feature is particularly useful for battery-operated systems, where battery life is a primary concern. While migrating to the 42MX devices, connect this pin to GND.
- NC: No Connection. This pin is not connected to the circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

Table 2 lists the power supply ranges for the ACT2 and 42MX devices.

Table 2 • Power Supply Ranges

| Device | VCC | VCCA | VCCI | Maximum Input Tolerance | Nominal Output Voltage |
|--------|-------|-------|-------|-------------------------|------------------------|
| ACT2 | 5.0 V | – | – | 5.5 V | 5.0 V |
| | 3.3 V | – | – | 3.6 V | 3.3 V |
| 42MX | – | 5.0 V | 5.0 V | 5.3 V | 5.0 V |
| | – | 3.3 V | 3.3 V | 3.6 V | 3.3 V |
| | – | 5.0 V | 3.3 V | 5.3 V | 3.3 V |

I/O Comparison

All I/Os are at the same location for compatible devices that have the same package.

Special Pins Comparison

MODE, PROBE, SDI, SDO, TDI, TDO, and JTAG pins are fully compatible in terms of location, default configuration, and functionality.

Power-Up Recommendation

When powering up 42MX in the mixed-voltage mode, VCCA must be greater than or equal to VCCI throughout the power-up sequence. If VCCI exceeds VCCA during power-up, either the I/O input protection junction on the I/Os will be forward-biased or the I/Os will be at logical HIGH, resulting in ICC rising to high levels. Microsemi strongly recommends this power-up sequence to ensure the device's functionality. For the purpose of migrating to 42MX, this will not be an issue, since VCCA and VCCI will be connected to the same board VCC supply. For Transient current requirement during power-up, For more information about this, see [40MX and 42MX FPGA Families](#).

Configuring Unused I/Os

By default, unused I/Os in the ACT2 and 42MX devices are configured as low drivers by the Microsemi Designer software, as shown in [Figure 1](#) below. Unused I/Os should be terminated to GND or left floating. Do not drive an unused I/O to any value other than GND.

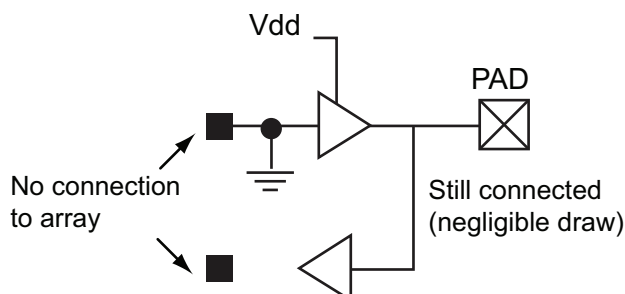


Figure 1 • Configuration for Unused I/Os in ACT2 and 42MX

Design Migration Procedure

The ACT2 and 42MX families are fully supported by the Microsemi Libero® Integrated Design Environment (IDE) and Microsemi Designer FPGA development software. This section provides instructions for using the Microsemi Libero IDE/Designer tool suite to migrate the ACT2 design to the 42MX family. Design files, such as ADB or ADL, EDN, and PIN file, are required to complete the process. An independent script is provided to migrate automatically to the 42MX ADB file without manual intervention. This script resolves several issues that need to be carefully handled in the manual procedure, such as timing constraints, compatible packages, operating conditions, and others. Microsemi strongly recommends using the script flow as the primary method of design migration to the 42MX family.

Migrating Using TCL Script `migrate_to_mx.tcl`

Download the `migrate_to_mx.tcl` script file from:

http://www.microsemi.com/soc/download/rsc/?f=migrate_to_mx_1_12

This script automatically finds the compatible die and package in the 42MX family. If the ACT2 package does not have a compatible 42MX pin-to-pin package, the script tries to migrate the ACT2 package to the largest 42MX package of the same type. The only ACT2 package that does not have a compatible 42MX pin-to-pin package is A1225A-PG100. When this script is run, it converts the design to package PG132 (the closest package of PG type) of A42MX09 device.

Running TCL in Batch Mode

File(s) required: Original.adb and migration tcl

Usage:

```
<command prompt>><path to Designer software installation "bin" directory>/Designer  
script:<path to tcl script file>/migrate_to_mx.tcl+<path to original adb file>/original.adb+<path to  
new adb file>/newname.adb logfile:<path to log file>/newname.log
```

Refer to [Figure 2](#) for an example. To specify the path to your files, use a forward slash (/).



Figure 2 • Example of TCL Script

After running this command, the new ADB, ADL, and LOG file is generated in the specified directory.

Running TCL Script in Designer GUI

File(s) required: Original.adb and migration tcl

Open the ACT2 ADB file in Designer and select **File > Execute Script**. Enter the destination where you want to save the new 42MX ADB file into **Arguments**. Click **Run** ([Figure 3](#)).

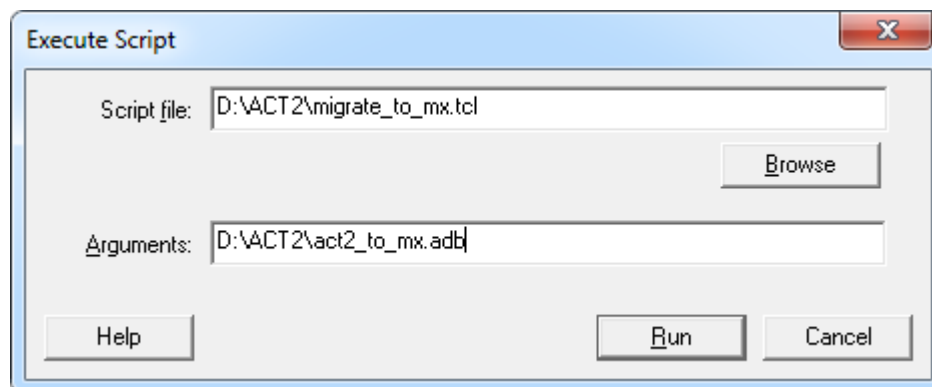


Figure 3 • Execute Script

Click **Save**, if the script succeeds with the migration procedure. Otherwise, the new ADB file will be at the original state of the design before the execution of the script.

Manual Migration Procedure

Step 1: Opening an Existing ACT2 Project in Designer

File(s) required: Original.adb

This step assumes that the ACT2 ADB file has the complete information up to Layout. If you only have the netlist ADL/EDN and other constraint source files, start from "Step 3: Creating New 42MX Project in Designer" on page 9.

Open the Designer software and select **Open Existing Design** to open the project ADB file. When the project is opened, the **Compile** and **Layout** icons should be green (Figure 4).

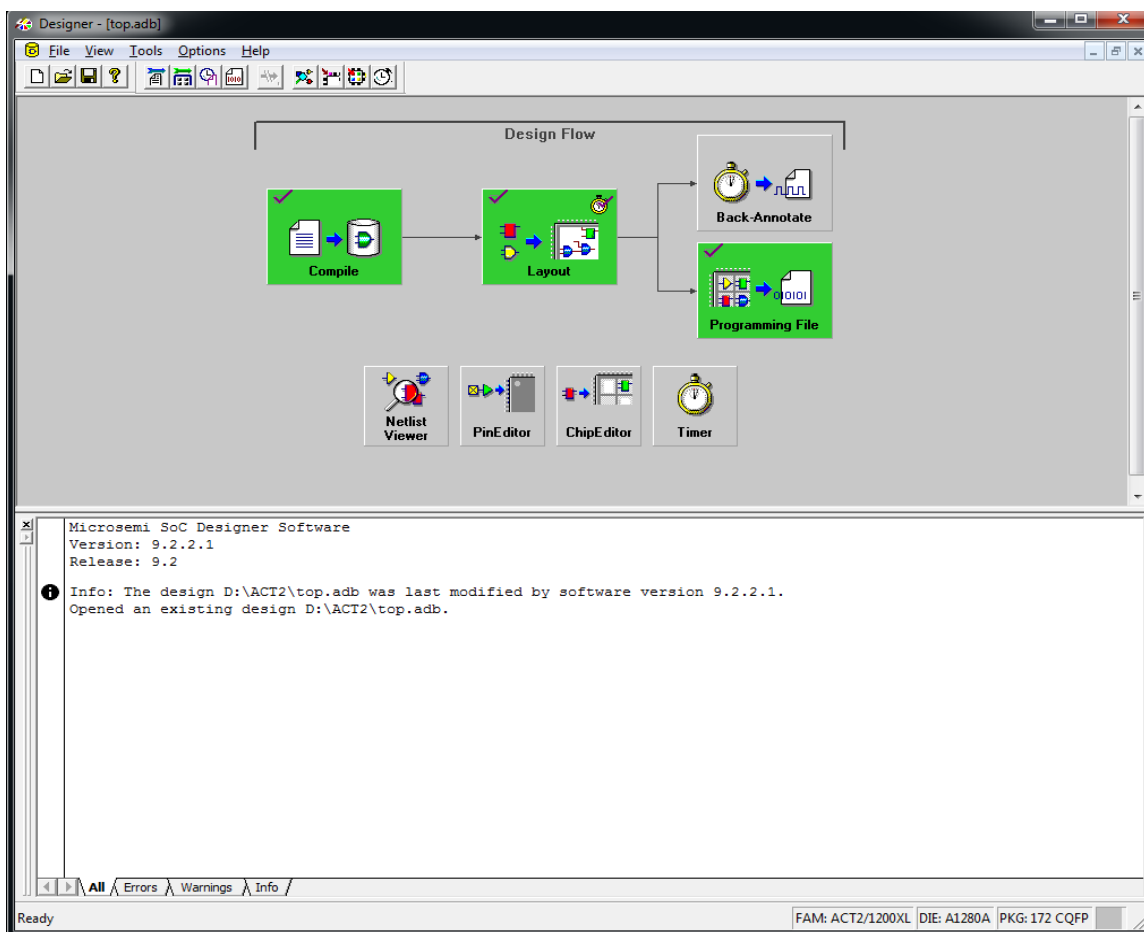


Figure 4 • Compile and Layout Icons in Designer

Step 2: Exporting Netlist and Pinout List from Designer

Select **File > Export > Netlist Files** to export the EDN netlist (Figure 5). Choose **File > Export > Constraint files** to export the pin list (*.PIN) from Designer (Figure 6).

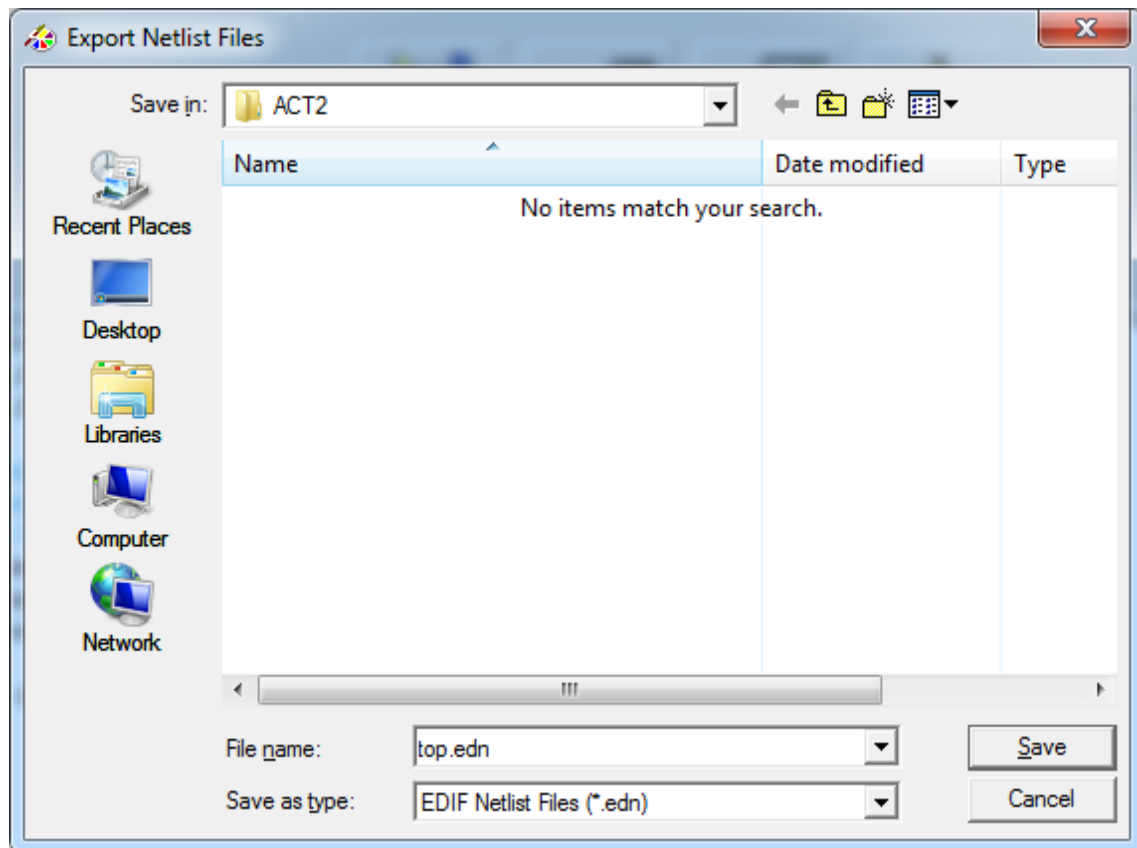
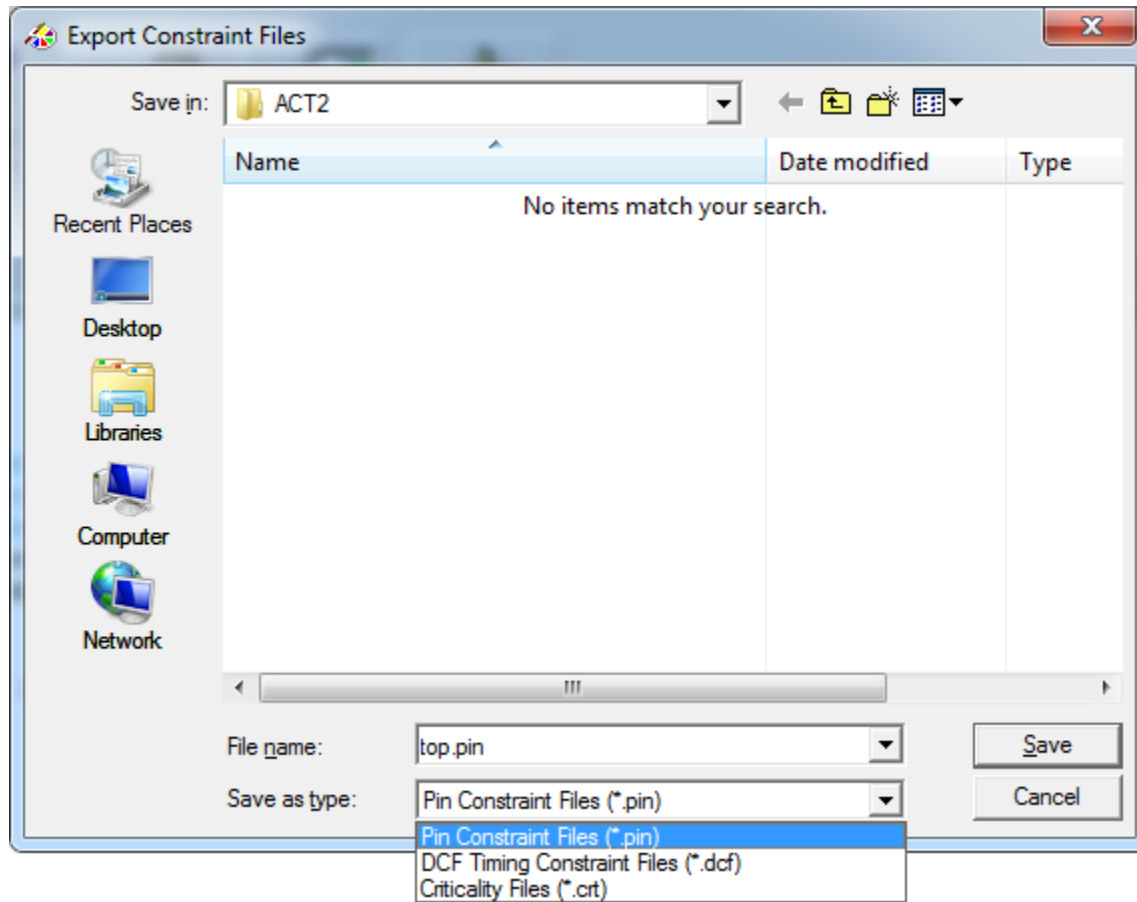


Figure 5 • Exporting Netlist Files

To preserve the timing constraints, export a DCF, CRT file from the ACT2 design (Figure 6).

**Figure 6 • Exporting Constraint Files**

Step 3: Creating New 42MX Project in Designer

In Designer, choose **File > New**. Enter the design name and select the family 42MX, as shown in [Figure 7](#).

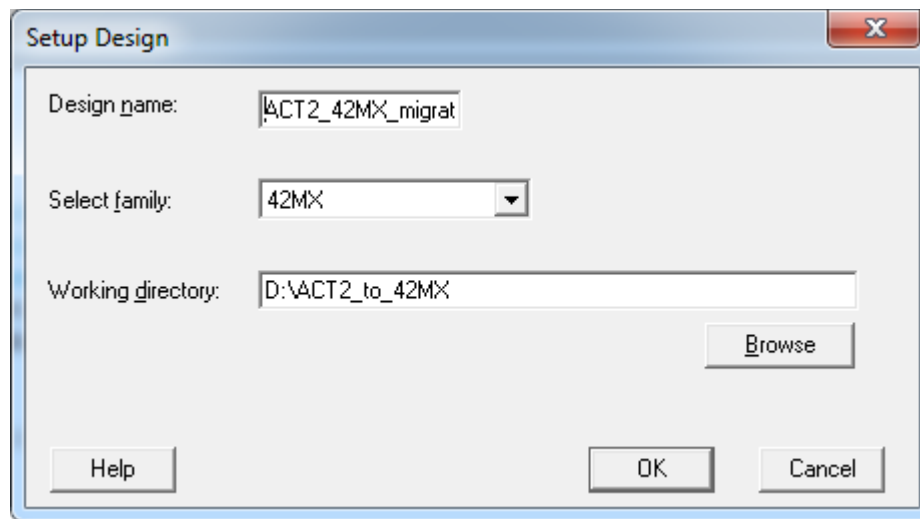


Figure 7 • Setup Design

Step 4: Importing Netlist and Constraint files into New 42MX Project

Choose **File > Import Source Files**. Add the EDN netlist and PIN files of the ACT2 project into this new 42MX project, as shown in Figure 8.

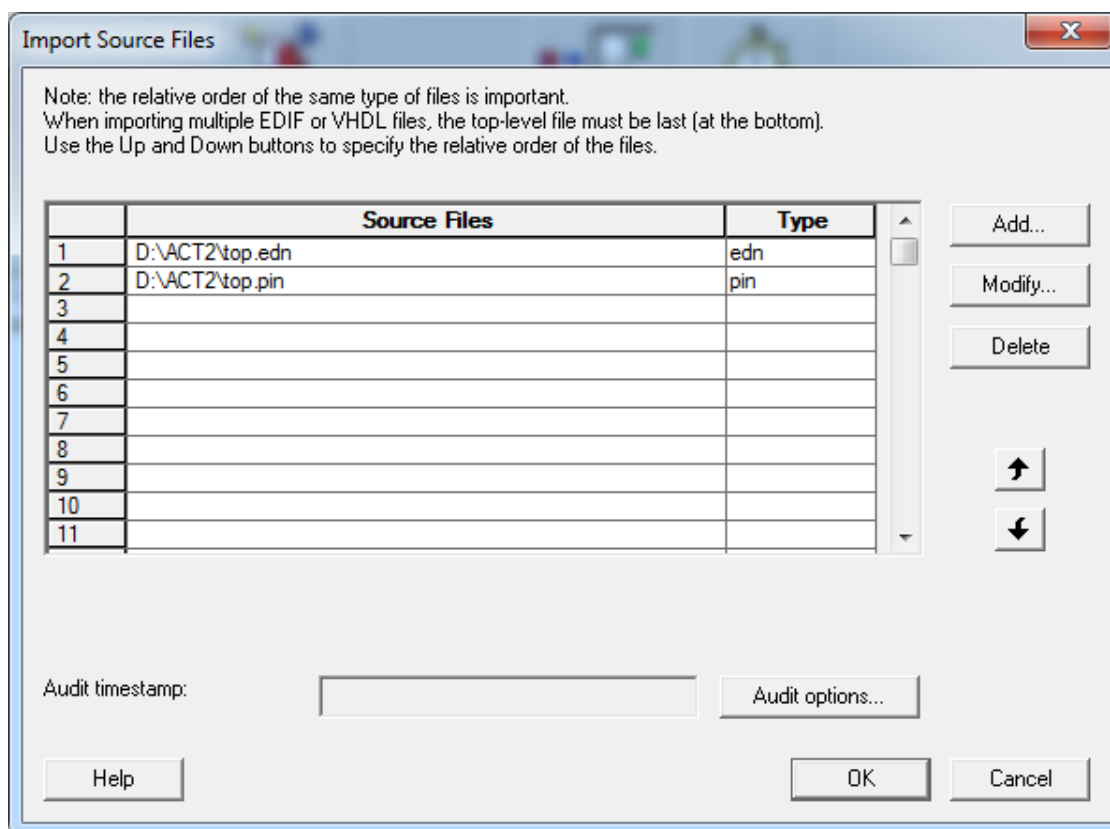


Figure 8 • Importing Source Files

Choose **File > Import Auxiliary Files**. Add the CRT and DCF files of the ACT2 project into this new 42MX project, as shown in Figure 9.

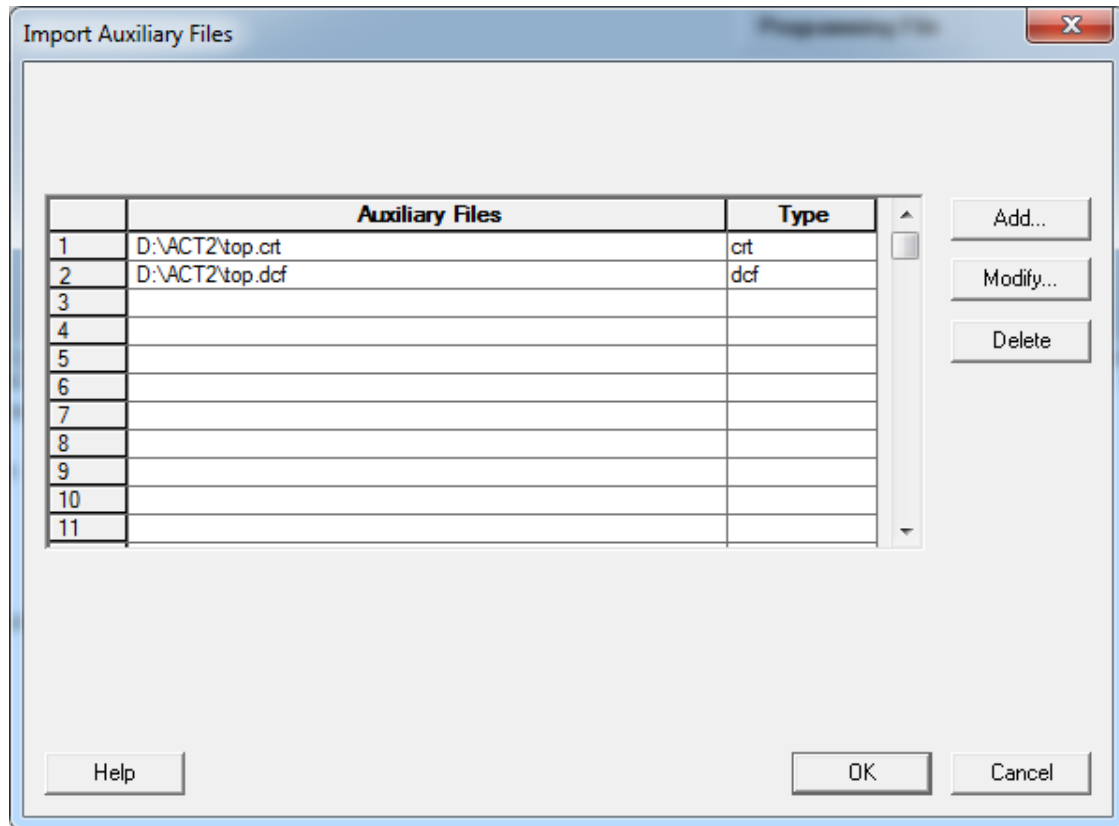


Figure 9 • Importing Auxiliary Files

Step 5: Following the Design Flow

Click the **Compile** button. **Device Selection Wizard** window opens. Choose the compatible 42MX Die/package, as shown in Figure 10.

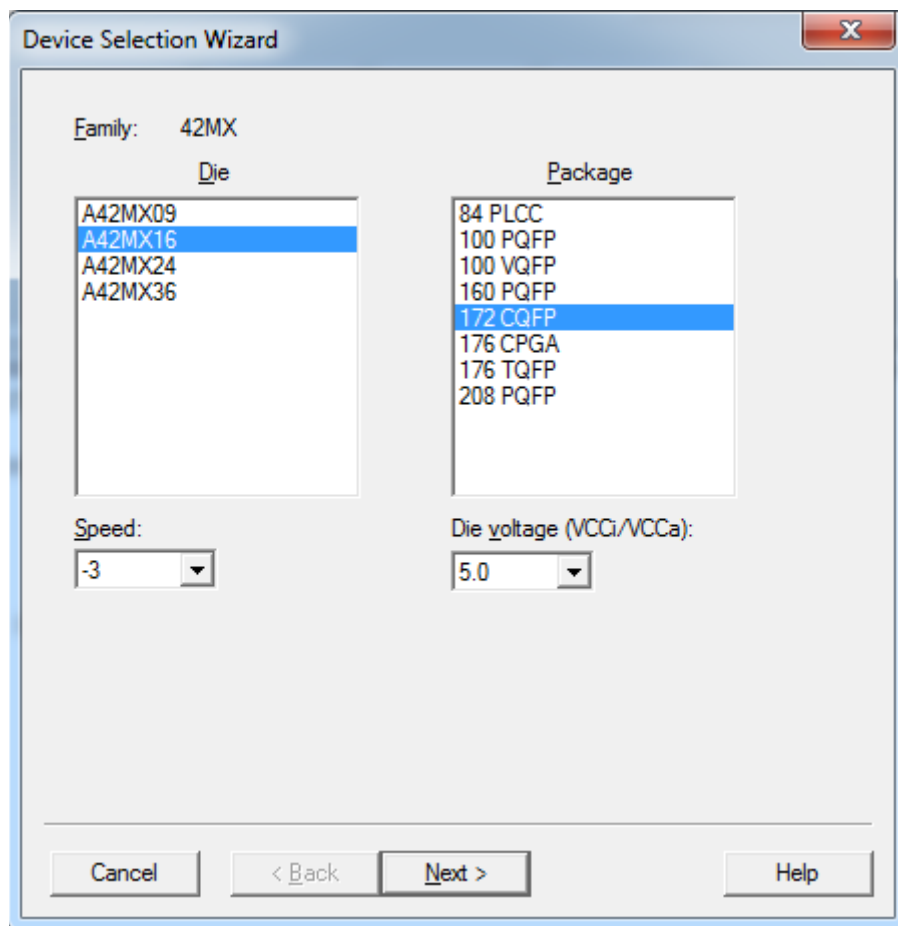


Figure 10 • Device Selection Wizard

Also, set identical operating conditions and carefully choose the device speed grade for the new 42MX design. Examples of operating conditions are VCCi/VCCa, Restrict-Probe-pins, Junction temperature, and Voltage range. From here, follow the Designer flow to complete migrating to the ACT2 design.

Timing Concerns

The 42MX family is faster than the ACT2 family. Microsemi recommends to perform a new timing analysis and pay attention to the hold time, cross clock domain paths, clock-to-out, and multi-cycle paths. Refer to the [Static Timing Analysis Using Designer's Timer](#) application note for more information on performing timing analysis using the Microsemi Timer tool. Verify the potential simultaneously switching outputs by checking whether various adjacent outputs have enough timing differences (staggered timing) to avoid negative effects. Refer to [Simultaneous Switching Noise and Signal Integrity](#) application note for details. The 42MX I/Os have a faster slew rate than the ACT2 devices. Run a board level signal integrity analysis before finalizing the board design. Refer to the [Using Schmitt Triggers for Low Slew-Rate Input](#) application note for details. The manual migration procedure does not preserve all placements, even for compatible packages. To preserve the timing constraints, export the DCF, CRT files from the ACT2 design, which is described in the "Manual Migration Procedure" section on page 6. Import this DCF, CRT file into the 42MX design after the Compile step. The [migrate_to_mx.tcl script](#) automatically preserves timing constraints as well as all placements, if possible.

Programming

Programming Software

Programming files are not compatible between the two families. Generate a new programming file (AFM) from the migrated design.

Programming Hardware

Silicon Sculptor 3 uses the same module for both families.

Refer to the Microsemi website for a list of [Silicon Sculptor modules](#).

Summary

The following steps describe how to migrate from ACT2 to 42MX:

1. Find the compatible 42MX device and package from [Table 1](#).
2. Connect the VCCA, VCCI, and NC pins to the board power supply VCC.
3. Update to the latest version of the software and follow "Design Migration Procedure" on page 4.
4. Redo the timing analysis.
5. Generate a new 42MX programming file.
6. Program 42MX using Silicon Sculpture 3 (use latest revision of the adapter module) and the latest programming software version.

Conclusion

The 42MX family shares several architectural features and the library of basic elements with the ACT2 family, and offers higher speed and special functionalities. Understanding the differences between the two families makes a seamless migration from the ACT2 family to the 42MX family possible.

Appendix

Table 3 • Migration Packages

| ACT2 Devices | Suggested Migration | ACT2 Package | Migration Package | Notes |
|--------------|---------------------|--------------|-------------------|------------------------------|
| A1225A | A42MX09 | PG100 | N/A | Need new package development |
| | | PL84 | PL84 | |
| | | PQ100 | PQ100 | |
| | | VQ100 | VQ100 | |
| A1240A | A42MX09 | PG132 | PG132 | |
| | | PL84 | PL84 | |
| | | PQ144 | PQ144 | |
| | | TQ176 | TQ176 | |
| A1280A | A42MX16 | CQ172 | CQ172 | |
| | | PG176 | PG176 | |
| | | PL84 | PL84 | |
| | | PQ160 | PQ160 | |
| | | PQ208 | PQ208 | |
| | | TQ176 | TQ176 | |

List of Changes

The following table lists critical changes that were made in each revision of the document.

| Revision* | Changes | Page |
|---|---|------|
| Revision 1 (November 2014) | Updated the document for SAR 62569. | NA |
| | Updates made to maintain the style and consistency of the document. | NA |
| Revision 0 (June 2013) | Initial Release. | NA |
| <i>Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.</i> | | |



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