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Introduction

This document provides detailed design guide to sustain extreme high voltage/current surges per few of the most popular immunity standards using Microsemi PD69108/4 IC for PoE functionality.

Overview

Surge immunity is a basic feature required within telecommunication systems in order to increase system reliability when exposed to surge event. When designing surge protection it is common to check if the required installation of the telecommunication cable is located indoor or outdoor. Surge protection is usually divided to two protection stages:

- Primary protection, deals with high energy surge and is usually located between EUT (Equipment under test) and external cable subjected to surge event, however it can be implemented at the EUT front end. Used mostly for outdoor cable installation.
- Secondary protection deals with lower surge energy and is usually located within the EUT *front* end. Used mostly for indoor cable installation.

None of the above protection stages intends to protect from direct lightning strikes event but a surge event occurs near the telecommunication line. This design guide is intended to assist the designer to implement primary protection mechanisms for protection from outdoor surge events.

Disclosure: an outdoor surge event in this document points to equipment that its telecommunication cables are located outdoor but the equipment itself located indoor. For equipment that is located totally outdoor additional regulation must be comply such as waterproof, AC input line protection, etc.

Immunity requirement's

Many standards around the world define different surge voltage level, source impedance and maximum current. This document deals with few of the most severe surge events. In most of the cases, a system sustaining the following events will sustain the following standards:

- EN 61000-4-5:2006
- GR-1089-core 2011
- ITU-T K.21 2011
- YDT 993-2006

The following tests were analyzed:

Test #01

- **Test level**

Configuration	Wave Shape	Voltage	Max Current	Test Impedance
Common mode	1.2/50µs (2Ω impedance)	6KV	1.33KA	**2 pair** – 10Ω on each one out of 4 lines **4 pair** – 20Ω on each one out of 8 lines

- **Test setup**

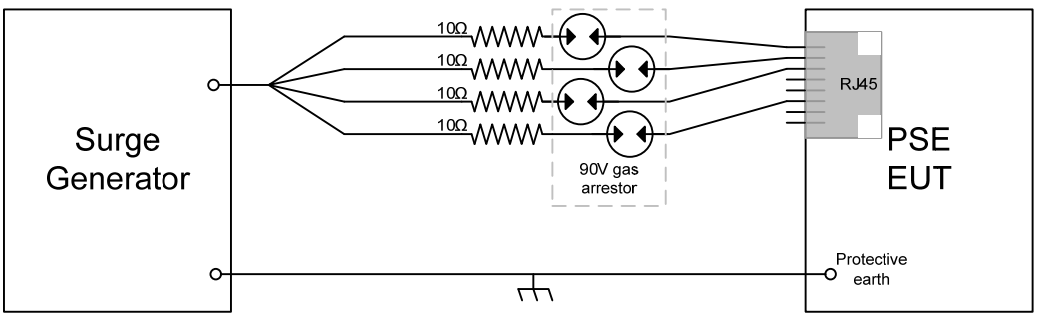

Figure 1: 2 pair test setup

Note: The 90V gas arrestor located in serial to each line enables performing the test under operative port as otherwise the port was loaded by the 10Ω resistors

- **Test procedures**
  - EUT is operating and all its ports are loaded
  - Applying positive and negative surges to a non-operative port
  - Applying positive and negative surges to an operative port
  - Verifying the port under surge is operative and all other ports are not disturbed by the surge during and after the test (only the port under test may reset)

Test #02

- **Test level**

Configuration	Wave Shape	Voltage	Max Current	Test Impedance
Common mode	10/700µs (15Ω impedance)	6KV	285A	**2 pair** – 25Ω on each one out of 4 lines **4 pair** – 25Ω on each one out of 8 lines

- **Test setup**

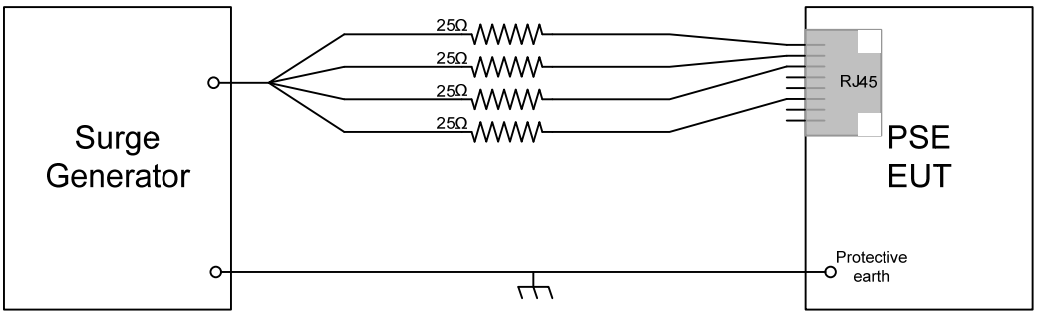

Figure 2: 2 pair test setup

- **Test procedures**
  - EUT is operating and all its ports are loaded
  - Applying positive and negative surges to a non-operative port
  - Verifying the port under surge is operative and all other ports are not disturbed by the surge during and after the test (only the port under test may reset)

Test #03

- **Test level**

Configuration	Wave Shape	Voltage	Max Current	Test Impedance
Differential mode	10/700µs (15Ω impedance)	1.5KV	285A	25Ω on one pair

- **Test setup**

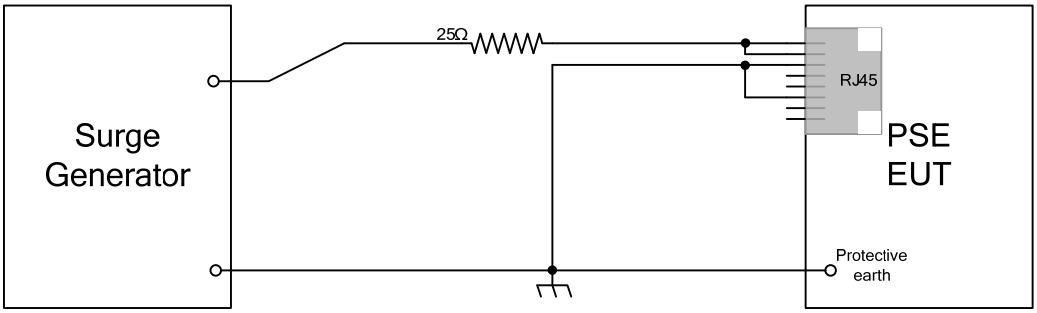

Figure 3: 2 pair test setup

- **Test procedures**
  - EUT is operating and all its ports are loaded
  - Applying positive and negative surges to a non-operative port
  - Verifying the port under surge is operative and all other ports are not disturbed by the surge during and after the test (only the port under test may reset)

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Surge protection circuit design

The following circuit complies the above tests.

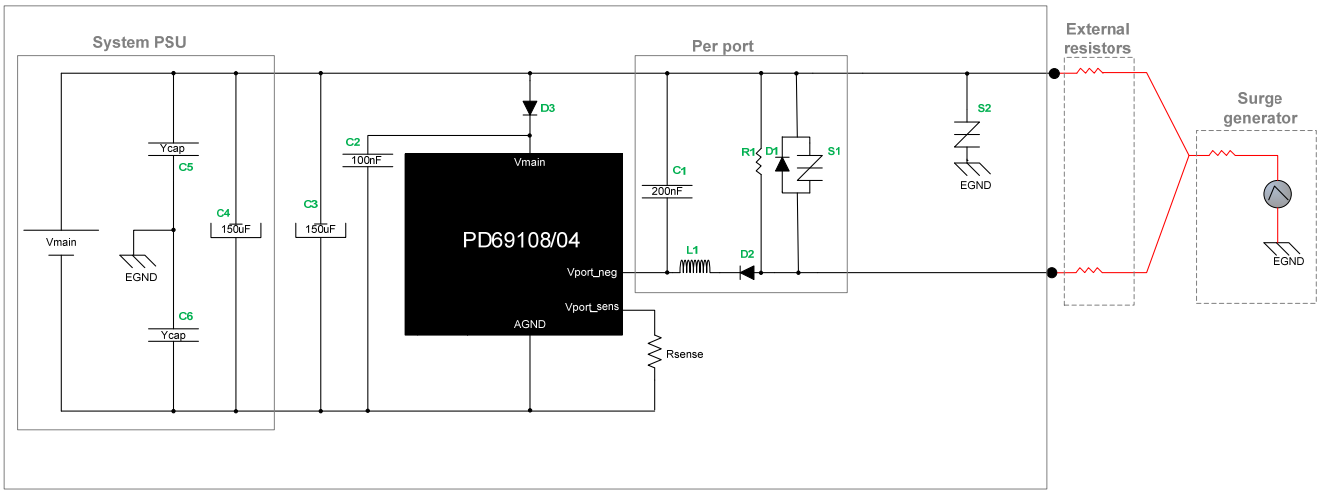

Figure 4: Common mode positive surge current path

Surge Protection components per 8 port IC

Qty	Reference	Description	PCB Foot Print	Manufacturer		Remarks
				Brand	Part Number	
2	D2, D3	Diode 1600V	SMA	Vishay	BYG10Y-E3	1
1	D1	Diode 1000V	SMB	Diode inc	S3MB-13-F	1, 2
1	R1	Resistor 1MOhm	1206	Samsung	RC3216F1004CS	Discharge resistor
1	L1	Bead 30m ohm	0805	Murata	BLM41PG471SN1	3
1	S1	Sidactor 58V 800A (8/20us)	DO-214	Little fuse	P0640SDLRP	1
1	S2	Sidactor 275V 800A (8/20us)	DO-214	Little fuse	P3100SDLRP	1
1	C1	Capacitor 200nF/100V	1206	TDK	C3216X7R2A224K	1

Remarks:

1. Can be replaced by any equivalents part
2. This diode should sustain forward current of 800A@1.2/50µs
3. The necessity of this bead depends on the PCB layout and noise coupling result from the high currents of test #01. It is a good design practice to prepare a provision for this bead and assemble it according to test results.

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Detailed circuit description

When designing application immunity to surge event there are two concepts to consider:

- Designing isolation mechanism that will prevent from the surge to breakthrough to the chassis by keeping clearance distance between the PoE circuitry and chassis. This kind of protection is common for low voltage surge protection of up to 2KV.
- Designing a low impedance current path to chassis and keep the high currents away from the protected circuitry. This kind of protection is suitable for low and high voltage surge protection.

In this case, a low impedance current path is leading the currents from the surge source to the chassis and keeps it away from the protected circuitry.
The following drawings show the expected current path for each surge event.

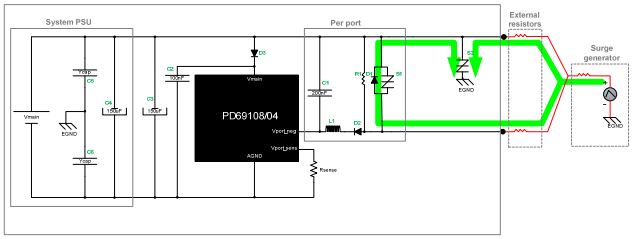

Figure 5: Positive common surge

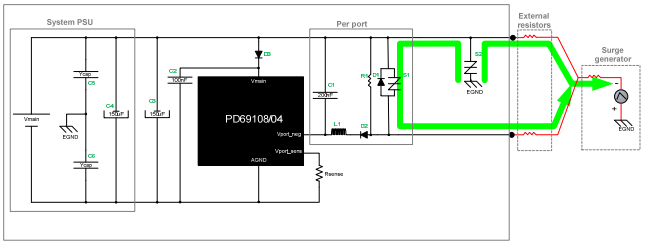

Figure 6: Negative common surge

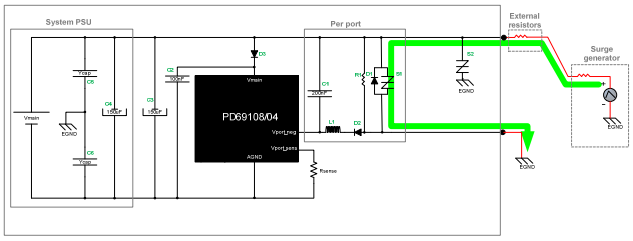

Figure 7: Positive differential surge

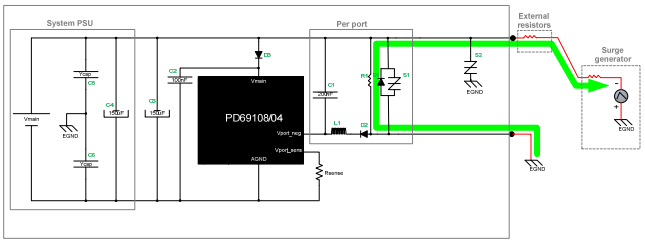

Figure 8: Negative differential surge

As can be noted, the high current path goes through the port diode (D1), port sidactor (S1), and system sidactor S2. Since maximum surge current is 1.33KA (test#01) two system sidactors (S2) in parallel should be enough to handle current for all ports. This is why S2 is not part of the port front end components. However, due to this high current, S2 injects noise that may interfere to system normal operation. It is good design practice to make PCB provision of two S2 per PoE IC (per 8 ports) and to determine how many should be assembled during testing in order to spread the current and reduce generated noise.

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Layout considerations

In order to lead the high current in efficient way and minimize noise radiation, a special care should be taken on PCB layout, following some recommendations for a proper layout (with respect to surge immunity). Any other layout recommendation relating to PoE should be implemented.

- Keep chassis trace close to RJ45 gang and do not penetrate to PoE environment.
- Chassis trace of 10mm thick should be enough for surge current.
- Make sure chassis trace/plane is well connected to the box screw and that the screw is located close to the RJ45 gang.
- Keep 80mil creepage for each component connecting between chassis and PoE circuitry.
- Do not layout PoE traces in parallel to chassis but orthogonal in order to minimize noise coupling.
- If the layout consists of more than 4 layers, use internal layers for PoE routing and external layers for plans (V_{main} and GND) in order to have better noise immunity.
- Locate S2 (see Figure 4) near RJ45 gang connected between chassis and V_{main} plane. If vias are needed, use thick vias in order to support the high surge currents. Spread these protection devices along the board (2 devises per 8 ports) and determine the final assembly during surge tests.
- Spread the system electrolytic capacitance along the board connected between analog GND and V_{main}. Use at lease 4x47µF per system in order to keep V_{main} overshoot low during the surge.
- Keep S1+D1 (See Figure 4) as close as possible to RJ45 gang and keep PoE IC away from it (30mm should be sufficient).
- Place L1, C1, and D2 as close as possible to PoE IC. (Determine of using L1 during testing. If not needed, use a short resistor instead)

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 21-April-2013		Initial Release

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