Libero SoC v11.1 Release Notes

Libero SoC v11.1 is the premier release supporting IGLOO2 FPGAs.

IGLOO2 FPGAs address the needs of today's mainstream FPGA markets by providing a LUT based fabric, 5G transceivers, high speed GPIO, block RAM and DSP blocks in a differentiated, cost- and power-optimized architecture. The new IGLOO2 architecture offers up to five times more logic density and three times more fabric performance than the previous generation IGLOO family.

Visit the IGLOO2 documentation page to obtain the Datasheet and Silicon User's Guides.

Also included in this release are the larger two members of the SmartFusion2 family, M2S100(T)(S)(TS) and M2S150(T)(S)(TS) devices. These devices are the first of 3 devices in the SmartFusion2 family to support best-in-class design security based on Cryptographic Research Incorporated (CRI) DPA resistant technology with integrated security accelerators and Intrinsic ID's physically unclonable function (PUF) technology in a non-volatile device. This enables root-of-trust applications with key management and data security processing with the industry's best design protection.

For more information on leveraging these features in your design visit the SmartFusion2 documentation page.

All SmartFusion2 designs created using Libero SoC v11.0 must be updated using Libero SoC v11.1 before programming production silicon. See **Updating your SmartFusion2 Design** below for details.

What's New in this Release

Supported Families

IGLOO2
SmartFusion2
SmartFusion
Fusion
ProASIC3
ProASIC3E
ProASIC3L
IGLOO
IGLOOe
IGLOO+

IGLOO2 Device Support

Die	Package	Speed Grade	Temp Ranges	Included with Free Gold License	Programming
M2GL150 & M2GL150T	1152 FC	STD	COM, Custom	No	Disabled
		-1	COM, IND, Custom		
M2GL150TS & M2GL150S		-1	IND, Custom		
M2GL100 & M2GL100T		STD	COM, Custom		
		-1	COM, IND, Custom		
M2GL100TS & M2GL100S		-1	IND, Custom		
M2GL050 & M2GL050T	400 VF, 484 FBGA, 896 FBGA	STD	COM, Custom	Yes	**Enabled**
		-1	COM, IND, Custom		
M2GL050TS & M2GL050S		-1	IND, Custom	No	
M2GL025 & M2GL025T	400 VF, 484 FBGA	STD	COM, Custom	Yes	Disabled
		-1	COM, IND, Custom		
M2GL025TS & M2GL025S		-1	IND, Custom	No	
M2GL010 & M2GL010T		STD	COM, Custom	Yes	Disabled
		-1	COM, IND, Custom		
M2GL010TS & M2GL010S		-1	IND, Custom	No	
M2GL005	484 FBGA	STD	COM, Custom	Yes	Disabled
		-1	COM, IND, Custom		
M2GL005S		-1	IND, Custom	No	

SmartFusion2

Design Update Required

All SmartFusion2 designs created using Libero SoC v11.0 must be updated using Libero SoC v11.1 before programming production silicon.

All SmartFusion2 designs created using Libero SoC v11.0 will be invalidated when opened in Libero SoC v11.1. For details see Updating your SmartFusion2 v11.0 Design below.

M2S005 designs started using the Fully Bonded package must be moved to the 484 FBGA package. The Fully Bonded package will be removed in the next release.

New SmartFusion2 Silicon Devices

Die	Package	Speed Grade	Temp Ranges	Included with Free Gold License	Programming	Part Marking
M2S150 & M2S150T	1152 FC	STD	COM, Custom	No	Disabled	Not Yet Available
		-1	COM, IND, Custom			
M2S150TS & M2S150S		-1	IND, Custom			
M2S100 & M2S100T		STD	COM, Custom			
		-1	COM, IND, Custom			
M2S100TS & M2S100S		-1	IND, Custom			
M2S050 & M2S050T	400 VF	STD	COM, Custom	Yes	**Enabled**	M2S050 PP or M2S050
		-1	COM, IND, Custom			
M2S050TS & M2S050S		-1	IND, Custom	No		
M2S025 & M2S025T		STD	COM, Custom	Yes	Disabled	Not Yet Available
		-1	COM, IND, Custom			
M2S025TS & M2S025S		-1	IND, Custom	No		
M2S010 & M2S010T		STD	COM, Custom	Yes	**Enabled**	M2S010
		-1	COM, IND, Custom			
M2S010TS & M2S010S		-1	IND, Custom	No		
M2S005	484 FBGA	STD	COM, Custom	Yes	Disabled	Not Yet Available
		-1	COM, IND, Custom			
M2S005S		-1	IND, Custom	No		

Requirements and Limitations Specific to Large Devices

New Devices

SmartFusion2

M2S150, M2S150T, M2S150S, M2S150TS
M2S100, M2S100T, M2S100S, M2S100TS

IGLOO2

M2GL150, M2GL150T, M2GL150S, M2GL150TS
M2GL100, M2GL100T, M2GL100S, M2GL100TS

Minimum Requirements

Libero Platinum License

Contact your regional Microsemi Sales Contact to purchase a Libero Platinum product.

64-bit Operating System with 6 GB RAM (8 GB RAM is recommended)

Windows XP, Windows 7, Linux RHEL 5, Linux RHEL 6

Updating your SmartFusion2 Design

All SmartFusion2 designs created using Libero SoC v11.0 must be updated using Libero SoC v11.1 before programming production silicon.

Several software changes implemented in Libero SoC v11.1 require you to update your SmartFusion2 design.

- For details about specific issues see: Errata Sheet for SmartFusion2 Devices.
- Default values for TX De-emphasis have been corrected.
- You must select the PLL supply voltage globally; all your PLLs must operate from the same supply.

Design Invalidation

All SmartFusion2 designs created using Libero SoC v11.0 will be invalidated when opened in Libero SoC v11.1.

1. When the v11.0 project file opens in v11.1, the Convert Project dialog box displays with an option to back-up your existing design. Check the box to Create a backup of your original project.
2. Click OK. Your design will be invalidated.
3. Follow the instructions in the tools to update your design using the latest cores.
    - Download all new cores available. Select **View > Windows > Catalog** and click **Download them now**.
    - For SmartDesign, update all instantiated components and cores to the latest versions available in the Libero Catalog.
    - Do not open System Builder components as a SmartDesign. Double-click to open the System Builder UI, proceed through all the pages and re-generate. There is no notion of replace for System Builder cores.
    - After all component and core instances are updated to the latest versions, check the configuration of each core before generating the design.
    - Open the Design Firmware window and download all the latest Firmware. Select the new version of each Firmware core and the **Download Required** dialog box appears. Click **Yes** to download the Firmware core.

    Pay particular attention to the PLL message displayed after your project is updated:

    ```
    Info: Project is updated. All PLL supply voltages must be sourced from a single Supply Voltage. Use the Project Settings dialog box to verify that your global PLL Supply Voltage is set correctly.
    ```
4. Regenerate your design.
5. Check that your constraint files are properly organized and that the tool options are correct.
6. Continue through the design flow.

Reference Documents

The following reference documents support software release v11.1. Click the link for more information.

IGLOO2 Documents, SmartFusion2 Documents

IGLOO2

SmartFusion2

SoftConsole

OEM Release Notes & User Guides

Mentor Graphics ModelSim® ME

Synopsys Synplify Pro ME

Synopsys Identify ME

Synphony Model Compiler ME

Resolved Issues in the v11.1 Release

Refer to your Technical Support Hotline Case Number to determine if it has been fixed in this release. The case number and SAR are listed below.

Table 1 Resolved SARs in Libero SoC v11.1 Release

SAR	Case Number	Product	Summary
46996 47513	493642-1298148007 493642-1318150504 493642-1311141474	Microcontroller Subsystem	Eliminated SoftConsole debugger DAPReadRange failed error when ENVM DS client placeholder is used.
46964	493642-1298303954	Microcontroller Subsystem	Fixed cause of Compile error: This design has an MSS configured to use an external 32Khz RTC XTL. This device has only one XTL which is shared with the fabric and the configuration of the XTL is not matching.
45912	493642-1260871847	Project Manager	Fixed cause of Compile error: MSS Connectivity: Incorrect fanout 9 for pin
44142	493642-1176543702	Project Manager	Fixed exported Tcl commands that did not execute.
47716	493642-1328708170	SmartTime	Fixed generate clock constraint mapping when the master clock is not known (differential i/o, gated clocks, etc.). Allows the master clock to be found later when the clock is added.
39878	493642-1202183800	SynplifyPro	Added TMR support in Synplify Pro for SmartFusion2 designs.
32302	493642-47063910 493642-1265247710	Timing	Exported SDC for the external setup/hold constraints does not match what is set in UI.
46978	493642-1110045502	Layout	Added A2F500 message. Warning: PLC503: Instance CLKINT_0/U_CLKSRC/U_GL is using the A2F500M3G fabric CCC/PLL GLA output. This resource is using the glitchless mux (NGMUX) connected to the GLA output of the fabric CCC/PLL. In order for the NGMUX to operate correctly, the signal driving this instance must be a free-running clock signal. Refer to SmartFusion Microcontroller Subsystem User Guide for more details. Verify that this signal is a continuous clock signal.

Known Limitations, Issues and Workarounds

Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines the InstallShield Wizard displays a message stating "The installation of Microsoft Visual C++ 2005 SP1 Redistributable Package (x86) appears to have failed. Do you want to continue the installation?" Select **Yes** and the installation will complete successfully.

SmartFusion2 and IGLOO2

IBIS models cannot be generated within Libero SoC. Please download them from our web site.

Block Design will be supported in a future release.

SECDED for the DDR Controllers will be supported in a future release.

SAR 46571 - M2S050 has only one Oscillator

When you instantiate the Oscillator in your design and also use MSS RTC, the Clock Source of the RTC must match the clock source used in the Oscillator. For example, configuring the RTC with Clock Source set to 32 KHz RTC Crystal Oscillator while the Oscillator block is configured with the External Main Crystal Oscillator set to 5 MHz is invalid. The frequencies must match.

Requirements and Limitations Specific to Large Devices

SmartFusion2 - M2S150, M2S150T, M2S150S, M2S150TS and M2S100, M2S100T, M2S100S, M2S100TS

IGLOO2 - M2GL150, M2GL150T, M2GL150S, M2GL150TS and M2GL100, M2GL100T, M2GL100S, M2GL100TS

Minimum Requirements

Libero Platinum License - Contact your regional Microsemi Sales Contact to purchase a Libero Platinum product.

64-bit Operating System with 6 GB RAM (8 GB RAM is recommended) - Windows XP, Windows 7, Linux RHEL 5, Linux RHEL 6

Libero

SAR 41668 – SW Update Check window opens in full screen; cannot see buttons.

Workaround: Double-click in the header section of the window and it will redisplay correctly.

SAR 47395 – Automatic I/O register combining for SmartFusion2 and IGLOO2 will be added in a future release.

SAR 41619 - IGLOO+ hot-swappable option is not displayed correctly in the GUI.

Hot-swappable is always ON for IGLOO+ and cannot be changed. The GUI allows you to check/uncheck this feature, but it is ignored by the tools. These I/Os are always hot swappable.

SAR 43772 - Linux: The SmartFusion2 configurators for DDR and FICs are missing the diagram describing the details of the block.

This issue will be fixed in a future release.

SAR 42170 - MVN Cross probing is not supported for Path List and Expanded Path View of the Min and Max Analysis windows.

This issue will be fixed in a future release.

SAR 42954 - Not all remote cores are visible in the Catalog panel after switching to a new vault, unless you reload the Catalog.

Workaround: Reload the Catalog after switching to a new vault. Select the **Settings** icon in **Catalog** and choose **Reload Catalog**.

SAR 46334 –Floorplanning PDC file names (*_fp.pdc) may not be in alphabetical order.

Workaround: Make sure the latest placement assignment changes are in the FP PDC file with a name last in the alphabetical ascending order with respect to other FP PDC files.

SAR 46161 - The post-synthesis EDN file will not appear in the design hierarchy until the project is closed and reopened.

SAR 46814 - The Placer ignores timing paths that go through a BIBUF (bidirectional I/O) if the path includes clock-to-input or clock-to-output constraints.

The Placer will not produce timing-optimized layouts that involve such paths. This issue is most likely to affect SmartFusion2 or IGLOO2 designs employing Single Data Rate (SDR)-style use model.

Workaround: Use Max Delay constraints for these paths. Create a Max Delay constraint which ends at the 'D' input of the BIBUF cell for output constraints, or that start from the 'Y' output of the BIBUF cell for input constraints.

SmartTime

SAR 34365 - Asynchronous Register paths are not displayed in timing analysis view.

This issue will be fixed in a future release.

SAR 43095 - In the Domain Browser of the Analysis window, Edit Clock for a Generated Clock does not open the Edit Clock dialog box.

Workaround: Open the Constraint Editor tool to edit the generated clock constraint.

SAR 45419 - Linux: SmartTime is unable to launch the web browser to display Help.

Workaround: Launch Help from Project Manager.

SAR 43767 – Maximize window button is missing from the Title bar.

Workaround: Double-click the title bar to maximize the window.

SAR 43726 - The exported Tcl file does not include commands to organize SDC files.

Workaround: Requires editing the exported TCL file carefully. This issue will be fixed in a future release.

SAR 46845 - The setup analysis fails to use the clock source latency constraint for ProASIC3 and IGLOO families.

Clock source latencies set on clock source are being ignored.

Workaround: Specify the clock latency on the "clock name" instead of on the "clock source".

SAR 47963 - Incorrect values for Input and Output Delay are entered automatically when external Setup and Hold values are entered in the Constraints Editor.

This is a GUI-only issue. The SDC files are generated correctly.

The problem occurs when switching the radio button between:

- External Setup/Hold and Input Delay
- Clock to Output and Output Delay

Synthesis

SAR 42808 - Warning: Unrecognized option ignored: "-_include"

When Synplify Pro is invoked through Libero and the design has RTL with “-_include” <file_name>, the following option is added in the *.prj file:

```
add_file -_include <file_name>
```

Synplify Pro issues this message:

```
Warning: Unrecognized option ignored: "-_include"
```

This warning message can be ignored. The synthesis tool will locate the file in the Libero project /hdl folder.

SAR 46982 - Synplify Pro treats the PLL as a black box

SDC constraints applied to the PLL input do not propagate forward. To actively constrain it; you must constrain both the input and the output of the PLL using the "create_clock and "create_generated_clock" constraints. More information can be found in KI70291.

SAR 46983 - False Path, Multicycle Path and Max delay constraints are not propagated to the SDC file used by Synplify Pro.

For more information about constraints consult Chapter 4, Specifying Constraints, in the Synplify Pro User Guide.

Synplify Pro Warning: Unrecognized technology/part/package in Synplify Pro

When executing synthesis using the Libero integrated flow a warning appears if the silicon family, die or package is not present in Synplify Pro. In most cases the design will automatically be mapped to an existing device and continue. If no mapping exists the flow will halt.

Missing Die

Unrecognized part [die] specified for device [silicon_family] in [design_name]:synthesis

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Package

Unrecognized package [package_name] specified for part [die] in [design_name]:synthesis

Design will be mapped to a pre-programmed default and synthesis will proceed.

Missing Silicon Family

Warning: Unrecognized technology: [silicon_family]

Unrecognized technology: [silicon_family] in [design_name]:synthesis

Synplify Pro halts.

Programming

SAR 42451 - Programming Tcl commands in the Libero flow do not work in batch mode.

The following tcl commands do not work in batch mode:

- configure_tool -name {IO_PROGRAMMING_STATE} -- Device I/O States During Programming
- configure_tool -name {PROGRAM_OPTIONS} -- Programming Features
- configure_tool -name {PROGRAMDEVICE} -- Configure Action/Procedures
- configure_tool -name {EXPORTPROGRAMMINGFILE} -- Export Programming File Options
- run_tool -name {EXPORTPROGRAMMINGFILE} -- Export Programming File

Workaround: Use the Libero GUI: Project/Excute Script

SmartFusion2 and IGLOO2 programming file generation on Linux will be available in a future release. Use Libero for Windows.

SVF for SmartFusion2 and IGLOO2 will be available in a future release.

SAR 48448 - Zeroization will be available in a future release.

SAR 45867 - STAPL player for SmartFusion2 or IGLOO2 STAPL will be available in a future release.

SAR 41069 - Add PDB loading from DDF for Libero environment

When performing chain programming within Libero with a PDB file, you may get an exit 6 idcode failure.

Workaround: Use a STAPL file or use the standalone FlashPro tool for chain programming.

SAR 47535 - Update eNVM Memory Content should not open multiple dialogs.

If you double-click Update eNVM Memory Content (in the Design Flow window) several times then you can open multiple dialog boxes.

Workaround: Close all but one of the open Update eNVM Memory Content dialog boxes.

SAR 43530 - SmartFusion2 M2S050T_ES must be enabled after other devices in a chain.

When you have a chain with the M2S050T_ES enabled before other devices, you cannot enable programming for the non-SmartFusion2 devices.

Workaround:

1. Disable the M2S050T_ES device for programming.
2. Enable each non-SmartFusion2 device for programming.
3. Enable the M2S050T_ES device for programming and proceed.

SmartDebug

SmartDebug Tcl commands in the Libero flow will be supported in a future release.

SmartFusion2 and IGLOO2 devices will read invalid memory content if the MSS is held in the reset state or M3 is executing invalid microcode programmed into the FlashMemory

Workaround: Program a valid design. Confirm that the MSS is not in the reset state.

Debug file generation for M2S010 devices will be supported in the next release.

System Requirements

Refer to System Requirements on the web for more information regarding operating system support and minimum system requirements.

Disk Space Required:

Libero SoC v11.1 with all tools installed requires 3.5 GB

Libero SoC v11.1 stand-alone is 1.6 GB

SmartFusion2 and IGLOO2 RAM Requirements for a typical design

Die Size	Peak Memory Usage
005 & 010	2.0 GB
025	8.0 GB
050	8.0 GB
100 & 150	8.0 GB

SmartFusion2 and IGLOO2 require a 64-bit OS.

Red Hat Enterprise Linux Tips for Launching Libero – See the Libero Software Installation and Licensing Guide.

RHEL 6 64-bit Setup

You must modify the default operating system installation to run Libero on RHEL 6. System administration privileges may be required to make these modifications.

1. Libero software on Linux expects to see the libXm.so.3 package of the Open Motif Library.
   - Since Libero is a 32-bit application, please make sure to use the 32-bit Open Motif Library even if the computer is running a 64-bit Operating System.
   - One version of Open Motif that provides libXm.so.3 is Open Motif v2.2.3.
   - If you are unsure whether you have the Open Motif Library Installed, try the following commands:

     List the Open Motif libraries installed

     rpm -qa | grep -i motif

     List the files and paths associated with Open Motif libraries

     rpm -qal | grep -i motif

   - If you do not have a Motif Library Installed, download and install from

     http://motif.ics.com/motif/downloads

2. You must install the following libraries using Yum.
   - RHEL Workstation 6.3 64-bit requires only the first 4 packages.
   - RHEL Server 6.0, 6.1, 6.2 and 6.3 (64-bit) requires all 7 packages listed below.

   The commands and packages are shown in the table below.

Yum package	Fixes Error Message
yum install libXft-2.1.13-4.1.el6.i686	X Libraries not in LD_LIBRARY_PATH (libero)
yum install openmotif22-2.2.3-19.el6.i686	Missing MOTIF libs (libero)
yum install glib2-2.22.5-7.el6.i686	Missing libgthread-2.0.so.0 (libero)
yum install ncurses-libs-5.7-3.20090208.el6.i686	Missing libncurses.so.5 (modelsim)

Additional packages required for RHEL 6.0 through 6.3:

Yum package	Fixes Error Message
yum install libXrender-0.9.5-1.el6.i68	Missing libXrender.so.1
yum install fontconfig-2.8.0-3.el6.i686	Missing libfontconfig.so.1
yum install freetype-2.3.11-14.el6_3.1.i686	Missing libfreetype.so.6

3. Start the system `rpcbind` utility with the `-i` option to enable backward compatibility with earlier RPC library versions.

   Replace rpcbind with rpcbind -i in the system start-up script /etc/init.d/rpcbind

   Restart rcpbind service

```
/etc/init.d/rpcbind restart
```

Synopsys and Mentor Graphics Tools

These tools are included with the Libero SoC v11.1 installation.

Synplify Pro ME H-2013.03M-1 Release Notes

ModelSim AE 10.1c

Identify ME H-2013.03M Release Notes (Windows only)

Synphony Model Compiler ME H-2013.03M SP1 Release Notes (Windows only)

Prerequisite Software: In order to run Synphony Model Compiler ME, you must have MATLAB/Simulink by MathWorks installed with a current license. You cannot run Synphony Model Compiler ME without MATLAB/Simulink.

Download Libero SoC v11.1

Windows and Linux Version Libero SoC v11.1

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