Introduction

This application note provides detailed information and PCB design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's™ 12-channel PoE Manager, the PD69012.
Using this application note, the PCB designer is able to integrate PoE capabilities into an Ethernet switch.
The PD69012 is designed to implement all real time functions as specified in the IEEE 802.3af-2003 and IEEE802.3at-draft3.3 standard including: detection, classification and port status monitoring, as well as system level activities such as: power management and MIB support for system management. The PD69012 is designed to detect and disable disconnected ports, using both DC and AC disconnection methods, as specified in the standard.

This application note is to be used in conjunction with application note AN-174, Cat. No. 06-0054-080.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-draft3.3 standard, DTE Power via MDI
- PD69012 Data Sheet, Cat. No. 06-0069-058
- PD69000 Data Sheet, Cat. No. 06-0070-058
- Microsemi Application Note AN-174 for Designing a 48-port Enhanced PoE System (802.3af/802.3at Compliant, UART)

Approach

In order to properly integrate the PD69012 PoE Manager into a new circuit or adapt an existing one, it is essential to follow the presented guidelines. The information sets out limitations and restrictions imposed by isolation demands of the circuit, as well as circuit layout recommendations for optimal operation.

Isolation & Termination

Overview

According to the IEEE 802.3af and the IEEE802.3at-draft3.3 standard, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations.
These requirements are taken into account by PoE switch vendors, while designing the switch circuitry. However, when a PoE Manager is integrated into a switch, special design considerations must be met, due to the unique combination of Data and Power circuitries.

The following paragraphs define these requirements and provide recommendations for their implementation, so as to assist designers in meeting those requirements and in integrating the Microsemi's PoE Chip Set and the daughter boards.

Isolation

As specified in the IEEE PoE standards, 1500 Vac rms isolation is required between the switch's main board circuitry including protective and frame ground and the Media Dependent Interface (MDI). Figure 1 illustrates the overall isolation requirements.

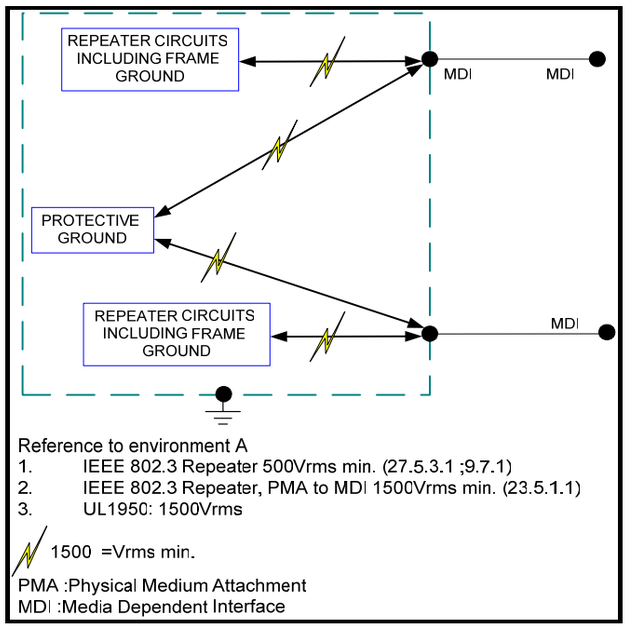

Figure 1: Isolation Requirements Scheme

Meeting Requirements

Hi-voltage Isolation

- For a switch with no PoE circuitry: isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers (see Figure 2).
- When integrating a PoE circuitry into a switch, the output power may be supplied through the central tap of the pulse transformer's secondary side (unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation, if the PoE ground or DC input is connected to the switch's circuitry/ground.

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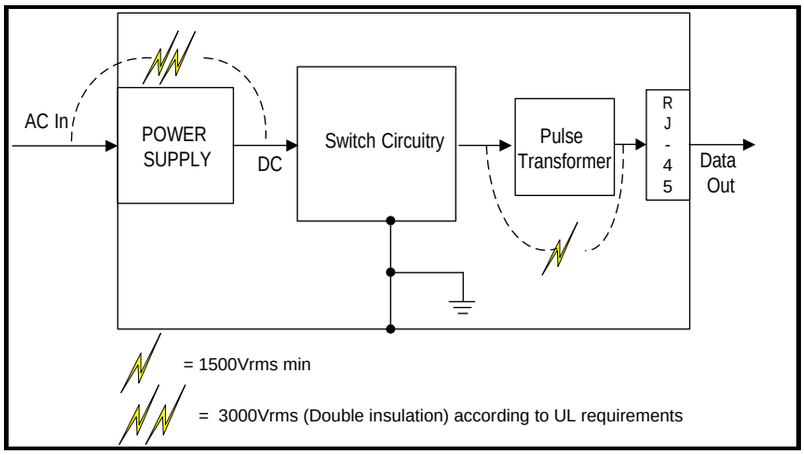

Figure 2: Standard Switch Circuitry

In order to comply with the above isolation requirements, the PoE Managers must be isolated in regards to all other switch circuitries. One of the following methods is used:

- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry (see Figure 3).
- A single DC input (separate power supplies) for both the switch and PoE circuit; additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry (see Figure 4).

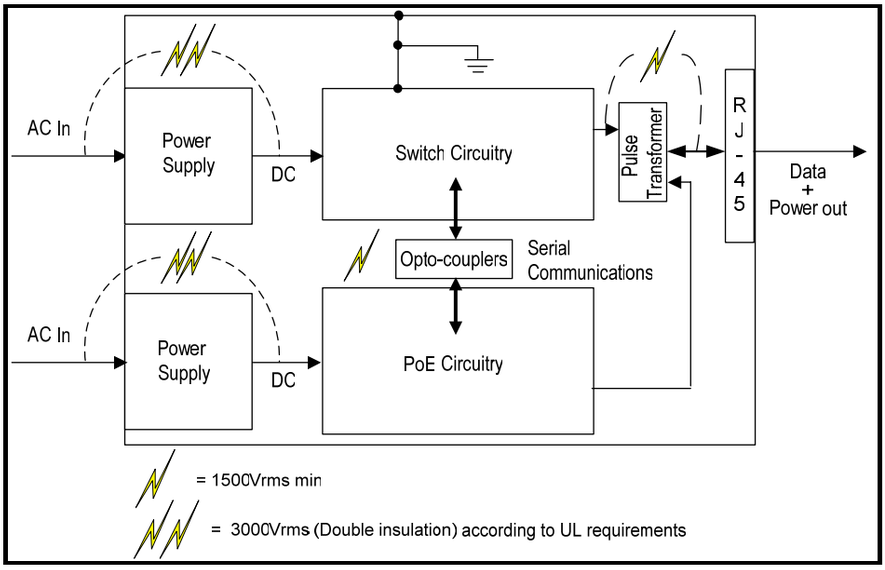

Figure 3: Switch Circuitry with Two DC Sources

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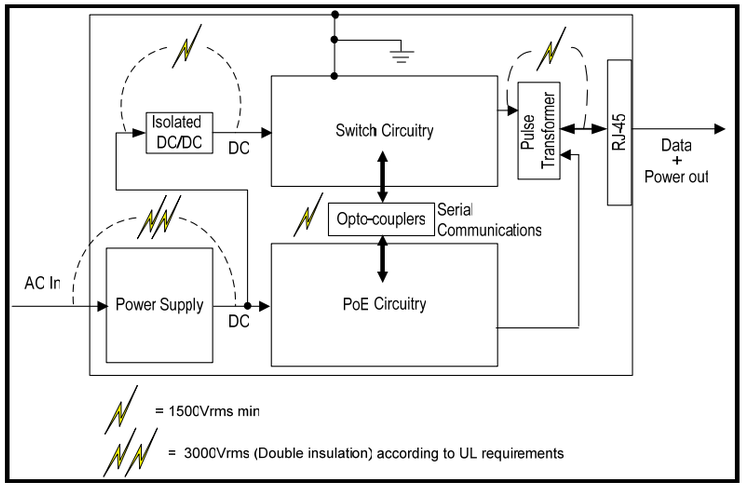

Figure 4: Switch Circuitry with a Single DC Source

In order to maintain 1500 Vrms isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended, to provide a safe margin for hi-pot requirements.

PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. In order to meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry (see Figure 5). Note that in most PoE systems, it is recommended to use 0 Ohm resistors for R1 and R2. However, certain systems may benefit from 75 Ohm resistors. It is recommended that filtering provisions are made. Note that in quite PoE systems the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes:

- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances.
- Y-capacitive/resistive network to chassis.

Since each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note For best EMI performance and in order to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs, or the spare pairs. Both methods are detailed in Figure 6 which illustrates an MDI-X (or Auto MDI-X) connection, associated with the switch.

Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 Vrms isolation between PoE voltages and frame ground (EGND). Notice that RJ-45 jack assemblies have a metal cover that almost reaches to the PCB surface.

Proper traces clearance (at least 80 mils) are to be maintained between EGND traces for the RJ-45 modular jack assembly metal covering and adjacent circuit paths and components. To prevent 1500 Vrms isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ-45 connector assemblies.

PoE technology involves voltages as high as 57VDC. Thus, plan adjacent traces for 100V operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

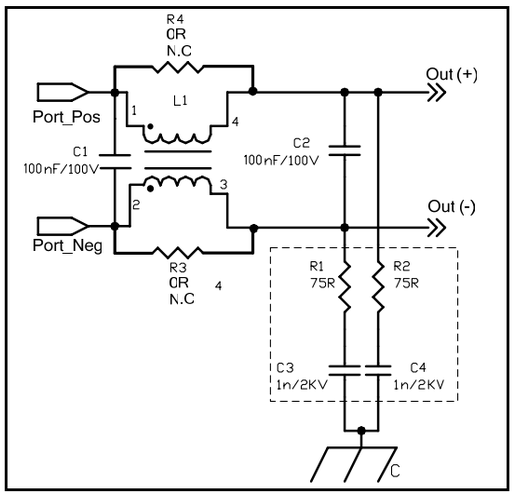

Figure 5: Recommended EMI Filter

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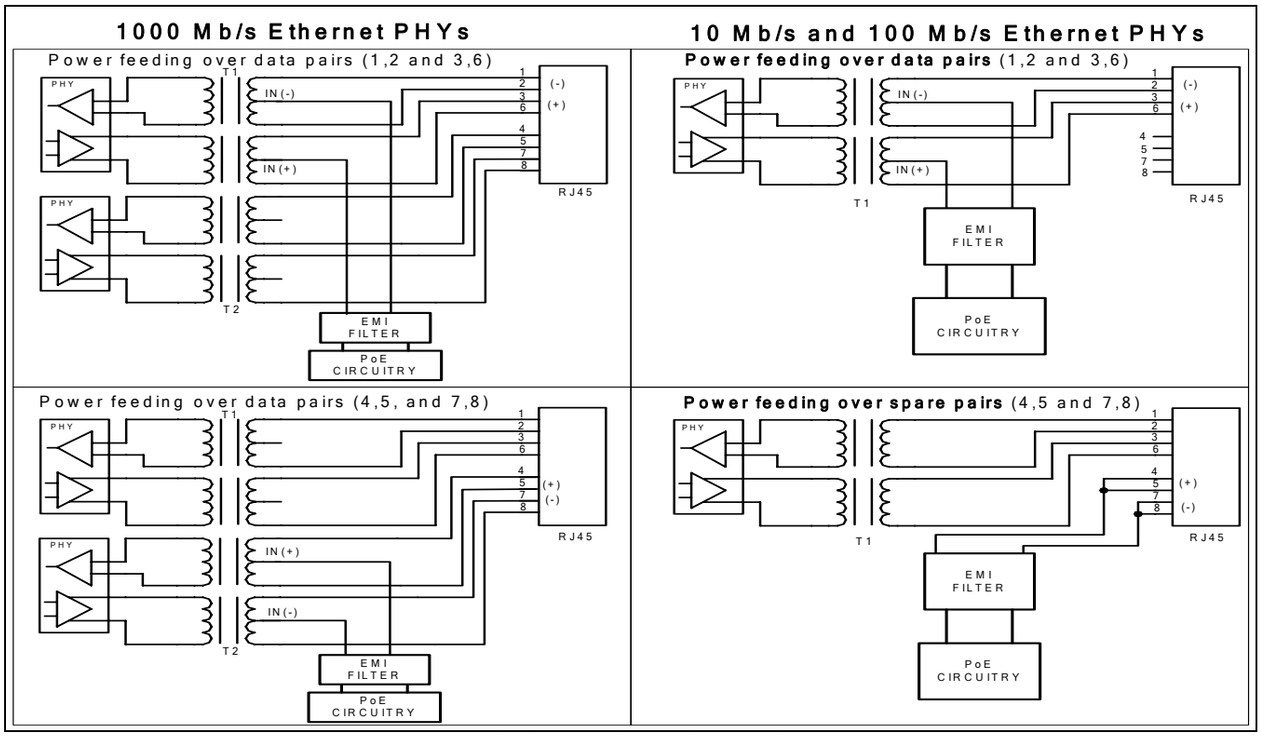

Figure 6: Output Ports Design Details

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Layout Guidelines

Microsemi's PD69012 PoE Manager is designed to simplify the integration of PoE-circuitry, based on the IEEE PoE standards into switches.

The pin-out arrangement has been configured for optimal PCB routing. Microsemi recommendations for proper PCB layout are as follow:

Figure 7 describes the various circuits and elements surrounding the PD69012 PoE Manager in a block diagram. This block diagram includes the following peripheral elements, identified by numbers:

- 3.3V Voltage source (V_{PERI}) (1)
- Line detection resistor – feeds the line detection voltages into the ports (2)
- Sense resistor for current measurement (3)
- Output capacitor – used for filtering (4)
- External power MOSFET (5)
- Protection diode against reverse polarity (6)
- Configuration pins filters (7)
- Charge pump components (8)

Note The V_{PERI} potential may include an external transistor connected to pin 48, destined to increase current drive. To prevent heat from being transferred to the PD69012, locate this transistor away from the PoE Managers.

For details on the interconnection circuitry of the PD69012, refer to the Application Notes listed in the "Applicable Documents" section.

The circuitry provided, is intended to facilitate the design of a switch when integrating a PoE capability into it.

Locating PoE Circuitry in a Switch

Placement of the PoE circuitry must be as close as possible to the switch's pulse transformers, in order to minimize the length of high current traces, as well as RFI pick-up.

The circuit can be fully integrated into the switch's PCB, or can be easily placed on top of the switch's using daughter board PoE application. Typical integration of PoE modules inside a switch is shown in Figure **8** and Figure 9

Ground & Power Planes

As the Chip Set PoE solution (PD69012 & PD69000) is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines.

Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines, illustrated in Figure 10:

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Due to thermal constraints, analog ground plane (AGND), must be the first layer after the component side (top layer). The AGND is utilized to transfer the heat generated by the PD69012 (see Thermal Pad Definition & Design paragraph)
- If separate layers are used for different grounds or power, try not to overlap the planes, to minimize noise transfer from layer to layer
- Earth ground is used to tie in the metal frame of the RJ-45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure as specified in the isolation requirements (above in this application note)
- Only a single connection point is to be used between the digital and analog grounds, in order to prevent ground loop currents. This connection is to be accomplished at the "star point" of PD69012 Slave0 as shown in Figure 10 and Figure 12
- It is recommended that the grounding layout is implemented as described in Figure 10. A number of separate grounding areas are essential in the design, in order to minimize noise effects from the heavy currents flowing to the ports. Several separate ground areas are established to concentrate sensitive circuits, apart from the main grounding surfaces
- The GND_ANALOG_CPU surface is to be extended under pins 22-31 of the PoE Controller. This grounding area is connected at one point (pin 16 of the PoE Controller) to the digital ground (DGND). Connect the analog filtering capacitors to this ground
- The digital ground (DGND) surface is to be extended under pins 41-60 of the PD69012 Managers for connection of various DGND points
- Rsense resistors for each PoE Manager are all connected to local "star point" on the analog ground (AGND). To achieve this, use four tied power via's of 12 mil diameter each (see Figure 11, Figure 12 and Figure 13)
- In addition, the Rsense resistors' "star point" connection for the PD69012 utilized as Slave0, is to be the focal interconnection point for the digital and analog grounds (see Figure 12)
- Leave spacing for ceramic 1nF bypass capacitors (Cb) (Figure 12) between the analog and digital layers near each PoE Manager. The capacitors form low impedance paths for digital driving signals
- Leave appropriate spacing (provision for) for two parallel and inversed Schottky diodes (Da, Db) (Figure 12) between the analog and digital layers near each PoE Manager. The diodes form low impedance paths for highly energized signals running between analog and digital layers and enhance circuit immunity
- The power plane for the 48V input must be designed to carry 35A continuous current, based on full 48-port capacity. Minimize DC power losses on this plane by using a wide copper land

Current Flow Through the PoE application

The port's current flow in a DC disconnect application is as follows:

1. Coming from the switch's power supply to the centertaps of the line transformer (not through the DB)
2. From the centertap of the line transformer through the switch's RJ45 to the PD side
3. The current from the PD flows through the RJ45 and through the line transformer to the DB PoE circuitry.
4. From the DB analog ground (AGND) back to the switch's power supply

Note The port's heavy current goes directly to the PD side without going through the PoE DB Managers.

Specific Component Placement

Peripheral Components

To prevent heat transfer among various components, the following gaps should be maintained:.

- Minimum gap between PD69012s should be 50mm
- Minimum gap between PD69012 to PoE controller should be 50mm
- Minimum gap between PD69012 to Q1 (for further details related to Q1, refer to Application Note AN-174 for Designing a 48-port Enhanced PoE System (802.3af/802.3at Compliant, UART), should be 30mm.
- It is recommended to leave an open gap in the ground plan to isolate the heat transfer from the two areas
- The spacing between the sense resistors and the external MOSFETs to the PD69012 should be about 15mm. It is recommended to use 'Through-Hole' resistors mounted vertically or horizontally off the board as specified in the IPC-A-610 standard. The resistors should be placed in such a way that they won't prevent airflow to the PoE Manager. Using SMD resistors requires proper airflow and leaving an open gap in the ground plan (if required) to isolate the heat from the PoE Manager
- Do not group all sense resistors and the external MOSFETs close to each other, to prevent a hot spot on the PCB, under full load conditions

PoE Controller & Peripherals

Refer to the PD69000 Data Sheet, Cat. No. 06-0070-058 for recommendations related to the PoE controller layout guidelines.

The following Guidelines are destined for the integration of the PoE Controller into a PoE circuit.

- Filtering capacitors for VDD (pin 17) and for VDDAD (pin 40) are to be located close to these pins. The filtering capacitor for the analog input of pin 30, the components connected to pin 25 (I2C_ADDR) and to pin 23 (HW_VER), are to be located close to the input pins and above the quiet analog ground 'GND_ANALOG_CPU'.
- Termination resistors (49.9 Ohms) for the digital lines (pins 1, 4, 5, 9, 10, 12-15 and 32) must be located close to the respective pins

PD69012 PoE Manager & Peripherals

- The side of the PoE Manager that includes pins 41 to 60 should face the PoE Controller. These pins function as communication and control pins for the Manager. In addition, that same side should face the digital ground
- Bypass capacitors for the PoE Manager operating voltages, are to be located close to the relevant pins. In cases where two bypass capacitors are placed on the same line, the lower value capacitor is to be located closest to the pin on the same layer and the higher value capacitor can be located at a more distant location
- Locate Vperi 0.1uF and 2.2uF filtering capacitors as close as possible to the PoE Manager using shortest traces for the DGND pin (pin 40) of the PoE Manager and for the Vperi (pin 57)

Conductor Routing

General Guidelines

Conductor (or printed lands) routing is to be performed as practiced in general layout guidelines, Specifically:

- Conductors that deliver a digital signal are to be routed above the digital ground plane
- Avoid routing analog signals above the digital Gnd
- These signals are layout sensitive: SENSE_NEG, PORT_SENSE0 through PORT_SENSE11
- Vperi transistor: Verify that a transistor case with proper heat dissipation is chosen

Specific Requirements for Clock & Sensitive Signals

Issues that require special design considerations:

- The SENSE_NEG (pin 61) is to be routed to QGND (pin 54) and a trace from QGND is to be connected to the local PoE Manager "star point" (AGND). The PD69012's AGND (pins 21, 62) must also be connected directly to the local PoE Manager "star point" by individual traces
- The 100nF bypass capacitor (item-1 in Figure 7) from Vperi to DGND must be placed as close as possible to the respective pins. Its conductors to Vperi and pin 40 should be as short as possible
- The VPORT_POS capacitor (1nF) is to be located close to the PD69012 pins.
- The IREF resistor (connects to pin 50), used for current reference, is directly connected to AGND (pin 62)

- Each PD69012's port incorporates a current sense resistor. For proper power management and control, these lines are to be laid out in such a way that measured current is not impeded by adjacent ports current flow or by excessive path resistance. To achieve this, a single common point is to be used to aggregate the current flow of all 12 ports to the analog ground (AGND) layer. This point is referred to, as the local PoE Manager "star point" (see

- Figure **11**, Figure 12 and Figure 13). It is critical to design the total layout path (traces resistance from PORT_SENSE pin to the AGND star point), for an accurate resistance value, since wrong resistance value results in current measurement error and un-reliable power management. Parasitic resistance added by the layout traces, must be planned as follow:

- In cases where 500 mohm sense resistor is used,, the parasitic resistance added should be 1mΩ to 9mΩ (at room temperature). The total resistance from each PORT_SENSE pin to the AGND star point should be 501mΩ to 508mΩ.

- In cases where 487mohm sense resistor is used the parasitic resistance added, should be 8mΩ to 20mΩ (at room temperature). The total resistance from each PORT_SENSE pin to the AGND star point should be 495mΩ to 507mΩ.

  Layout Useful Method (optional) – in order to achieve the above accuracy, when preparing the layout for the sense resistor traces. Design this path to achieve a specific parasitic resistance (as specified above). Record the trace's length and width values. Assuming that all traces have the same copper thickness, use the following rule to design the remaining traces:

  k = L1/ w1, where:

  k is a constant value

  L1 length of trace1

  w1 width of trace 1

  Plan all other traces to obtain an identical k value (i.e.: L2 / w2 = k). The conductors are to be routed so that they will merge only at the star point.

  Note The four vias connecting the "*star-point*" with the AGND plane should have a 12 mil diameter each. Avoid using plugged vias to preclude temperature rise.

- Carefully route the ESPI communication clock (SCK) line coming from the PoE Controller in such a way that it will not disturb other lines. It is recommended that two ground lines (connected to DGND) are routed alongside the clock line in order to isolate it from the rest of the lines
- The PoE Manager includes a Charge Pump circuitry. Locate related components (item 8 in Figure 7), close to the Manager, with short traces to pins 13, 14 and route Charge Pump's ground circuitry directly to the analog ground (pin 21)
- The IREF resistor (pin 50) used as a current reference (item 9 in Figure 7) is directly connected to the AGND (pin 62)
- Several analog signals are sensitive to environmental and system noise. The external components associated with these signals are to be connected to the QGND (pin 54- see Figure 7). These signals are:
  - I2CINI (pin 53) setting the I^2C address of the particular PoE Manager (item 7 in Figure 7)
  - ASICINI (pin 51) setting the mode of operation of the particular PoE Manager (item 7 in Figure 7)

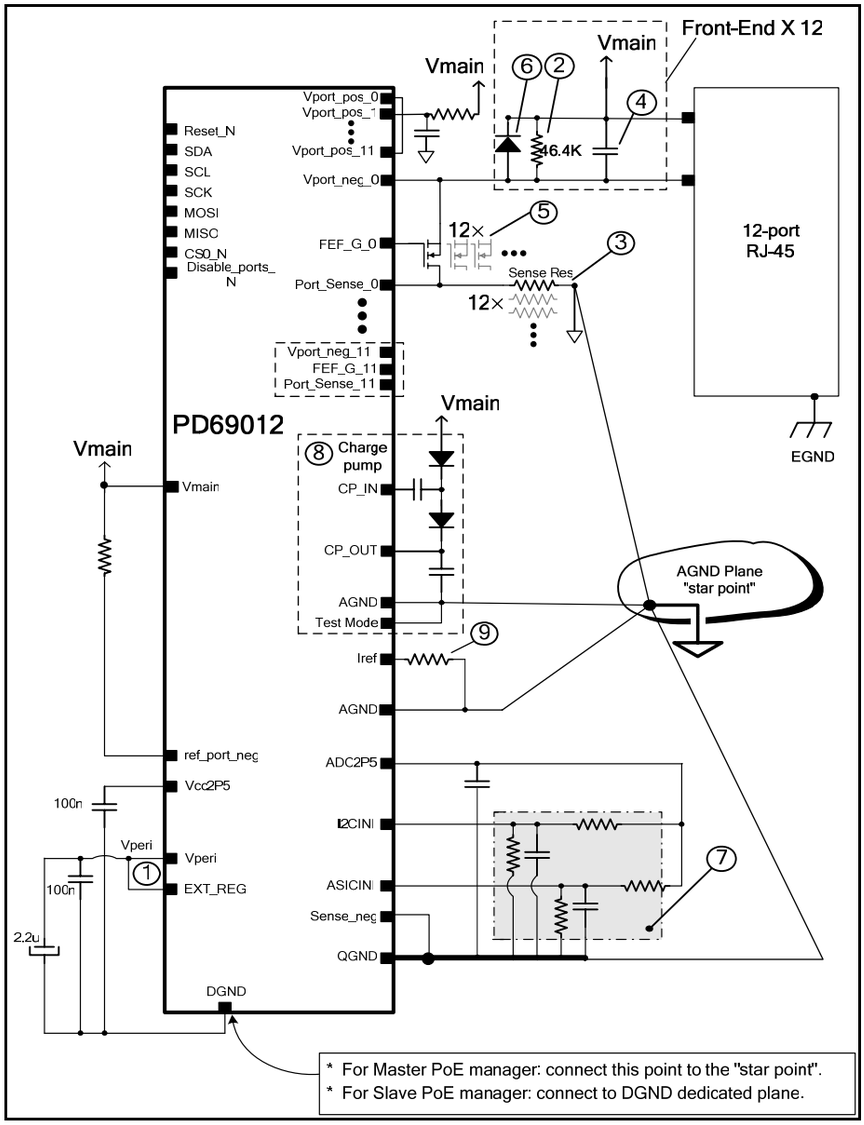

Figure 7: Component Identification for PD69012 Circuitry

Port Outputs

For robust design, the ports output traces are to be 45-mil wide so as to handle maximum current and port power.

However in order to obtain maximum 10°C copper rise minimum width for traces is set in accordance with the layer location and copper thickness:

- For 2-ounce copper, external layer:15 mils
- For 2-ounce copper, internal layer: 20 mils
- For one-ounce copper, external layer: 25 mils
- For one-ounce copper, internal layer: 30 mils
- For 1/2-ounce copper, external layer: 30 mils
- For 1/2-ounce copper, internal layer: 55 mils (20°C copper rise)

The ports output traces must be short and parallel to each other, in order to reduce RFI coupling and to keep the series resistance low.

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Output Ports Interconnections

The PoE ports outputs must be connected to the switch's pulse transformers as shown in Figure 6. The common mode choke is used to reduce RFI noise. A 'Bob-Smith' termination (resistor-capacitor) to chassis ground is optional.

The circuit is to be located as close as possible to the pulse transformer.

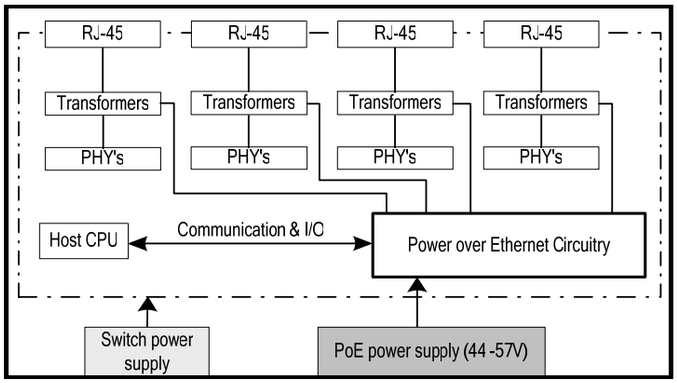

Figure 8: Block Diagram - PoE Circuitry inside the Switch

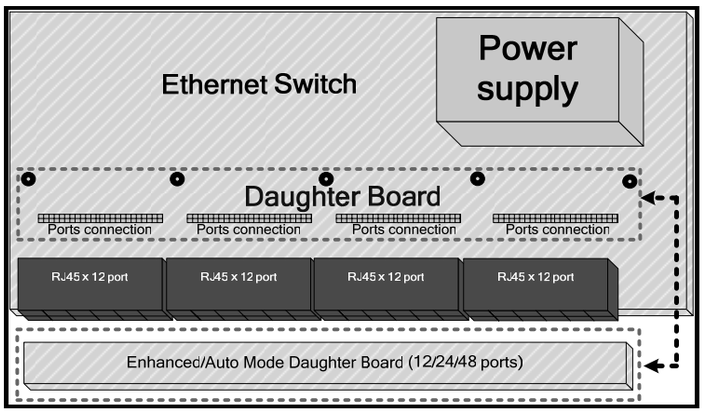

Figure 9: PoE DB Circuitry inside the Switch

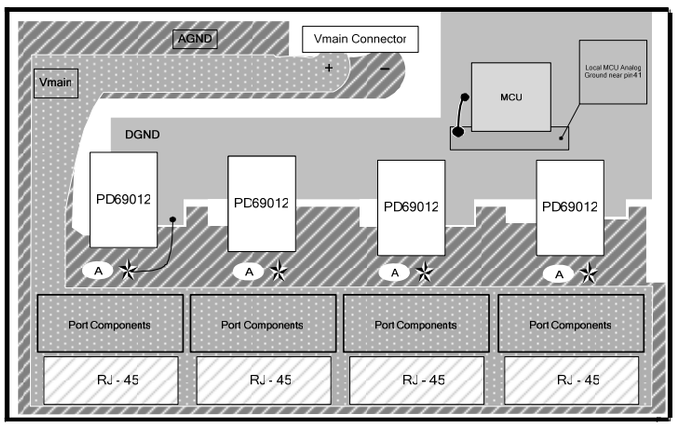

Figure 10: Ground and Power Planes

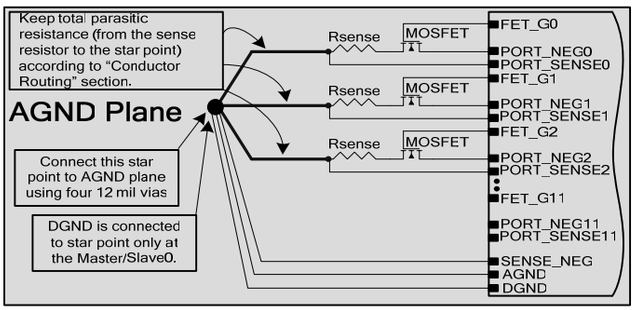

Figure 11: Star Point and Sense Resistors Design Criteria

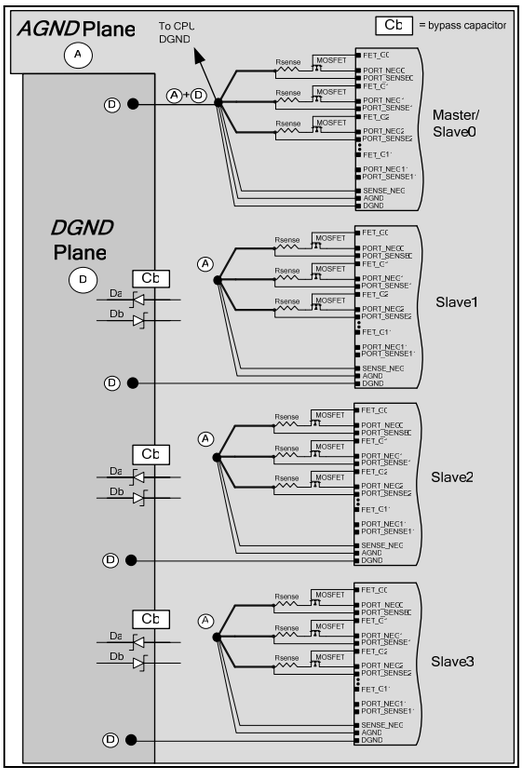

Figure 12: Overall Grounding Scheme

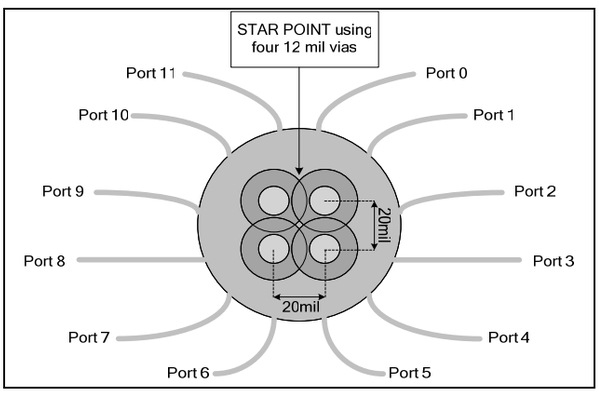

Figure 13: Star Point Layout

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Thermal Pad Definition & Design

Introduction

The PD69012 utilizes thermal dissipation exposed pad in an 80-lead LQFP package.

The package is molded in such a way that the lead frame is exposed at the bottom surface of the package.

Direct soldering of the exposed pad to a copper land provides an efficient thermal path.

Requirements

The PCB design should consider the exposed pad of the PD69012. This pad is used for thermal cooling of the package. The PD69012 pad is soldered to a dedicated area on the PCB.

Thermal Pad Design

The PD69012 is packaged in an 80LQFP package type with an exposed pad. This exposed pad is a metal substrate on the bottom of the package.

The attachment process for exposed pad package is equivalent to standard surface mount packages. See Figure 14 for a design PCB layout of the recommended contact pad.

For proper heat dissipation, the following footprint layout guidelines should be followed:

- The AGND copper area must be the first layer under the PoE Manager, to allow lowest heat resistance

Figure 15 shows the associated, solder printing paste masks. The solder printing paste mask openings are lined-up in respect to the thermal pad.

Since large solder printing paste mask openings may result in poor release, the opening should be subdivided as shown in Figure 15:
For a nominal package standoff of 0.1 mm, a solder printing mask stencil thickness of 5 to 6 mils should be considered.

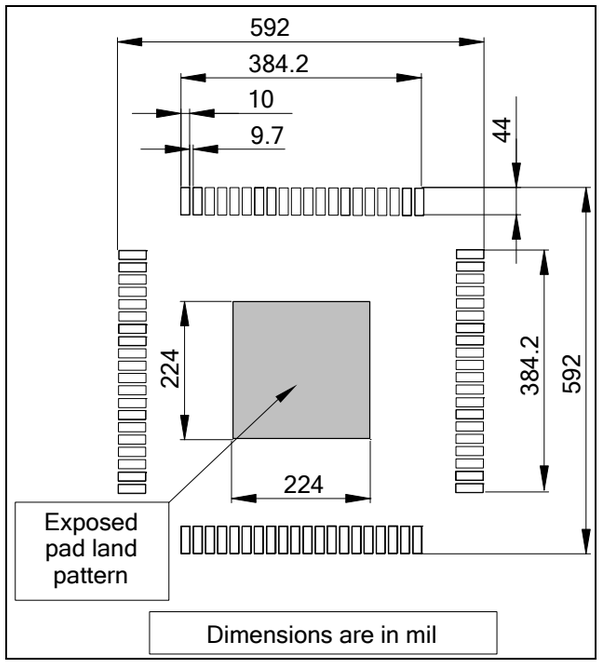

Figure 14: Recommended PCB Layout- Thermal Pad Footprint (CS)

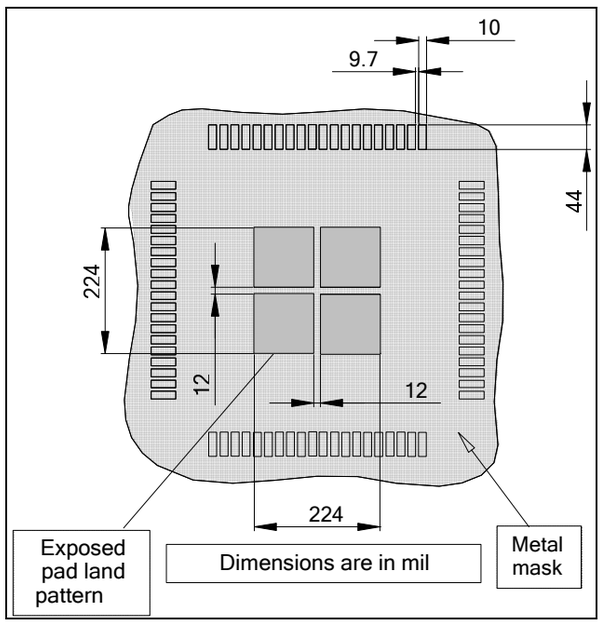

Figure 15: Recommended Solder Printing Paste Mask Apertures (CS)

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 31 May. 08		Initial release
0.2 / 31 June. 08	Whole document	General modifications as a result of developement
0.3 / 31 August. 08	Overhaule maintenance	Figures 2, 3 and 4 replaced
0.4 / 22 December. 08	P1, P9	1. Figures 10, 11 and 12 replaced 2. draft 3.0 modified to draft 3.3 3. xDisable_ports signal isolation has been changed from "Normaly Enable" to "Normaly Disable".
0.5 / 22 January. 09	P7	Sense resistor value changed to support 500mohm or 487mohm.

22/01/09 (Rev. 05)

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Cat. Number: 06-0055-080

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