Designing a 48-port Enhanced PoE System (802.3af/802.3at Compliant, UART/I²C Interface)

APPLICATION NOTE

Introduction

This application note provides detailed information and circuitry design guidelines for implementing a 48-port Power over Ethernet (PoE) system based on Microsemi's™ 12-channel PoE manager – PD69012. For communication with hosting system a UART or I²C interface is used.

This document allows designers to integrate PoE capabilities, as specified in IEEE802.3af and IEEE802.3at standards, into an Ethernet switch. Enhanced mode provides additional PoE capabilities using PD69000 PoE Controller.

PD69012 PoE manager implements real time functions as specified in IEEE 802.3af and IEEE802.3at standards, including detection, classification and port-status monitoring, as well as system level activities such as power management, and MIB (Management Information Base) support for system management. PoE manager is designed to detect and disable disconnected PDs (Powered Devices) using both DC and AC disconnection methods, as specified in standard.

This application note should be used in conjunction with *Application Note 175, catalogue number 06-0055-080 for Layout Design Guidelines*. For easier design and development, an Evaluation board (**P/N PD-DB-7448E**) can be ordered.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69012 datasheet, catalogue number 06-0069-058
- PD69000 datasheet, catalogue number 06-0070-058
- Application Note 175, Layout Design Guidelines for PoE Systems, catalogue number 06-0055-080
- PD-IM-7400 Evaluation Board User Guide, catalogue number 06-0025-056
- Serial Communication Protocol User Guide, catalogue number 06-0032-056
- Technical Note 134, Emergency Power Management, catalogue number 06-0014-081

Background

PD69012 has two operation modes:

- **Auto mode** (Automatic operation) provides a basic set of features for a stand-alone application (no need for a local PoE Controller).
- **Enhanced mode** provides an enhanced features-set using a local dedicated PoE Controller (PD69000).

This application note defines Enhanced mode of operation. In this mode, PoE managers communicate with PD69000 PoE Controller via an Enhanced Serial Peripheral Interface (ESPI) bus.

PoE Controller's features are listed below.

Enhanced Mode Features

- IEEE 802.3af compliant
- IEEE802.3at compliant
- IETF Power Ethernet MIB (RFC 3621) compliant
- Can be cascaded for up to eight PoE managers, 96 ports
- Pre-standard PD detection
- Detection of Cisco devices
- UART and I²C communication
- Advanced power management; up to 96 ports
- User friendly PoE communication protocol
- Continuous voltage and current monitoring per port and per system
- Parameter setting per port and per system
- Disables ports
- Thermal monitoring & protection
- Built-in 3.3V regulator
- Internal power on reset
- Port matrix
- Interrupt out
- H/W system status pin
- Port's LEDs support
- Emergency Power Management
- Software download for program upgrading
- RoHS compliant

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Integration

The system described is destined for a 48-port switch. Same design can be applied to 1 to 8 PoE managers controlling 12 ports each (from 12 ports to 96 ports in multiplies of 12).

PoE system daughter board can be easily integrated on top of a switch and thereby provides capability to add any PoE application while using different daughter applications (Enhanced mode or Auto mode) (refer to Figure 1).

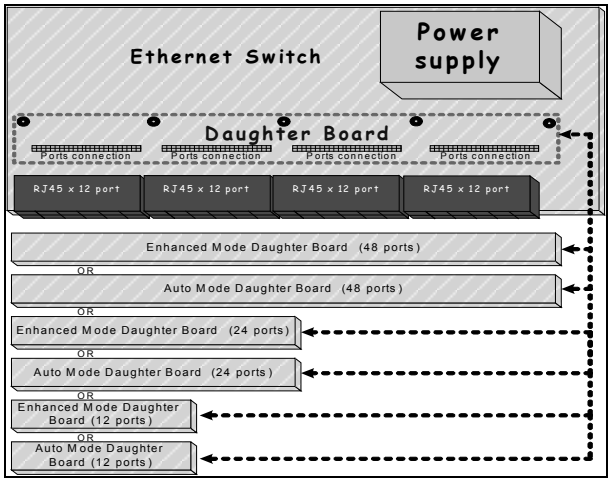

Figure 1: PoE Daughter Board Integration

Overall Description

Circuit includes the following blocks (Figure 2):

1. PoE circuit for 48 ports based on four PD69012s

2. PoE Controller circuit, used for initializing, controlling, and monitoring each of the PD69012s via an internal ESPI bus. PoE Controller communicates with Host CPU via an isolated UART interface, or via a non-isolated I²C interface (refer to Figure 2, options A and B).

3. Isolation circuit for UART and isolation circuit for indication/control signals (refer to Figure 2, option A) or isolation circuit for ESPI bus and Reset signals (refer to Figure 2, option B).

Note In general, (unless otherwise mentioned) this Application Note deals with the UART interface; for I²C interface information, refer to I²C Interface section.

In cases where a 48 port enhanced PoE system having UART interface is designed, refer to Figure 6 to Figure 12.

In cases where a 48 port enhanced PoE system with I²C interface is designed, refer to Figure 7 to Figure 10, Figure 13 and Figure 14.

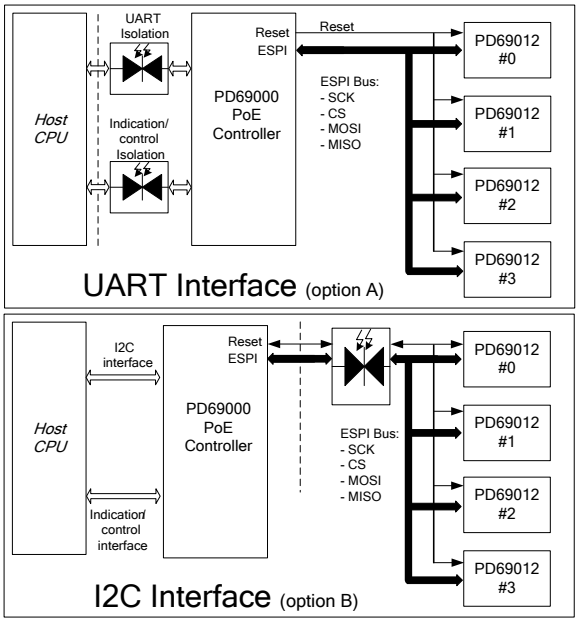

Figure 2: 48-port Enhanced Mode Configuration

General Circuit Description

The 48-port configuration for a PoE system shown in Figure 2 comprises four PoE managers circuits (PD69012) functioning as slaves to a PoE Controller (PD69000). The PoE Controller utilizes a ESPI bus to control PD69012s. PoE operations are automatically performed by PoE manager circuits, while PoE Controller performs power management and other tasks.

Communication Interfaces

Communication between Host CPU and local PoE Controller is performed via an isolated UART interface or an I²C interface. For more information, refer to the *Serial Communication Protocol User Guide, catalogue number 06-0032-056*.

ESPI Bus

ESPI bus is used for internal communication and includes the following lines:

- **MOSI (Master Out/Slave In)** provides communication from PoE Controller to PD69012s.
- **MISO (Master In/Slave Out)** provides communication from PD69012s to PoE Controller.
- **SCK** is a serial clock generated by the Controller.
- **CS (Chip Select)** is utilized by the PoE Controller to transmit data to all PD69012s simultaneously, while only the chosen PoE manager responds back.

Control

An **xReset_IN_isolated** control signal driven by Host CPU resets the PoE system.

An **xDisable_ports_isolated** control signal driven by Host CPU disables all PoE ports at once.

Refer to Figure 3.

Indications

A digital output signal, **xSystem_ok_isolated** derived from PoE Controller, indicates main input voltage is within range.

PoE Controller produces an **xInt_out_isolated** interrupt signal which indicates PoE events.

Communication Flow

Host CPU issues commands, utilizing a dedicated Serial Communication Protocol to PoE Controller via isolated I/O lines. This isolation is a basic requirement of IEEE PoE standards.

PoE Controller converts Serial Communication Protocol to the required register configuration, for storage in PD69012.

Main Supply

PoE system operates within a range of 44 to 57V (802.3at port's range is 50 to 57V). To comply with UL SELV regulations, maximum output voltage **should not** exceed 60V.

When utilizing DC Disconnect function, the PoE system can operate over up to 57V. However, AC Disconnect function requires a 5V level to be added to supply voltage (55 + 5 = 60V).

Therefore, maximum input voltage **should not** exceed 55V. Supplied voltage must be isolated from Switch supply and chassis by $1500V_{rms}$.

Grounds

Several grounds are utilized in the system:

- Chassis
- Digital
- GND_Analog_CPU (Controller's ground)
- Analog

Chassis ground is connected to switch's chassis ground. This ground plane should be $1500V_{rms}$ isolated from PoE circuitry.

Digital, **GND_Analog_CPU** and analog grounds are electrically same ground. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

This is further detailed in the *AN-175 Application Note, catalogue number 06-0055-080*.

3.3V Regulator

Each PD69012 has a 3.3V regulator (EXT_REG & VPERI) providing up to 6mA. This current is utilized for powering components external to PoE domain; those components must also be isolated by $1500V_{rms}$ from the switch circuitry.

An external transistor can be connected to output port to increase current. Q1 can provide up to 30mA to PoE Controller and to opto-couplers in the interface circuitry (refer to Figure 6).

Detailed Circuit Description

Following sections describe Overall Block Diagram (refer to Figure 6).

Communication Interfaces

There are two communication interfaces in this circuitry:

- Between Ethernet switch and PoE Controller; this interface is a $1500V_{rms}$ isolation UART interface or an I^2C interface. Note that each circuitry's side is fed by a separate power supply. Isolation circuit is detailed in Figure 12.
- Between PoE Controller and PoE managers; interface used here is a standard ESPI.

Control and Indication Signals

Control/Indication signals are of the single H/W lines type, running between Host CPU and PoE Controller. These signals are optically coupled to achieve $1500V_{rms}$ isolation (refer to Figure 3).

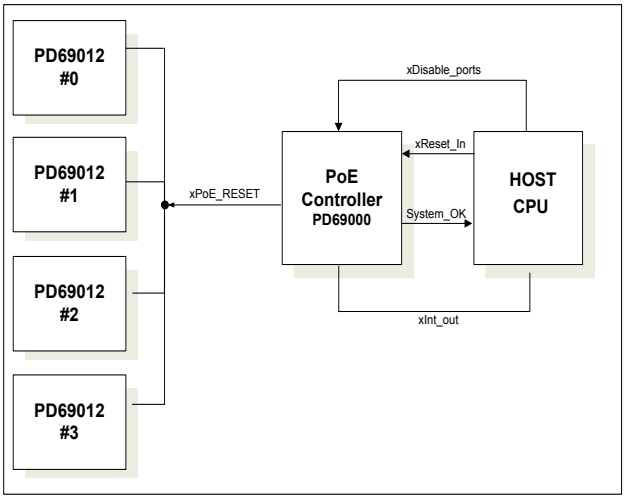

Figure 3: Control and Indication Signals

Control Signals

There are two control lines driven by Host CPU to PoE Controller:

- **xDisable_ports**: Disables all PoE ports. When PoE Controller detects low level voltage at pin #29 it sends a disable command via ESPI to PoE manager's ports.
- **xReset_In**: Resets PoE Controller and all PoE managers. When the PoE Controller detects low level voltage at pin #1 it enters Reset mode and all its output pins switch to Tri-state mode. When **xReset_In** line returns to 'high', PoE Controller initializes and sends (upon a flag state) 'low' level

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logic to PoE managers via **xPoE_RESET** line (pin # 32).

Indication Signals

Two signals are utilized to provide Host CPU with the following event indications.

- **System_OK**: Indicates main voltage is within desired range.
- **xint_out**: Interrupt signal coming from PoE Controller, indicating events such as Port On, Port Off, Port Fault, PoE Manager Fault, Voltage out of Range, etc.

For full list of interrupt events, refer to serial communication protocol, *User Guide 06-0032-056*.

PoE Controller Circuitry

Refer to Figure 7.

PoE Controller features 1.2Mb/s ESPI for each of the PoE managers, and a communication interface with Host CPU via UART or I^2C protocol.

UART or I^2C communication between Host CPU and PoE Controller are managed by setting the address of pin #25 of PoE Controller (I^2C_ADDR). For UART and I^2C communication address table, refer to I^2C Interface, page 6.

PoE Controller runs at about 10MHz, facilitated by an external resonator XL1.

PoE Controller requires stable, filtered power for its operation. Therefore a number of components are included in the design:

- **C86 and C89**: Used for filtering and stabilization of V_{PERI} voltage generated by PD69012 circuitry and Q1.
- **C82 and C83**: Used for filtering reference voltages (V_{DDAD} and V_{REFH}).
- **VPERI**: PoE Controller's 3.3V operating voltage is obtained from PoE manager Circuitry #0 via current driver Q1 (refer to Figure 6). This device can provide up to 30mA, based on the application requirements.
- **SELF_RESET**: As required by the application, PoE Controller can self-reset itself. This reset can also be performed by an external source utilizing **xReset_In** signal (usually by Host Controller).
- **HW_VER (Hardware Version)**: This input line provides a hardware configuration indication to PoE Controller. This line is factory controlled and may not be changed (voltage divider R134/R132).

LED Support

Refer to Figure 4.

LED support for port status indication is provided by **SPI bus** (SCK and MOSI), **LED_CS** and **xLED_Latch** signals. Bus behavior is synchronous serial communication (Clock, Data) in one direction (write only), 100kb/s, transmitting the status of up to 96 ports. Packet is transmitted with Start header and End header bytes. For more details, refer to *Technical Note-118 catalogue number 06-0008-081*.

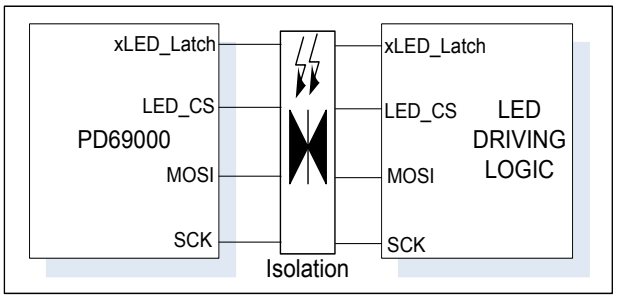

Figure 4: SPI Bus and LED Support

Emergency Power Management

PoE circuits can be powered by up to four separate power supplies (refer to Figure 5). It is recommended each power supply be capable of generating a logic signal that indicates its operate/fail status. Two logical output signals can be derived from PSU:

- Power good signal (default)
  - PG = logical '1'; indicates operational power supply
  - PG = logical '0'; indicates failed power supply

  In this mode, R241 should not be connected, whereas R240 should be connected in a pull-down configuration.
- xPower good signal
  - PG = logical '0'; indicates operational power supply
  - PG = logical '1'; indicates failed power supply

  In this mode only R241 is connected in a pull-up configuration.

The PoE circuit allocates power to the system in accordance with overall available power derived from logic signals that arrive from power supplies. With four power supplies that have up to four different output power levels; up to sixteen power banks can be derived from their combinations. Pins being used are as follows:

Pin Number	Signal	Remarks
#36	PG0	Power Good 0
#37	PG1	Power Good 1
#38	PG2	Power Good 2
#39	PG3	Power Good 3

If PG pin is not used, pin can be connected to GND or V_{peri} (according to the appropriate PG logic) with no resistor. Figure 5 illustrates the connections between power supplies' logic signals and PoE Controller.

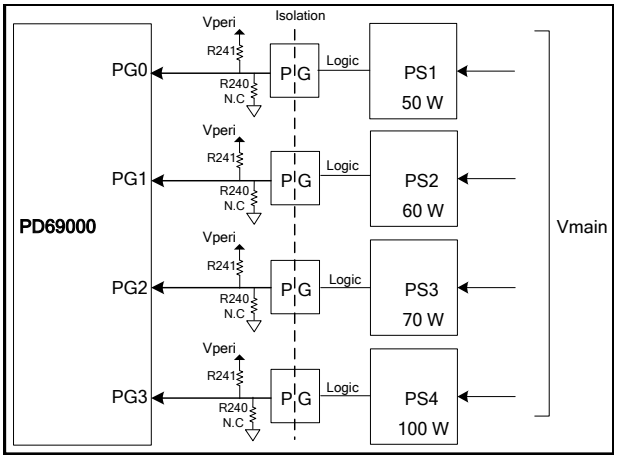

Figure 5: Power Good

For isolation requirement destined for Emergency Power Management, refer to *Technical Note-134 catalogue number 06-0014-081*; "Isolation Requirements Section".

xHSWP - PoE Hot Swap Functionality

Hot swapping (hot plugging) functionality is the capability to remove and replace PoE system while units are operating. PoE system can be plugged and unplugged only while using dedicated hot swap hardware (not included in this application note). An xHSWP signal is issued from PoE Controller to hot swapping hardware to control it.

PoE Manager Circuitry

Refer to Figure 8.

PD69012 performs a variety of internal operations and PoE functions that require a minimum of external components. Each PD69012 handles up to 12 ports. Figure 8 shows PoE Manager #0 with its related components for a 12-port configuration.

Note For the solution described in this Application Note (48-port), multiply by four the circuitry shown in Figure 8.

Enhanced Mode Configuration

Set by R328/R329 divider tied to the ASICINI line (R328/Figure 6). Divider's voltage value is set at Enhanced Mode operation to configure PoE manager to Slaves 0-7, as specified in the following table:

ASIC_INI	Minimum Voltage	Maximum Voltage	Resistors Value	
			R329 (low)	R328 (high)
Slave0	0.19	0.29	10000	93100
Slave1	0.35	0.44	10000	52300
Slave2	0.51	0.6	10000	34800
Slave3	0.67	0.75	10000	24900
Slave4	0.83	0.9	10000	18700
Slave5	0.99	1.06	10000	14300
Slave6	1.15	1.21	10000	11300
Slave7	1.3	1.36	10000	8870

Line Detection Calibration

When performing line detection procedure, PoE manager utilizes certain voltage levels over output port. To accurately set these levels, reference voltages are developed across a parallel combination of R218 and R222.

This combination simulates the equipment tied to the port.

Reference Current Source

Reference for internal voltages within PD69012 is set by a precision resistor (R313).

Charge Pump

An increase of 5V over power supply main input (44 to 55V, + 5V) is required.

5V increase is implemented by a Charge-Pump circuitry that utilizes three elements:

- A self-sustaining clock mechanism, utilized to start and keep the process going. This is performed in PD69012 internally.
- Energy transfer element (C64 and C66).
- Switching diode to constrain energy flow in one direction (D50).

Sense Resistors

A 500mΩ (or 487mΩ), (1%) sense resistor is connected to port output line. This resistor measures port's current.

Resistance of resistor with its traces should be close to 500mΩ. For more information, refer to *Layout Design Guidelines, catalogue number 06-0055-080*.

Low Pass Filter

Each of the output ports includes internal protection circuitry against external discharges that may damage PD69012. C67 and R244 create a path to the ground which limits damaging potentials (for circuitry of PoE Manager #0).

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Protection Fuse for Abnormal Operating Voltage

When an IC experiences an input voltage above its absolute maximum rating, it is exposed to unexpected damage. Since PoE manager is connected to a high current source, best design practice is to use a protection fuse (F49) to avoid high current path during PSU over voltage faults.

Front-end Circuitry

Refer to Figure 9.

This circuit is an analog front-end destined for a single port. For this application note, circuit is to be multiplied up to 48 times in accordance with the number of PoE ports in the system.

Output Ports

Refer to Port 0.

Output port circuitry is shown in Figure 9. Note that R10 (46.4k) is of the same value as R218, used as a line detection calibration resistor (Refer to Figure 9). Each port In turn is supplied with a constant current across this resistor.

Load resistance of PD attached to port is calculated in parallel with R10. Resulting voltage developed across both resistances is compared to calibration source (R218 || R222) voltage, which establishes terminal's validity. Other components are also used:

- D1 is a polarity reversal diode, used to prevent a reversed voltage from an external source.
- C1 forms a noise suppression component.
- F1 is utilized as a current limiting device, operating as specified in IEC 60950-1:2001. If the power supply is lower than 100W it is not required.

Note If output port circuitry is not fully populated, meaning 10 ports instead of 12, then unused ports are to be wired as follows: **PORT_SENSE** and **FET_G** should be tied to **AGND**, and **VPORT_NEG** should be tied to V_{main} nets. The following components can be removed for unused channels: Q127, C1, F1, D1, and R10.

UART Interface Circuitry

Refer to Figure 12.

Isolation circuitry comprises opto-couplers that are destined to provide $1500V_{rms}$ isolation required by standard (IEEE 802.3af and IEEE802.3at).

Circuit supports:

- 3.3V (or 5V) TTL level signals
- 19,200 bps
- 8 bit
- No parity
- 1 stop bit
- No flow control

I²C Interface

Refer to Figure 13 and Figure 14.

PoE Controller can communicate with hosting system using UART or I²C communication.

For I²C interface, cost effective design is to place PoE Controller in Host domain and isolate ESPI bus and reset signals (refer to Figure 2; PoE Controller is $1500V_{rms}$, isolated from PoE manager domain).

- To design a 48 port Enhanced PoE system with UART interface, refer to Figure 6 through Figure 12.
- To design a 48 port Enhanced PoE system with an I²C interface, refer to Figure 7 through Figure 10, and Figure 13 through Figure 14.
- An SDA signal should be connected to pin #4 of the PoE Controller. An SCL signal should be connected to pin #5 of the PoE Controller.

I²C communication between Host CPU and PoE Controller is managed by setting PoE Controller's address. This is done by selecting a value for R306. This resistor sets analog level into pin #25 (I2C_ADDR) as specified in the following table.

I²C Address	Address (hex)	R306 (ohms)	I²C Address	Address (hex)	R306 (ohms)
#0	UART	NA	#8	0x20	8870
#1	0x4	97600	#9	0x24	6810
#2	0x8	53600	#10	0x28	5230
#3	0xC	35700	#11	0x2C	3920
#4	0x10	25500	#12	0x30	2800
#5	0x14	19100	#13	0x34	1870
#6	0x18	14700	#14	0x38	1020
#7	0x1C	11300	#15	0x3C	324

Ground Interface Connection (AGND)

Power supplies ground connector J4 (refer to Figure 6) enables the current a path back to power supply.

Ground connection should be capable of carrying all strings current back to power supplies.

Thermal Design

Design for 802.3at PoE standard should take into account power dissipation of PoE manager, power dissipation of associated circuitry, and maximum ambient operating temperature of switch. Adequate ventilation and airflow should be part of design to avoid thermal over-stress on the following components:

Ambient Temperature

Application's thermal design should take into account temperature derived from Switch's power dissipation and from PoE daughter board, powered at maximum load.

PD69012 Maximum Operating Temperature

PoE design should ensure PD69012's maximum operating junction temperature (150° C) is **not** exceeded under worst case conditions. Worst case conditions typically involve operation under maximum ambient temperature, output ports fully loaded at 802.3at power, and all other unit functions fully operational. *PD69012 datasheet, catalogue number 06-0069-058* contains additional thermal characteristics details.

PD69000

Layout considerations should ensure that:

- PD69000 is placed away from potential high temperature spots.
- Maximum case temperature **does not** exceed 85°C under worst case conditions.

Sense Resistors

Refer to Figure 8.

Each port's front-end circuit has a single sense resistor. Resistor's value should be 500mΩ (or 487mΩ). It dissipates about 0.26W at 720mA (802.3at maximum load) and 62 mW at 350 mA (802.3af maximum load). Resistors should be placed near PD69012 to achieve maximum current accuracy. Heat generated from these resistors contributes to a higher ambient temperature near PD69012. For 802.3af ports, use the following sense resistors types:

QTY for 12 Ports	Description	PCB Footprint	Manufa.	Manufa. Part Number
12	RES TCK FLM 0.500R 1% 125 mW 0805 SMT	PD-0805	Venkel	LCR0805R500FSNT
12	RES TCK FLM 0.487R 1% 125 mW 0805 SMT	PD-0805	Koa	SR732ETTDR487F

For 802.3at ports use, the following sense resistors types:

QTY for 12 Ports	Description	PCB Footprint	Manufa.	Manufa. Part Number
12	RES TCK FLM 0.500R 1% 500 mW 1210 SMT	PD-1210	Venkel *	LCR1210R500FSNT-MS
12	RES TCK FLM 0.487R 1% 500 mW 1210 SMT	PD-1210	Venkel *	LCR1210R487FSNT-MS

*Dedicated part number for Microsemi PoE application; preferential pricing for Microsemi customers.

Note Sense resistor's temperature coefficient of resistance (ppm) must be less than or equal to $\pm 200\ [10^{-6}/^{\circ}C]$.

Power MOSFETs

Refer to Figure 8.

Each port circuit has a single external Power MOSFET. Design should ensure maximum operating junction temperature of MOSFET (150°C or 175°C as specified in MOSFET's datasheet) is **not** exceeded under worst case conditions.

For more details on how to examine and choose a MOSFET for a PoE application, refer to the *'How to choose MOSFET for 802.3at and 802.3af PoE applications' Technical Note*, *catalogue number 06-0022-081*. Examples for approved MOSFETs are shown in the following tables:

Table 1: 802.3af - MOSFETs Examples

#	PCB Footprint	Manufacturer	Manufacturer's Part Number
1	SOT-223	Fairchild	IRLM110A
2	DPAK	Fairchild	FQD5N15
3	SOT-223	Infineon	BSP372

Table 2: 802.3at - MOSFETs Examples

#	PCB Footprint	Manufacturer	Manufacturer's Part Number
1	DPAK	Fairchild	FQD19N10L
2	SOT-223	Fairchild	FDT3612_SB82273 *
3	DPAK	ST	STD10NF10T4
4	DPAK	IR	IRFR3910
5	SOT-223	Infineon	BSP373

*Dedicated part number for Microsemi PoE application; preferential pricing for Microsemi customers.

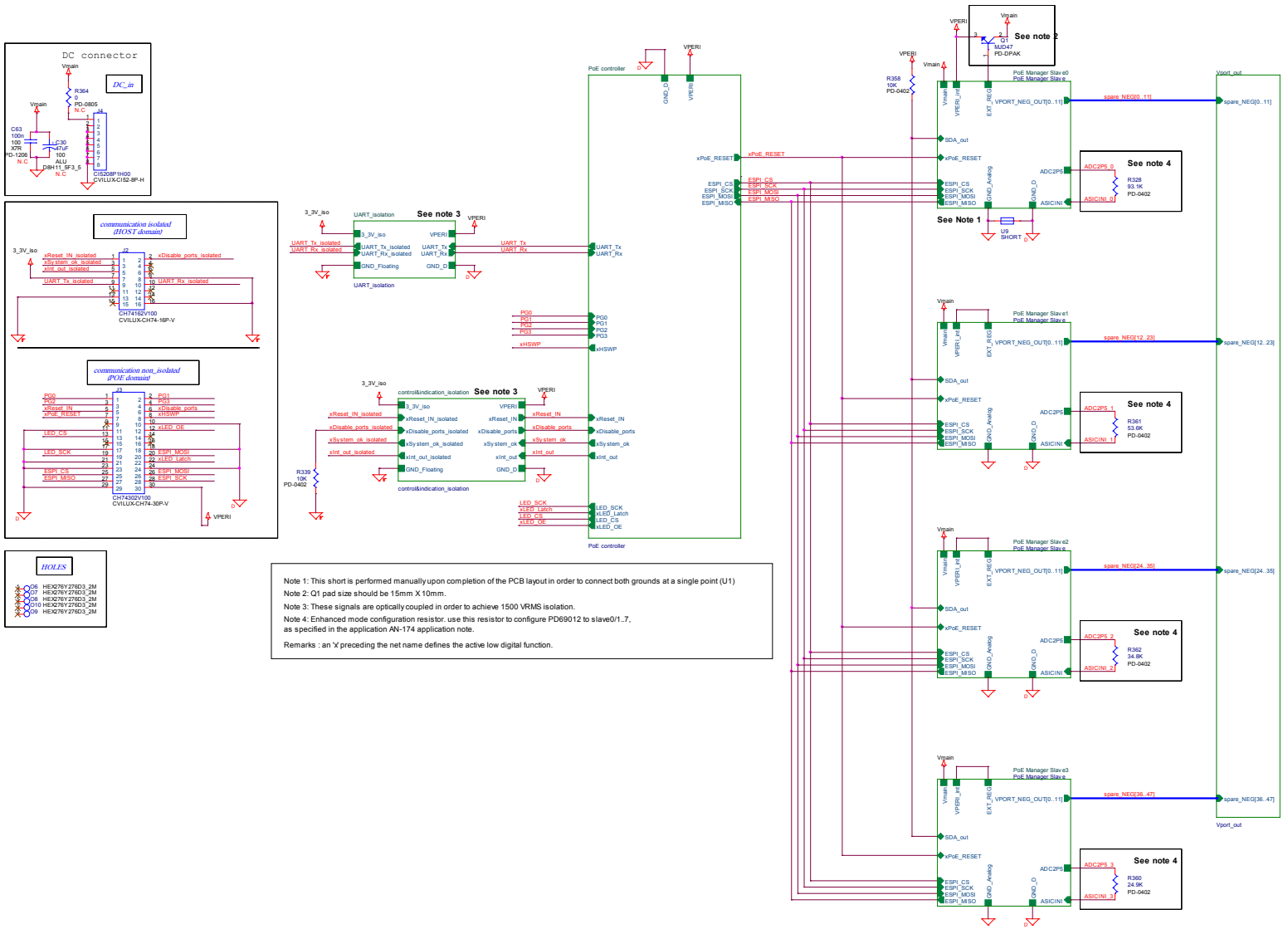

Figure 6: Overall Block Diagram for 48-port Enhanced System (UART Interface)

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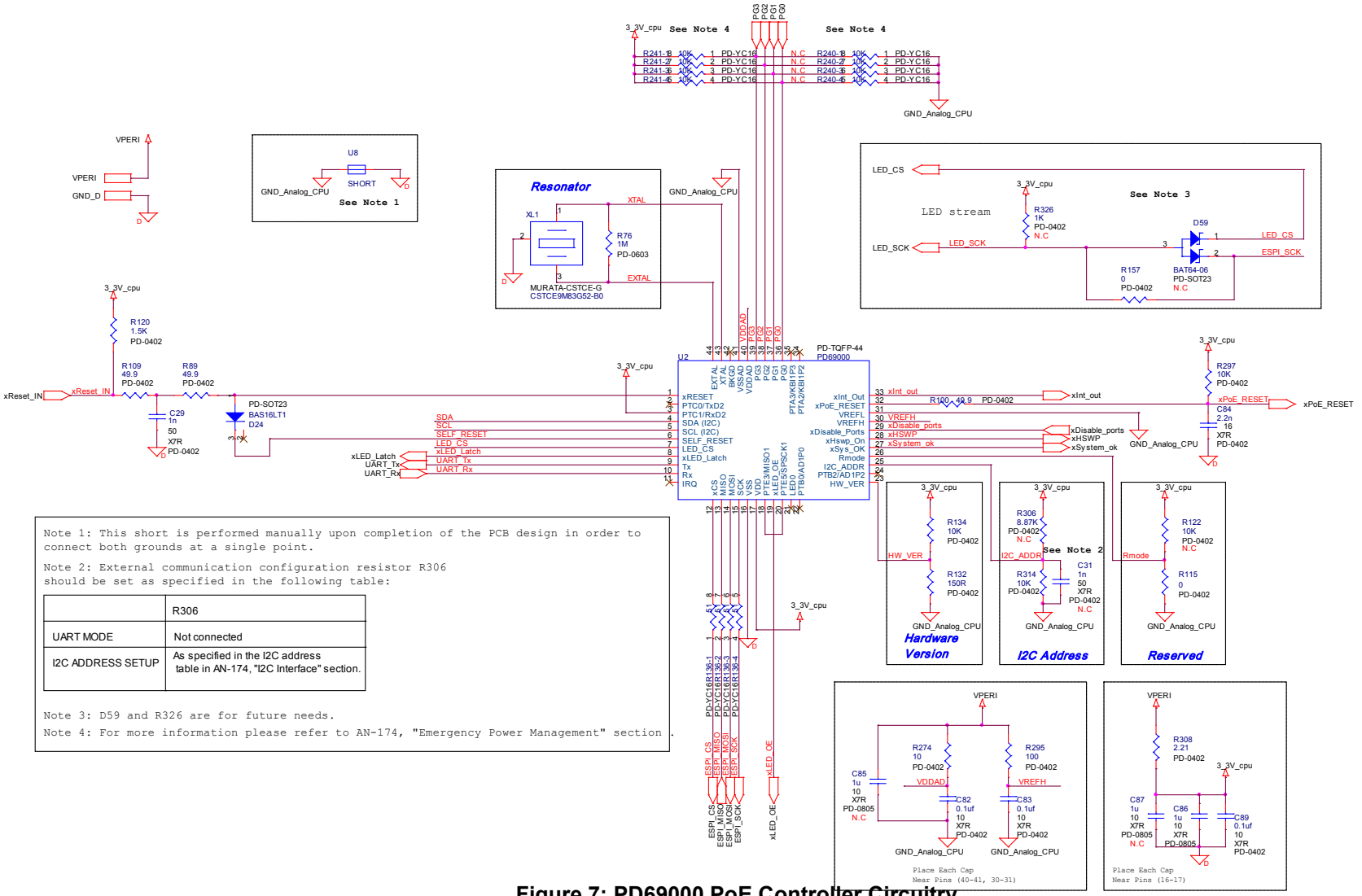

Figure 7: PD69000 PoE Controller Circuitry

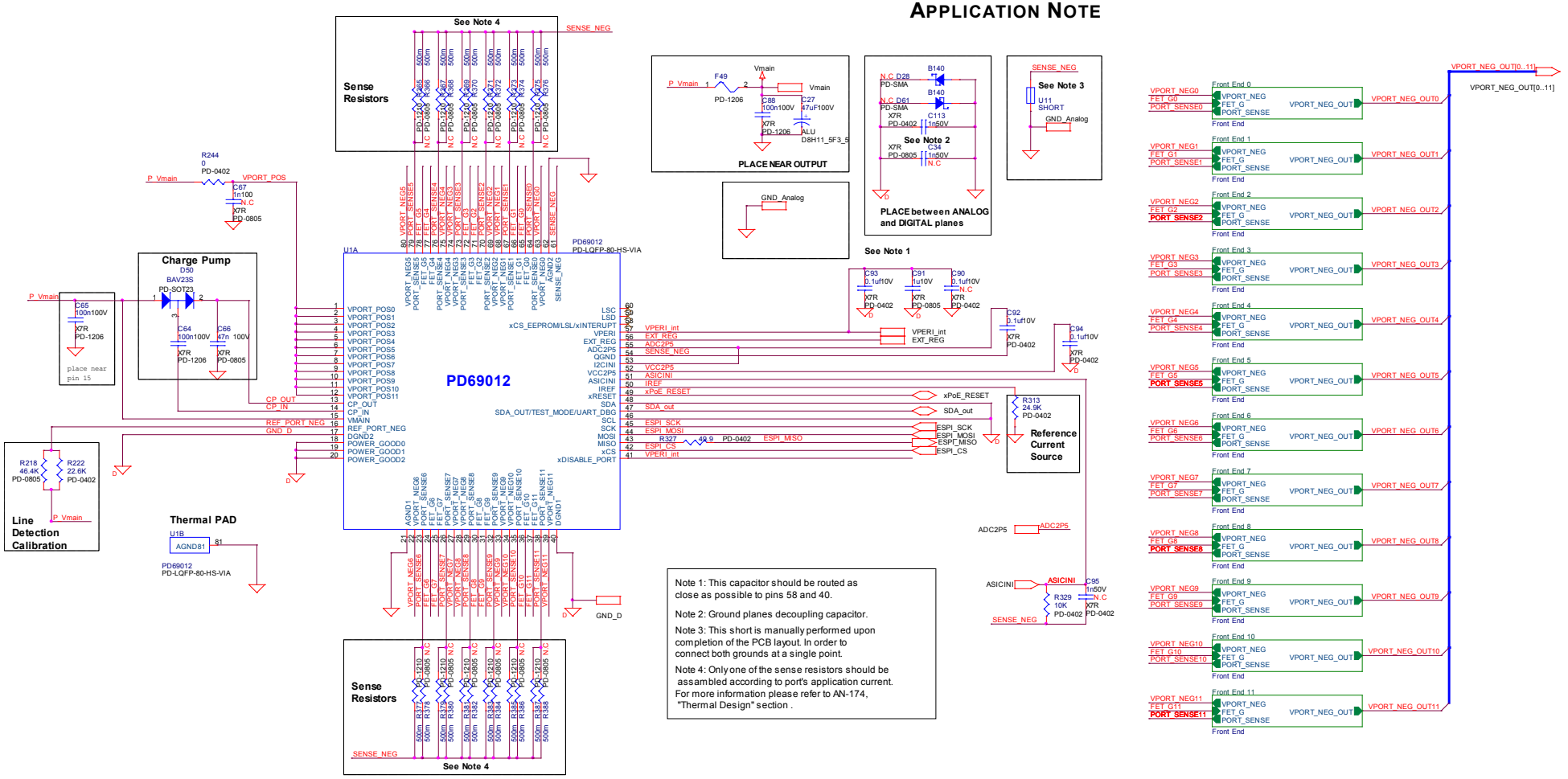

Figure 8: PD69012 Circuitry for PoE Manager #0

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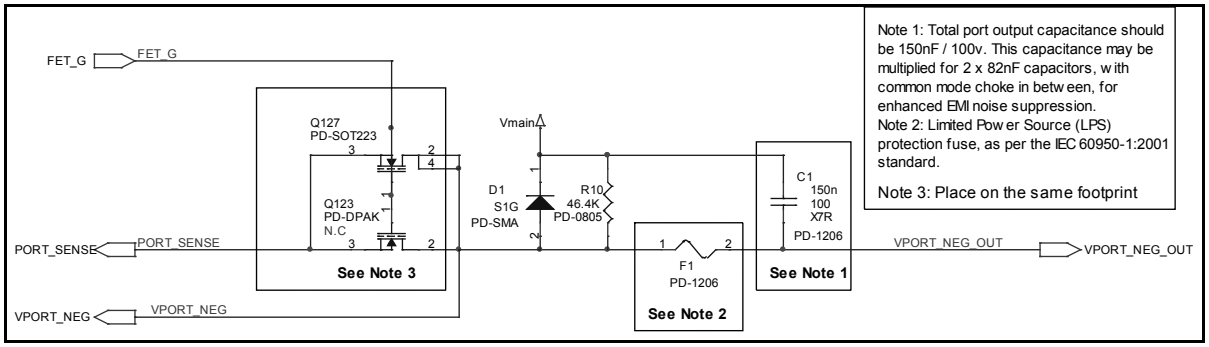

Figure 9: Front-End Circuitry

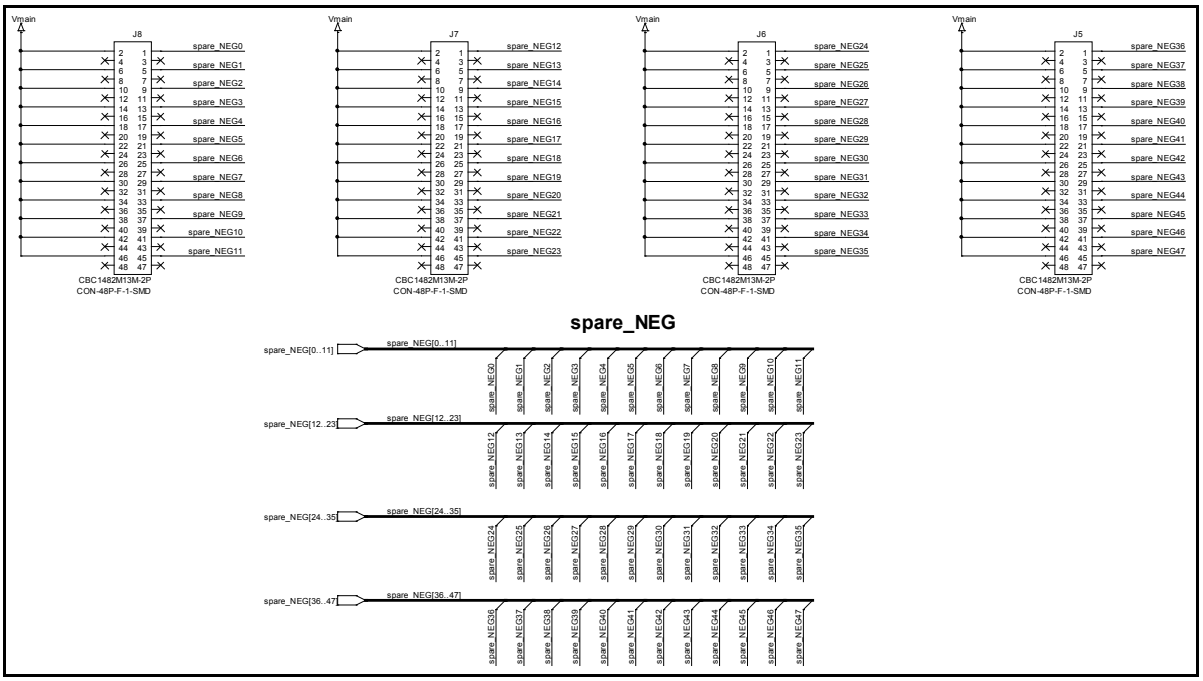

Figure 10: Vport Out (Port's Interface)

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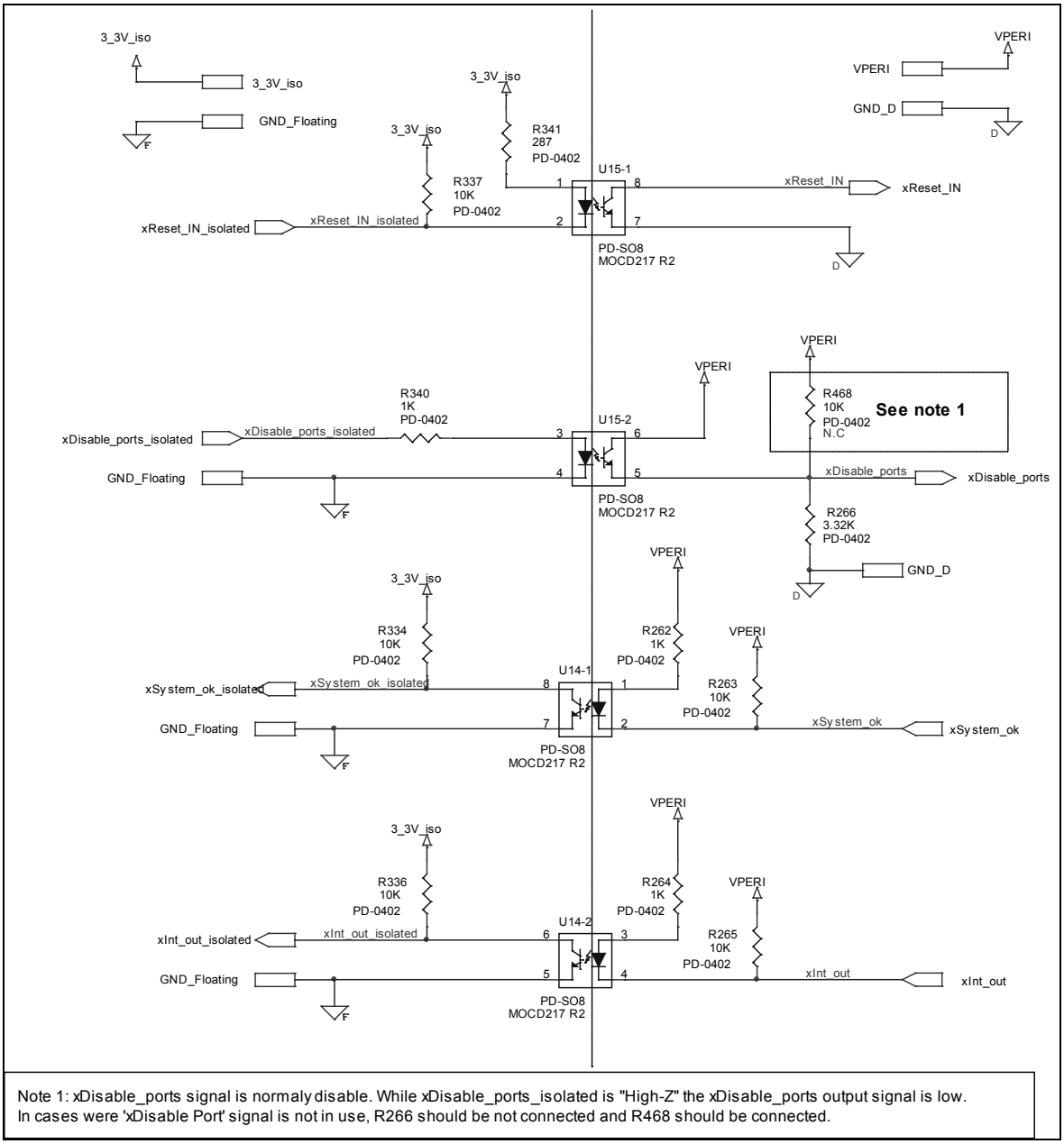

Note 1: xDisable_ports signal is normaly disable. While xDisable_ports_isolated is "High-Z" the xDisable_ports output signal is low.
In cases were 'xDisable Port' signal is not in use, R266 should be not connected and R468 should be connected.

Figure 11: Control and Indication Isolation Circuitry

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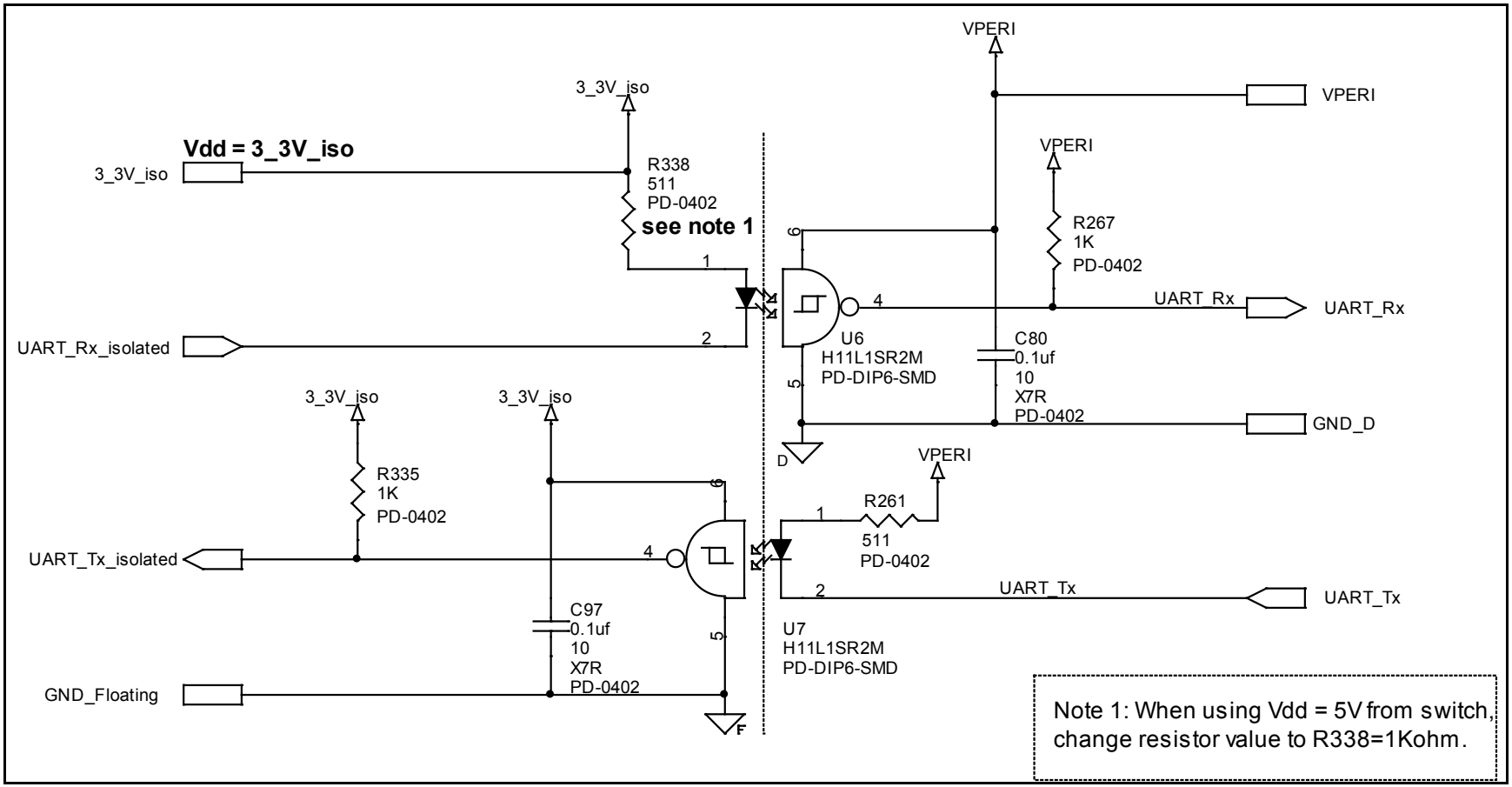

Figure 12: UART Isolation Circuitry

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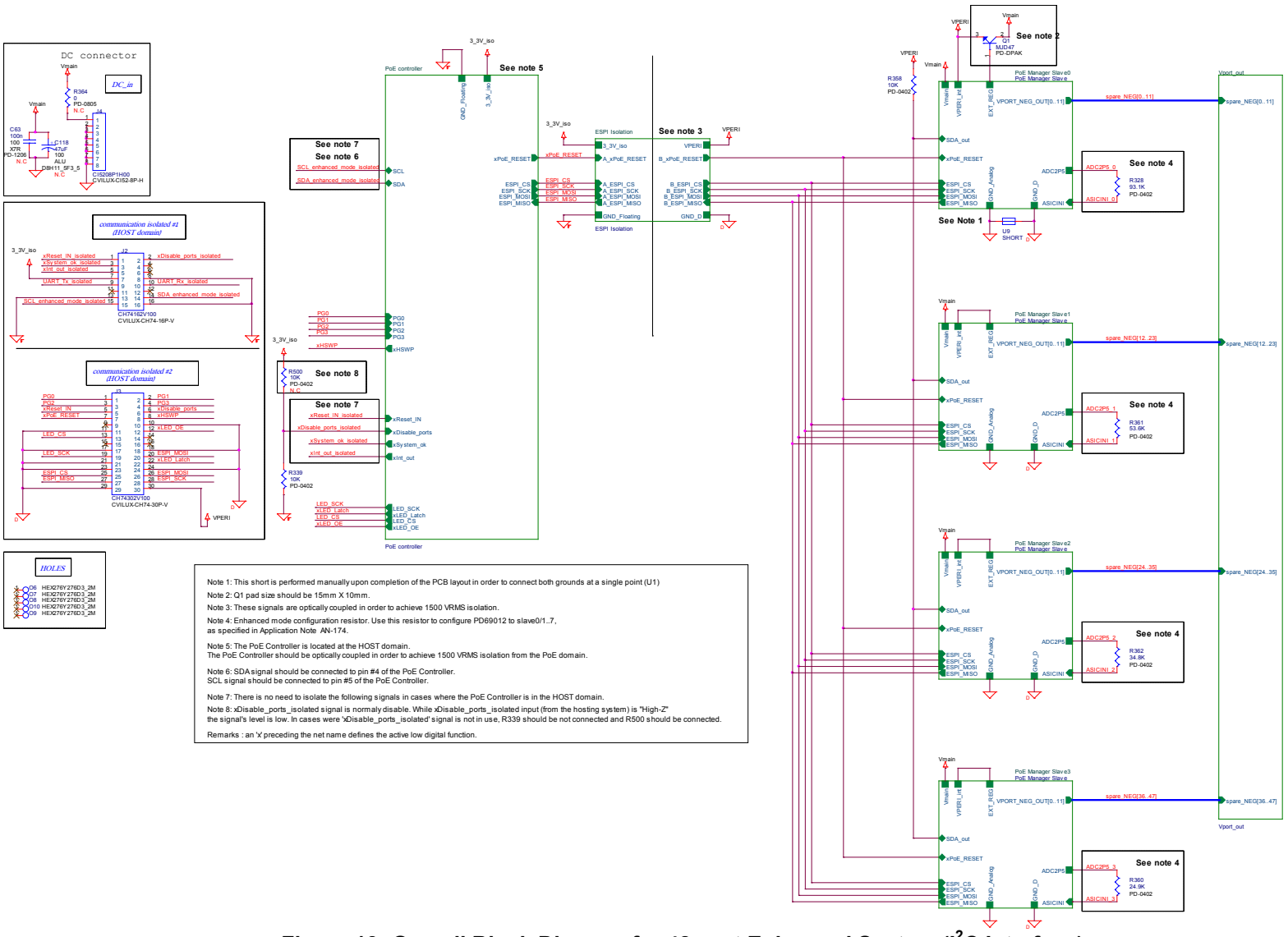

Figure 13: Overall Block Diagram for 48-port Enhanced System (I²C Interface)

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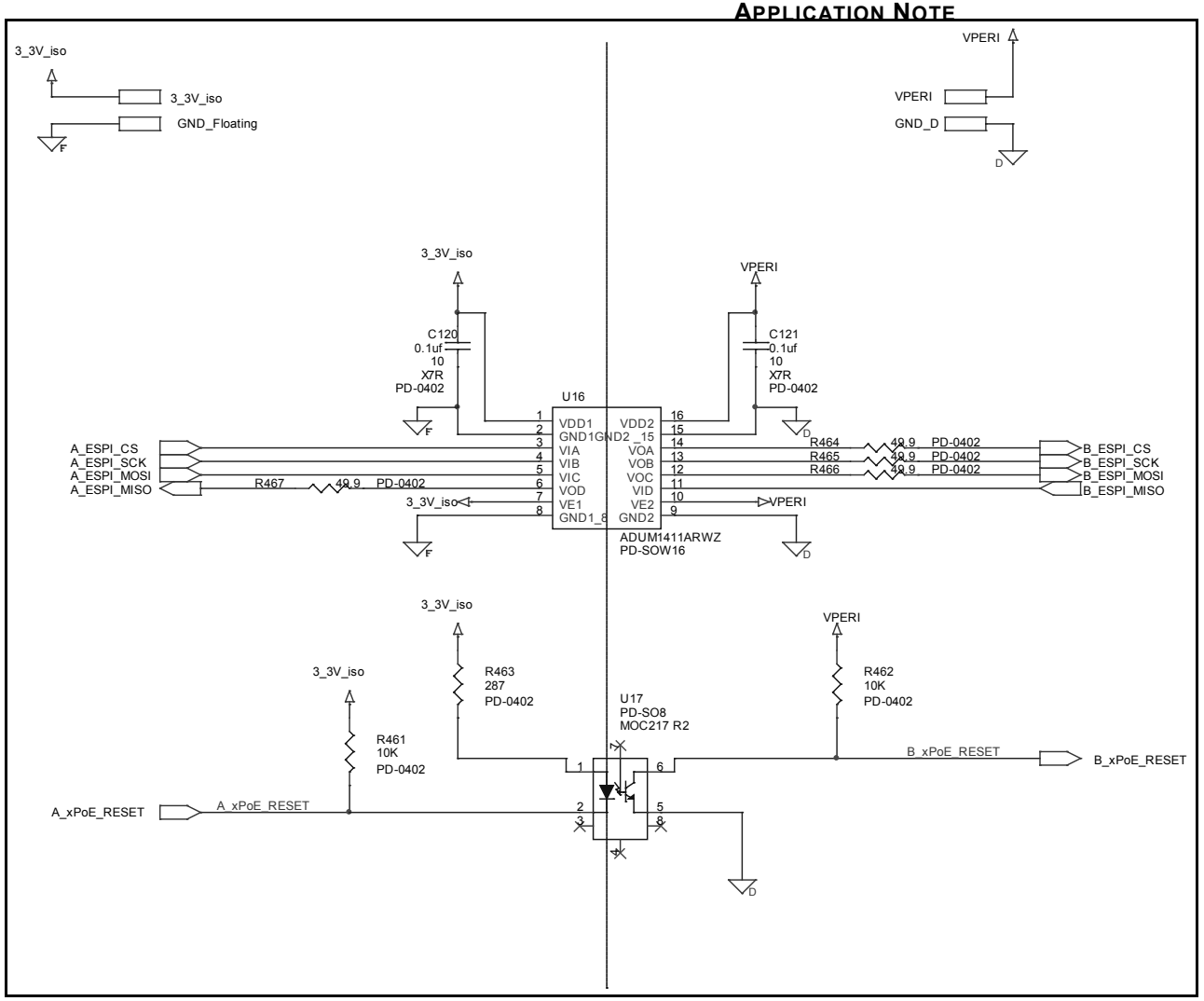

Figure 14: ESPI Isolation Circuitry

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Bill of Materials for a PoE System

Table 3: Main Block Components

Block	Qty	Reference	Description	PCB Foot Print	Manufacturer	Manufacturer's Part Number
Main	1	J2	Pin Header Dual Raw Board mount 16 Pin p 2mm TH	CVILUX-CH74-16P-V	CviLux	CH74162V100
	1	J3	Pin Header Dual Raw Board mount 30 Pin p 2mm TH	CVILUX-CH74-30P-V	CviLux	CH74302V100
	1	J4	Pin Header male 1 row 8 pins Horizontal	CVILUX-CI52-8P-H	CviLux	CI5208P1H00
	1	Q1	TRN NPN 250V 1A 15W D-Pak SMT	PD-DPAK	Fairchild	MJD47
	1	R328	RES SMT 93.1KΩ 1% 1/16w 0402	PD-0402	Rohm	MCR01MZPF9312 Bottom of Form
	1	R358	RES TCK FLM 10K 1% 62.5 mW 0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	1	R360	RES TCK FLM 24.9K 1% 62.5mW 0402 SMT	PD-0402	Yageo	RC0402FR-0724K9
	1	R361	RES SMT 53.6 KΩ 1% 1/16 w 0402	PD-0402	Yageo	RC0402FR-0753K6L Bottom of Form
	1	R362	Resistor, SMT 34.8K, 1%, 1/16W 0402	PD-0402	Rohm	MCR01MZPF3482
	1	R339	RES TCK FLM 10K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3

Table 4: PoE Controller Components

Block	Qty	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Controller	1	C29	CAP CER 1 nF 50V X7R 10% 0402 SMT	PD-0402	Murata	GRM36R71H102KA01L
	3	C82, C83, C89	CAP CER 0.1µF 10V X7R 10% 0402 SMT	PD-0402	Murata	GRM155R71C104KA88D
	1	C84	CAP CER 2.2nF 16V X7R 10% 0402 SMT	PD-0402	Yageo	CC0402KRX7R7BB222
	1	C86	CAP CRM 1µF 10V 10% X7R 0805 SMT	PD-0805	Phycomp	2222-240-15663
	1	D24	DIO 75V 200mA SOT23 SMT trr=4nSEC SWI	PD-SOT23	ON Semiconductor	BAS16LT1
	1	R76	RES 1M 62.5mW 1% 0603 SMT MTL FLM	PD-0603	Samsung	RC1608F1004CS
	3	R89, R100, R109	RES TCK FLM 49.9R 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF
	2	R115, R157	RES 0R 62.5mW 5% 0402 SMT MTL FLM	PD-0402	Vishay	CRCW0402-0R0 5% ET1 E3
	1	R120	RES TCK FLM 1.5K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-1K50 1% ET1 E3
	1	R132	RES TCK FLM 150R 1% 62.5mW 0402 SMT	PD-0402	Yageo	RC0402FR-07150RL
	3	R134, R297, R314	RES TCK FLM 10K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	1	R136	RES NET 4X51R 62.5mW 5% ISOL 1206 SMT	PD-YC16	CTS	742X083510JP
	1	R241	RES 10K 62.5mW 5% 1/4_1206 NET QUAD	PD-YC16	Vishay	CRA06S08310K0JTA

Block	Qty	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Controller	1	R274	RES TCK FLM 10R 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-0100-ELF
	1	R295	RES TCK FLM 100R 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-1000-ELF
	1	R308	RES TCK FLM 2.21R 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW04022R21FKED
	1	U2	PoE Controller	PD-TQFP-44	Microsemi	PD69000
	1	XL1	Resonator 9.83MHz SMT	MURATA-CSTCE-G	Murata	CSTCE9M83G52-B0

Table 5: PoE Manager Slave Components

Block	QTY*	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
PoE Manager Slave	1	C27	CAP ALU 47µF 100V 20% 8X11.5 105C P = 3.5mm T/H	D8H11_5F3_5	Rubycon	100PX47M T7 8X11.5
	2	C64, C65, C88	CAP CRM 100nF 100V 10% X7R 1206 SMT	PD-1206	AVX	12061C104KAT2A
	1	C66	CAP CRM 47nF 100V 10% X7R 0805 SMT	PD-0805	Murata	GRM40X7R473K100
	1	C91	CAP CRM 1µF 10V 10% X7R 0805 SMT	PD-0805	Phycomp	2222-240-15663
	3	C92, C93, C94	CAP CER 0.1µF 10V X7R 10% 0402 SMT	PD-0402	Murata	GRM155R71C104KA88D
	1	C113	CAP CER 1nF 50V X7R 10% 0402 SMT	PD-0402	Murata	GRM36R71H102KA01L
	1	D50	DIO DUAL 250V 225mA SMT SOT23 trr = 50nS SERIAL PH	PD-SOT23	Philips	BAV23S
	1	R218	RES TCK FLM 46.4K 125mW 1% 0805 SMT	PD-0805	EPCOS	B54102-A2463-F460
	1	R222	RES TCK FLM 22.6K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-22K6 1% ET1 E3
	1	R244	RES 0R 62.5mW 5% 0402 SMT MTL FLM	PD-0402	Vishay	CRCW0402-0R0 5% ET1 E3
	1	R313	RES TCK FLM 24.9K 1% 62.5mW 0402 SMT	PD-0402	Yageo	RC0402FR-0724K9
	1	R327	RES TCK FLM 49.9R 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF
	1	R329	RES TCK FLM 10K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	12	R365, R367, R369, R371, R373, R375, R377, R379, R381, R383, R385, R387	Res 500mΩ 1/2 W 200 ppm 1210	PD-1210	Venkel	LCR1210R500FSNT-MS**
	1	U1	12-port High PoE PSE Manager	PD-LQFP-80-HS-VIA	MICROSEMI	PD69012
	1	F49	FUSE 1.5A 63V V. FST BLO 1206 SMT	PD-1206	Bussmann	TR1/CC12PD-1.5A –R**

1. These quantities should be multiplied by the number of **PD69012** (four managers in this paper)

**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.

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Table 6: Front End Components

Block	Qty*	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
Front End	1	C1	CAP CRM 150nF 100V 10%^^X7R 1206 SMT	PD-1206	Syfer	1206J1000154KXT
	1	D1	DIO RECOV. REC 400V 1A SMA SILICON SMT	PD-SMA	Diodes Inc.	S1G
	1	F1	FUSE 1.5A 63V V. FST BLO 1206 SMT	PD-1206	Bussmann	TR1/CC12PD-1.5A –R**
	1	Q127	Transistor Fet N-Channel 100V			Refer to Power MOSFETs, page 7
	1	R10	RES TCK FLM 46.4K 125mW 1% 0805 SMT	PD-0805	EPCOS	B54102-A2463-F460

1. These quantities should be multiplied by the number of output ports (48 ports in this paper)

**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.

Table 7: Vport_out Components

Block	QTY *	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
Vport_out	1	J5	Pin Header Female 2 rows 48 Pins P1.27x1.27	CON-48P-F-1-SMD	CviLux	CBC1482M13M-2P

1. These quantities should be multiplied by the number of PD69012 (four managers in this paper)

Table 8: Control and Indication Isolation

Block	QTY	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
Control and Indication Isolation	3	R262, R264, R340	RES TCK FLM 1K 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-1001-E
	6	R263, R265, R334, R336, R337	RES TCK FLM 10K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	1	R266	RES TCK FLM 3.32K 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-3321-ELF
	1	R341	Resistor, 287Ω, 1%, 1/16W 0402	PD-0402	ASJ	CR10-2870FK

Table 9: Bill of Material for UART Communication Circuit (Host side 3_3V_iso = 3.3V)

Block	QTY	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
UART Isolation	2	C80, C97	CAP CER 0.1µF 10V X7R 10% 0402 SMT	PD-0402	Murata	GRM155R71C104KA88D
	2	R261, R338	RES TCK FLM 511R 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-5110-E
	2	R267, R335	RES TCK FLM 1K 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-1001-E
	2	U6, U7	IC optoisolator SMT 6 pin	PD-DIP6-SMD	Fairchild	H11L1SR2M

Table 10: Bill of Material for ESPI Communication Circuit (Host side 3_3V_iso = 3.3V)

Block	QTY	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
ESPI Isolation	2	R461, R462	RES TCK FLM 10K 1% 62.5mW 0402 SMT	PD-0402	Vishay	CRCW0402-10K0 1% ET1 E3
	1	R463	Resistor, 287 Ohm, 1%, 1/16W 0402	PD-0402	ASJ	CR10-2870FK
	2	C120, C121	CAP CER 0.1µF 10V X7R 10% 0402 SMT	PD-0402	Murata	GRM155R71C104KA88D
	1	U16	IC Dig.Isol VDD1-3ch/VDD2-1ch 1 Mbps 3.3/5V SO16	PD-SOW16	Analog Devices	ADUM1411ARWZ
	1	U17	IC OPTOISOLATOR MOC217	PD-SO8	Fairchild	MOC217 R2
	3	R464, R465, R466	RES TCK FLM 49.9R 1% 62.5mW 0402 SMT	PD-0402	Bourns	CR0402-FX-49R9-ELF

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Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 31 May. 08	-	Initial Release – Preliminary version
0.2 / 31 June. 08		General modifications as a result of developement
0.3 / 29 September. 08		General modifications as a result of developement
0.4 / 25 October. 08	Whole document	1. I²C interface supporting has been added. 2. xDisable_ports signal isolation has been changed from "Normaly Enable" to "Normaly Disable".
0.5 / 25 January. 09	Whole document	1. Application modified to support sense resistor value of 500mohm and 487mohm 2. Draft 3.0 modified to Draft 3.3
0.6 / 7 May. 09	"Front End" and "ESPI isolation" Bill of Material	1. C1 capacitor value changed from 47nF to 150nF. 2. R463 Resistor value changed from 1KΩ to 287Ω.
1.0 / 6 Oct. 09	Figure 8 Page 6	Adding a protection fuse Protection fuse for abnormal operating voltage
1.2 / 31 Jan. 11	Whole document	General editing/ Thermal design redone

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