More Resources in Low-Density Devices
- Lowest Power
- Proven Security
- Exceptional Reliability
IGLOO2 FPGAs

Microsemi IGLOO2 FPGAs Offer More Resources in Low-Density Devices with the Lowest Power, Proven Security, and Exceptional Reliability

IGLOO2 FPGAs are ideal for general purpose functions such as Gigabit Ethernet or dual-PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management, and secure connectivity. Microsemi FPGAs are used by customers in communications, industrial, medical, defense, and aviation markets.

Communications  Industrial  Defense  Automotive

IGLOO2 Features

More Resources in Low-Density Devices
• PCIe Gen2 support in 10K LE
• High-performance memory subsystem
• Highest I/O density

With Clear Advantages
• Lowest power
  • Reduces total power by up to 50%
  • 70 mW per 5G SERDES (PCIe Gen2)
• Proven security
  • Protection from overbuilding and cloning
  • Secure boot for FPGA and processors
• Exceptional reliability
  • SEU immune zero FIT Flash FPGA configuration
• Reliable safety-critical and mission-critical systems

Power as low as 7 mW standby, typical
• DPA-hardened, AES256, SHA256, on-demand NVM data integrity check
• SEU-protected/tolerant memories: eSRAMs, DDR bridges

IGLOO2 FPGA Architecture

IGLOO2 FPGAs offer 5K-150K LEs with a high-performance memory subsystem, up to 512 KB embedded flash, 2 × 32 KB embedded static random-access memory (SRAM), two direct memory access (DMA) engines, and two double data rate (DDR) memory controllers. Architecture highlights include:

- Up to 16× transceiver lanes
- PCIe Gen2, XAU/XGXS+, generic ePCS mode at 3.2G
- Up to 150K LEs, 5 Mbits SRAM, 4 Mbits eNVM
- Hard 667 Mbps DDR2/3 controllers
- Integrated DSP processing blocks

IGLOO2 FPGA

Up to 16 Lanes Multi Protocol SERDES

FPGA Fabric

Up to 150K Logic Elements

Multi-Standard GPIO
(1.2 V–3.3 V, LVDS, HSTL/SSTL)

Math Blocks
(AES256, SHA256, ECC)

SRAM – PUF

eSRAM_0

eSRAM_1

PDMA

HPDMA

FIC

AXI/AHB

DDR Bridge

High Performance Memory Subsystem

AXI/AHB

667 Mbps DDR Controller/PHY

667 Mbps DDR Controller/PHY

AXI/AHB

DDR Bridge

Fabric Interface Controller

Advanced Encryption Standard

High Performance Memory Subsystem

Advanced High-Performance Bus

Secure Hashing Algorithm

Advanced eXtensible Interface

10 Gbps Attachment Unit Interface

Double Data Rate

10 Gigabit Media Independent Interface

Elliptical Curve Cryptography

XGMII

Secure Flash

PCI Express

DDR3 Controller

Microsemi IGLOO® 2 FPGA
IGLOO2 FPGAs

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gpg.png

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<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>Low as 7 mW standby, typical</td>
</tr>
<tr>
<td>DPA-hardened</td>
<td>AES256, SHA256, on-demand NVM data integrity check</td>
</tr>
<tr>
<td>SEU-protected/tolerant</td>
<td>memories: eSRAMs, DDR bridges</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Standard Cell</th>
<th>FlashBased/SEU Immune</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMM_BLK</td>
<td>High Performance Memory Subsystem</td>
</tr>
<tr>
<td>FIC</td>
<td></td>
</tr>
<tr>
<td>AXI/SDRAM</td>
<td>Micro SRAM</td>
</tr>
<tr>
<td>AHB</td>
<td>Large SRAM</td>
</tr>
<tr>
<td>AHS</td>
<td>Math Blocks: 18(4x18)</td>
</tr>
<tr>
<td>APB</td>
<td>Math Blocks: 18(4x18)</td>
</tr>
<tr>
<td>AFI</td>
<td>AXI, XGXS</td>
</tr>
<tr>
<td>DDR</td>
<td>Direct Attach, XS, XS, XS, XS</td>
</tr>
<tr>
<td>AFI</td>
<td>Standard Cell/SEU Immune</td>
</tr>
<tr>
<td>ECC</td>
<td>Communications</td>
</tr>
<tr>
<td>ECC</td>
<td>Industrial</td>
</tr>
<tr>
<td>ECC</td>
<td>Defense</td>
</tr>
<tr>
<td>ECC</td>
<td>Automotive</td>
</tr>
</tbody>
</table>

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General Purpose Applications

PCIe 1G Control Plane
- PCIe Gen2 in 10K LE devices with I/O expansion

Bridging and Co-Processing
- SERDES to bridge CPRI, ADC/DAC

Secure Connectivity
- Best-in-class security data communications and anti-tamper
- Ultra-low static power for portability

Multi-Axis Motor Control
- Deterministic and secure multi-axis/ high-RPM solutions
- Motor control IP and development kit

Board Initialization
- PMBus, instant-on

Audio Processing, Storage, and Retrieval
- I2S-to-SPI bridge allows multiple audio recordings and playbacks
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IGLOO2 FPGA Features

High-Performance Memory Subsystem
- 64 KB embedded SRAM (eSRAM)
- Up to 512 KB embedded nonvolatile memory (nVM)
- One SPVC/COMM_BLK
- DDR bridge (2 port) with 64-bit A0 interface
- Non-blocking, multi-layer AHB bus matrix allowing multi-master scheme supporting 4 masters and 8 slaves
- Two AHBM/ABP interfaces to FPGA fabric (master/slave capable)

IGLOO2 FPGA Math Block
- Two digital controllers to offload data transactions
- 8-channel peripheral DMA (PDMA) for data transfer between soft peripherals in fabric and embedded eSRAMs, as well as support for memory-to-memory transfers
- eSRAM and external DDR memory for efficient data movement between embedded real-time memories

IGLOO2 FPGA Logic Element
- Programmable impedance
- Programmable amplitude
- Receiver features
- Programmable termination
- Programmable linear equalization
- Built-in system debug features
- PRBS/gain/sink
- Constant patterns
- Loopbacks

IGLOO2 FPGA SERDES
- Up to 16 lanes at up to 5 Gbps
- Dual-based reference clocks with single-lane rate granularity
- Tx and Rx PLLs programmable for each lane
- Reference clock is shared by groups of two lanes
- Transmitter features
- Programmable post-emphasis

IGLOO2 FPGA SERDES
- Programmable capacity
- Programmable rate
- Programmable baud rate
- Built-in system debug features
- Constant patterns
- Loopbacks

IGLOO2 Evaluation Kit
- Gives designers access to IGLOO2 FPGAs that offer leadership in I/O density, security, reliability, and lowpower for mainstream applications
- Supports industry-standard interfaces including Gigabit Ethernet, USB 2.0 OTG, SPI, I2C, and UART
- Can be powered by a 12 V power supply or the PCIe connector, and includes a FlashPro4 programmer
- Board features
  - IGLOO2 FPGA in the FGG484 package
  - JTAG/SPI programming interface
  - Gigabit Ethernet PHY and RJ45 connector
  - USB 2.0 OTG interface connector
  - 1 GB LPDDR, 64 MB SPI flash
  - Headers for 2C, UART, SPI, GPIOs
  - x1 Gen2 PCIe edge connector
  - Tx/Rx/VcK SMP pairs

Design Resources

Libero® SoC Design Software
Microsemi’s Libero SoC design suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adapt development tools that are used for designing with Microsemi’s power-efficient flash-based IGLOO2 devices. The suite integrates industry-standard Synopsys Simplify Pro synthesis and Mentor Graphics ModelSim simulation with best-in-class constraints management, debug capabilities, timing analysis, power analysis, secure production programming, and push button design flow.

This comprehensive suite features an intuitive design flow with GUI wizards to guide the design process. Its easy-to-adapt single-click synthesis to programming flow integrates industry-standard third-party tools, a rich IP library of DirectCores and CompanionCores, and supports complete reference designs and development kits.

http://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-socdwnloads

IGLOO2 FPGA Logic Element
- A fully permutable 4-input LUT
- A dedicated carry chain based on the carry look-ahead technique
- A separate flip-flop that can be used independently from the LUT

Clock-gated input and output registers for power optimizations

Intellectual Property
Microsemi enhances your design productivity by providing an extensive suite of proven and optimized IP cores for use with Microsemi FPGAs. Our extensive suite of IP cores covers all key markets and applications. Our cores are organized as either Microsemi-developed DirectCores or third-party-developed CompanionCores. Most DirectCores are available for free within our Libero tool suite and include common communications interfaces, peripherals, and processing elements.

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- 64 KB embedded SRAM (eSRAM)
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- One SPI/COMM_BLK
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- Two AHB/APB interfaces to FPGA fabric (master/slave capable)
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- Tx and Rx PLLs programmable for each lane
- Reference clock is shared by groups of two lanes
- Transmitter features
  - Programmable pre/post-emphasis
  - Programmable timing
  - Programmable equalization
  - Programmable loopback
- Receiver features
  - Programmable programmable
  - Programmable loopback

IGLOO2 FPGA Math Block
- High-performance and power-optimized multiplication operations
- Supports 16x16-bit multiplication (individual)
- Supports 17x17 unsigned multiplication
- Supports dot product: the multiplier
- Supports loopback capability
- Built-in system debug features
- Programmable SDMA, and supports complete reference designs and development kits.

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CompanionCore™

Functionality DirectCore Examples
Connectivity UART, 65535, 422/64, RS232/232
DSP CIC, FFT, FIR, Cordic, RS
Memory Controller FIFO, DDR, QDR, DDR, MemCtrl, MMC
Processor 8048, 8051, ARM926
Ethernet ML, RJ45, GM, XGMII
Security DES, 3DES, AES, SHA

Functionality CompanionCores Examples
Connectivity CAN, CANFD, PCIe, VME
DSP FFT, JPEG, RS, DVBMOD
Memory Controller SRAM/DRAM, Flash, SD
Processor 80186, 80188, LEON2, LEON3
Security SHA, ARC4, RNG, ZUC, AES, SHA, 802.1ae (MACsec)
# IGLOO2 FPGA Product Family

<table>
<thead>
<tr>
<th>IGLOO2 Devices</th>
<th>Features</th>
<th>M2GL005</th>
<th>M2GL010</th>
<th>M2GL025</th>
<th>M2GL050</th>
<th>M2GL060</th>
<th>M2GL090</th>
<th>M2GL150</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Logic/DSP</strong></td>
<td>Maximum logic elements (4LUT + DFF)</td>
<td>6,060</td>
<td>12,084</td>
<td>27,696</td>
<td>56,340</td>
<td>56,520</td>
<td>86,184</td>
<td>146,124</td>
</tr>
<tr>
<td></td>
<td>Math blocks (18x18)</td>
<td>11</td>
<td>22</td>
<td>34</td>
<td>72</td>
<td>72</td>
<td>84</td>
<td>240</td>
</tr>
<tr>
<td></td>
<td>PLLs and CCCs</td>
<td>2</td>
<td>6</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SPI/HPDMA/PDMA</td>
<td>1 each</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fabric interface controllers (FICs)</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Data security</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>eNVM (KBytes)</td>
<td>128</td>
<td>256</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LSRAM 18K Blocks</td>
<td>10</td>
<td>21</td>
<td>31</td>
<td>69</td>
<td>109</td>
<td>236</td>
<td></td>
</tr>
<tr>
<td></td>
<td>uSRAM 1K Blocks</td>
<td>11</td>
<td>21</td>
<td>34</td>
<td>72</td>
<td>112</td>
<td>240</td>
<td></td>
</tr>
<tr>
<td></td>
<td>eSRAM (KBytes)</td>
<td>64</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total RAM (Kbits)</td>
<td>703</td>
<td>912</td>
<td>1104</td>
<td>1826</td>
<td>2586</td>
<td>5000</td>
<td></td>
</tr>
<tr>
<td><strong>High speed</strong></td>
<td>DDR Controllers (count x width)</td>
<td>1 x 18</td>
<td>2 x 36</td>
<td>1 x 18</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>PCIe endpoints</td>
<td>0</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>4</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MSIO (3.3 V)</td>
<td>115</td>
<td>123</td>
<td>157</td>
<td>139</td>
<td>271</td>
<td>309</td>
<td>292</td>
</tr>
<tr>
<td><strong>User I/O</strong></td>
<td>MSIO (2.5 V)</td>
<td>28</td>
<td>40</td>
<td>62</td>
<td>40</td>
<td>106</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DDRIO (2.5 V)</td>
<td>66</td>
<td>70</td>
<td>176</td>
<td>76</td>
<td>176</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total user I/Os</td>
<td>209</td>
<td>233</td>
<td>267</td>
<td>377</td>
<td>387</td>
<td>425</td>
<td>574</td>
</tr>
<tr>
<td><strong>Grades</strong></td>
<td>Commercial (C), Industrial (I), Military (M)</td>
<td>C, I</td>
<td>C, I, M</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Total logic may vary based on utilization of DSP and memories in your design. Please see the IGLOO2 Fabric UG for details.*

*Feature availability is package dependent.*

## I/Os per Package

<table>
<thead>
<tr>
<th>Package Options</th>
<th>Package type</th>
<th>FCS(G)325</th>
<th>VF(G)256</th>
<th>FCS(G)536</th>
<th>VF(G)400</th>
<th>FCV(G)484</th>
<th>TQ(G)144</th>
<th>FG(G)484</th>
<th>FG(G)676</th>
<th>FG(G)896</th>
<th>FC(G)1152</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pitch (mm)</strong></td>
<td>0.5</td>
<td>0.8</td>
<td>0.5</td>
<td>0.8</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Length x width (mm)</strong></td>
<td>11 x 11</td>
<td>14 x 14</td>
<td>16 x 16</td>
<td>17 x 17</td>
<td>19 x 19</td>
<td>20 x 20</td>
<td>23 x 23</td>
<td>27 x 27</td>
<td>31 x 31</td>
<td>35 x 35</td>
<td></td>
</tr>
<tr>
<td><strong>Device</strong></td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td>I/O Lanes</td>
<td></td>
</tr>
<tr>
<td>M2GL005 (S)</td>
<td>161</td>
<td>171</td>
<td>84</td>
<td>209</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL010 (S/T/TS)</td>
<td>138</td>
<td>195</td>
<td>84</td>
<td>233</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL025 (T/TS)</td>
<td>180</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL050 (T/TS)</td>
<td>200</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL060 (T/TS)</td>
<td>200</td>
<td>207</td>
<td>267</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL090 (T/TS)</td>
<td>180</td>
<td>4</td>
<td>267</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2GL150 (T/TS)</td>
<td>293</td>
<td>4</td>
<td>248</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Highlighted devices can migrate vertically in the same package*