RTAXS EDAC-RAM Single Event Upset Test Report

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SUMMARY

This report focuses on the SEU (single event upset) effect in the EDAC-RAM in RTAX-S. The results come from heavy ion beam tests at BNL and TAMU. To further study the ECC and scrubbing function, probability theory and single-bit SEU measured previously are used to derive the EDAC-RAM SEU errors to compare with the directly tested results. The major conclusions include:

- The ECC (error correcting code) and scrubbing function can effectively harden the EDAC-RAM, and reduce the SEU rate to be less than 1×10^{-10} upset/bit-day.
- For EDAC-RAM without scrubbing and with low scrubbing rate conditions, the derived SEU corroborates with the directly tested SEU.
- The scrubbing function generally operates as expected for different clock frequencies.
- Background noise and single event transient (SET) are speculated as the probable causes for inconsistence between the derived SEU and tested SEU for high scrubbing rate conditions.

I. INTRODUCTION

The embedded RAM in the RTAXS family is hardened by an ECC (error correcting code) technique. Shortened Hamming codes for detecting 2 error-bits and correcting 1 error-bit are implemented for words of 8-bit, 16-bit, and 32-bit widths. This hardened RAM is called EDAC (error detection and correction)-RAM. A scrubbing mechanism is also implemented for EDAC-RAM to reduce the SEU rate for long-term data storage. This scrubbing refreshes the stored Hamming codes so that in a word an 1 error-bit condition never stays long enough to suffer another bit-upset and become an un-correctable 2 error-bits condition. Based on how long the data is stored in the EDAC-RAM, user can determine how often to scrub the EDAC-RAM. For implementing EDAC-RAM, Actel website (www.actel.com) provides an useful reference: "Using EDAC RAM for Rad-Tolerant RTAX-S FPGAs and Axcelerator FPGAs."

This report combines the results of tests at BNL and TAMU. The test objective is to find the SEU rate and verify the hardening of EDAC-RAM. Because the ground test uses fluxes many orders of magnitude larger than the fluxes in space, the scrubbing has to be turned on to observe the ECC in operation; without ECC, scrubbing alone cannot reduce the SEU errors.

II. DEVICE UNDER TEST

Table I and II lists the DUT parameters for BNL testing and TAMU testing respectively.

Table I BNL DUT Parameters

Device	RTAX2000S
Package	CQ352
Foundry	UMC
Technology	0.15 µm CMOS
Die Lot Number	NA
Date Code	NA
Quantity Tested	1
Serial Number	AXS1
IO Configuration	LVTTL
Design	RT_EDAC_RAM

Table II TAMU DUT Parameters

Device	RTAX1000S
Package	CQ352
Foundry	UMC
Technology	0.15 µm CMOS
Die Lot Number	D02F41
Date Code	0409
Quantity Tested	3
Serial Number	35203, 35238, 35433
IO Configuration	LVTTL
Design	RT_EDAC_RAM

II. TEST METHODS

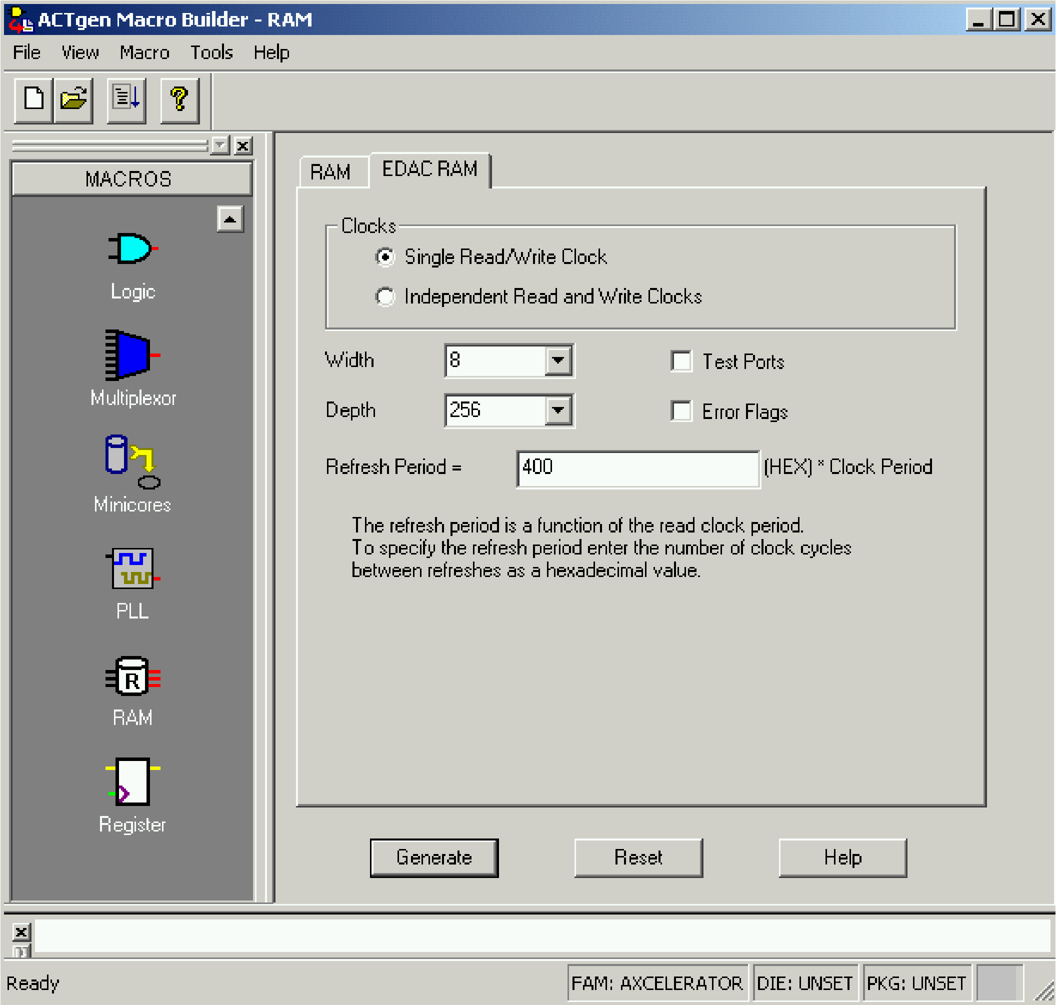
The general guidelines for single event effects (SEE) testing can be found in two documents: ASTM standard F1192M-95, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation on Semiconductor Devices," and JEDEC standard JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation."

A. *Heavy Ion Beam Radiation*

The BNL testing uses 210 MeV-Cl and 279 MeV-Br beams. The TAMU testing uses 1,077 MeV-Ag and 1,253 MeV-Xe beams. Tilting the DUT at an angle relative the incident beam achieves an effective LET for each run. Radiation details for each run are logged in Table III, and IV.

B. *Test Logic Design*

The test design is shown in Figure 1, in which the ACTgen-Macro-Builder builds an EDAC-RAM of 8-bit width and 256 depths with the refresh period of 2^{10} x Clock-Period for scrubbing. The design is the same for both the BNL and TAMU tests.



Clocks
● Single Read/Write Clock
○ Independent Read and Write Clocks

Width 8
Depth 256
☐ Test Ports
☐ Error Flags

Refresh Period = 400 (HEX) * Clock Period

The refresh period is a function of the read clock period. To specify the refresh period enter the number of clock cycles between refreshes as a hexadecimal value.

Ready | FAM: AXCELERATOR | DIE: UNSET | PKG: UNSET

Figure 1: Showing the EDAC-RAM built by ACTgen-Macro-Builder.

III. TEST RESULTS AND DISCUSSIONS

A. *Experimental Data Versus Derived Data*

Table III shows the testing parameters and raw data for the BNL testing, and Table IV shows those for the TAMU testing. In these Tables, for the same radiation condition the SEU errors for a run with scrubbing-on are much lower than the SEU errors for a Run with scrubbing-off; this clearly demonstrates the efficacy of the ECC and scrubbing function. Although the TAMU testing uses 10% less bias voltage than the bias for the BNL testing, there is no apparent bias dependence for the data, and the treatment in the following will ignore this bias difference.

To further investigate the ECC and scrubbing function, the SEU induced word-upsets for the EDAC-RAM are derived from the SEU data for a single-bit RAM by probability theory. The derived word-upsets is then compared with the direct experimental data to gain more information from the testing results. First, a scrubbing-off run is considered. The testing results of a single-bit acquire the saturation cross-section as 3.5 x 10^{-8} cm^2. Thus for a typical run to irradiate to total fluence of 1 x 10^7 ions/cm^2, the upset per bit is:

$$3.5\times10^{-8}(\text{cm}^2)\times10^7(\text{cm}^{-2}) = 0.35(\text{upsets}) \cong \text{Probability}(\boldsymbol{p}).$$

Since this upset number is well less than 1, it approximately equals to the probability for an upset to occur. Assuming no multiple bit-upsets by a single ion strike and using "hard-error" model, the number of word-upsets for a block of EDAC-RAM with 256 words of 8-bit width are:

$$256\times\{1-[(1-\boldsymbol{p})^{12}+12(1-\boldsymbol{p})^{11}\boldsymbol{p}]\} = 245\ .$$

Notice that each 8-bit word in EDAC-RAM actually occupies 12 bits in the physical memory cells; only more than one bit-upset in the 12 bits produces an EDAC-RAM word-upset. This derived number is very close to the experiment SEU data for LET ≥ 37.45 MeV•cm^2/mg, when the saturation cross-section applies.

For a run with scrubbing-on and using a 2 MHz clock, the refresh period is:

$$2^{10}\times\frac{1}{2(MHz)} = 512\mu s\ .$$

So a single bit upset in this period for high-LET ion strike with a flux of 1 x 10^5 ions/cm^2•sec is:

$$3.5\times10^{-8}(\text{cm}^2)\times10^5(\text{cm}^{-2}\bullet\text{sec}^{-1})\times512\times10^{-6}(\text{sec}) = 1.792\times10^{-6}(\text{upsets}) \cong \text{Probability}(\boldsymbol{p})$$

Again, since this number is significantly less than 1, it approximately equals to the probability (**p**) of an upset in this refresh period. Then the word-upsets for 256x8-bit EDAC-RAM in this refresh period are:

$$256\times\{1-[(1-\boldsymbol{p})^{12}+12(1-\boldsymbol{p})^{11}\boldsymbol{p}]\} = 5.43\times10^{-8}\ .$$

Finally, the word-upsets for this block of EDAC-RAM for total fluence of 1 x 10^7 ions/cm^2 are:

$$5.43\times10^{-8}\times\frac{100}{512\times10^{-6}} = 1.06\times10^{-2}\ .$$

This derived word-upset number is much lower than the SEU data obtained from direct experiment, for example, comparing the derived word-upset with the data of Run 842 or Run 844 in Table III. However, there is no definite explanation for this inconsistency at this moment. Previous experimental results indicate no multiple bit-upsets, by a single ion strike, to occur in a word of any width. Remaining probable causes are: single event transient (SET) induced upset during scrubbing, and testing noise, which limits the detection resolution so that in each run an one-error is almost indistinguishable to a zero-error.

Table III BNL Testing Parameters and Raw Data

BNL Run	DUT	Bias (V) V_{CCI}/V_{CCA}	Ion	LET MeV•cm^2/mg	Tilt	Flux Ions/cm^2/s	Fluence Ions/cm^2	Word-Upset	Comments
828	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+07	221	Scrub off
829	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+06	14	Scrub off
830	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+07	221	Scrub off
831	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+07	215	Scrub off
832	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+07	0	Bad data
833	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+07	216	Scrub off
834	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	19	Scrub off
835	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	10	Scrub off
836	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	16	Scrub off
837	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	17	Scrub off
838	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	14	Scrub off
839	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	0	Aborted, bad data
840	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	0	Aborted, bad data
841	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+06	1	Scrub on 2MHz
842	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+07	6	Scrub on 2MHz
843	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+07	209	Scrub off
844	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+05	1.00E+07	5	Scrub on 2MHz
845	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+07	214	Scrub off
846	AXS1	3.3/1.5	Br-81	37.45	0	1.00E+04	1.00E+07	3	Scrub on 2MHz
847	AXS1	3.3/1.5	Br-81	52.97	45	1.00E+04	1.00E+07	225	Scrub off
848	AXS1	3.3/1.5	Br-81	52.97	45	1.00E+04	5.00E+06	5	Scrub on 2MHz
849	AXS1	3.3/1.5	Br-81	43.24	30	1.00E+04	5.00E+06	151	Scrub off
850	AXS1	3.3/1.5	Br-81	43.24	30	1.00E+04	5.00E+06	1	Scrub on 2MHz
901	AXS1	3.3/1.5	Cl-35	11.44	0	1.00E+05	1.00E+07	130	Scrub off
902	AXS1	3.3/1.5	Cl-35	11.44	0	1.00E+05	1.00E+07	0	Scrub on 2MHz
903	AXS1	3.3/1.5	Cl-35	13.21	30	1.00E+05	1.00E+07	153	Scrub off
904	AXS1	3.3/1.5	Cl-35	13.21	30	1.00E+05	1.00E+07	1	Scrub on 2MHz
905	AXS1	3.3/1.5	Cl-35	16.18	45	1.00E+05	1.00E+07	166	Scrub off
906	AXS1	3.3/1.5	Cl-35	16.18	45	1.00E+05	1.00E+07	1	Scrub on 2MHz
907	AXS1	3.3/1.5	Cl-35	17.79	50	1.00E+05	1.00E+07	176	Scrub off
908	AXS1	3.3/1.5	Cl-35	17.79	50	1.00E+05	1.00E+07	0	Scrub on 2MHz

Table IV TAMU Testing Parameters and Raw Data

TAMU Run	DUT	Bias (V) V_{CCI}/V_{CCA}	Ion	LET MeV•cm^2/mg	Tilt	Flux Ions/cm^2/s	Fluence Ions/cm^2	Word-Upset	Comments
32	35203	3.0/1.35	Ag	44.4	0	5.00E+04	1.00E+06	15	Scrub off
33	35203	3.0/1.35	Ag	44.4	0	5.00E+04	1.00E+06	0	Scrub on 2MHz
34	35203	3.0/1.35	Ag	51.3	30	5.00E+04	1.00E+06	20	Scrub off
35	35203	3.0/1.35	Ag	51.3	30	5.00E+04	1.00E+06	2	Scrub on 2MHz
36	35203	3.0/1.35	Ag	62.8	45	5.00E+04	1.00E+06	29	Scrub off
37	35203	3.0/1.35	Ag	62.8	45	5.00E+04	1.00E+06	0	Scrub on 2MHz
38	35203	3.0/1.35	Ag	62.8	45	5.00E+04	5.00E+06	176	Scrub off
39	35203	3.0/1.35	Ag	62.8	45	5.00E+04	5.00E+06	1	Scrub on 2MHz
40	35203	3.0/1.35	Ag	44.4	0	5.00E+04	5.00E+06	150	Scrub off
41	35203	3.0/1.35	Ag	44.4	0	5.00E+04	5.00E+06	1	Scrub on 2MHz
42	35203	3.0/1.35	Ag	44.4	0	5.00E+04	5.00E+06	2	Scrub on 100kHz
43	35203	3.0/1.35	Ag	44.4	0	5.00E+04	5.00E+06	5	Scrub on 10kHz
44	35203	3.0/1.35	Ag	44.4	0	5.00E+04	5.00E+06	8	Scrub on 1kHz
45	35203	3.0/1.35	Ag	44.4	0	5.00E+04	5.00E+06	54	Scrub on100Hz
46	35238	3.0/1.35	Ag	44.4	0	5.00E+04	1.00E+06	21	Scrub off
47	35238	3.0/1.35	Ag	44.4	0	5.00E+04	1.00E+06	0	Scrub on 2MHz
48	35238	3.0/1.35	Ag	62.8	45	5.00E+04	1.00E+06	28	Scrub off
49	35238	3.0/1.35	Ag	62.8	45	5.00E+04	1.00E+06	0	Scrub on 2MHz
50	35238	3.0/1.35	Ag	51.3	30	5.00E+04	1.00E+06	26	Scrub off
51	35238	3.0/1.35	Ag	51.3	30	5.00E+04	1.00E+06	0	Scrub on 2MHz
52	35433	3.0/1.35	Ag	51.3	30	5.00E+04	1.00E+06	16	Scrub off
53	35433	3.0/1.35	Ag	51.3	30	5.00E+04	1.00E+06	0	Scrub on 2MHz
54	35433	3.0/1.35	Ag	62.8	45	5.00E+04	1.00E+06	31	Scrub off
55	35433	3.0/1.35	Ag	62.8	45	5.00E+04	1.00E+06	0	Scrub on 2MHz
56	35433	3.0/1.35	Ag	44.4	0	5.00E+04	1.00E+06	20	Scrub off
57	35433	3.0/1.35	Ag	44.4	0	5.00E+04	1.00E+06	2	Scrub on 2MHz

B. SEU Cross Section

Although noises probably cause experimentally measured word-upsets in the EDAC-RAM to be higher than the real number, the data can be used to set the worst-case boundary for SEU rates predictions. The extracted SEU cross-section is extracted from Table III and plotted in Figure 2. Also shown in this Figure is a curve fit using Weibull parameters: $LET_{TH} = 30$ MeV•cm^2/mg, width = 10 MeV•cm^2/mg, shape = 1.5, and saturation cross-section = 3.91×10^{-9} cm^2. Then using these Weibull parameters and the SpaceRad-4.5 simulator, with other parameters set as: active-volume depth to 0.15 µm, and funnel depth to 0.3 µm, the word-upset rate in 100 mil Al shield and GEO-MIN environment is obtained as 2.55×10^{-11} upset/word-day. For 16-bit and 32-bit words, the word-upset rate in the same environment can be derived by combinatorial calculation as 1.57×10^{-10} upset/word-day and 4.18×10^{-10} upset/word-day respectively. Notice that the actually physical bit widths for 8-bit, 16-bit and 32-bit word are 12, 29 and 47 respectively.

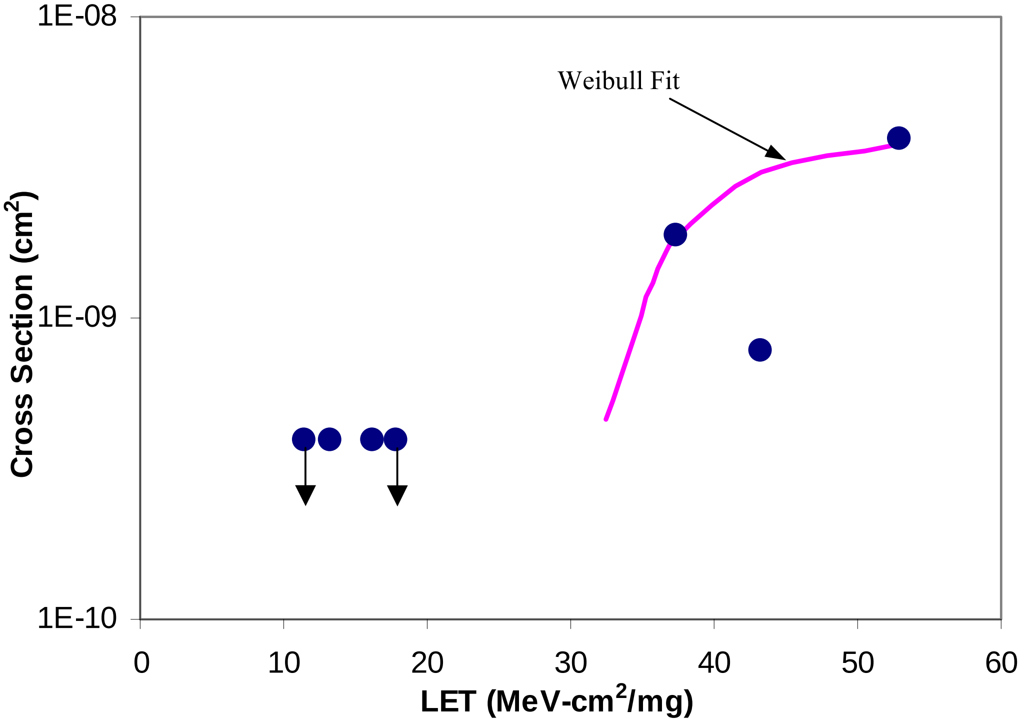


Figure 2: Plot showing the SEU cross-section per word versus LET for EDAC-RAM, the data points are those runs with scrubbing-on in Table III. The curved line is the Weibull fitting with parameters: $LET_{TH} = 30$ MeV/(mg/cm^2), width = 10 MeV/(mg/cm^2), shape = 1.5, and saturation cross-section = 3.91×10^{-9} cm^2.

Figure 3 plots the SEU cross section per word extracted from Table IV. These data are more scattered due to the lower total fluence. Nevertheless, they are consistent with the data in Figure 2.

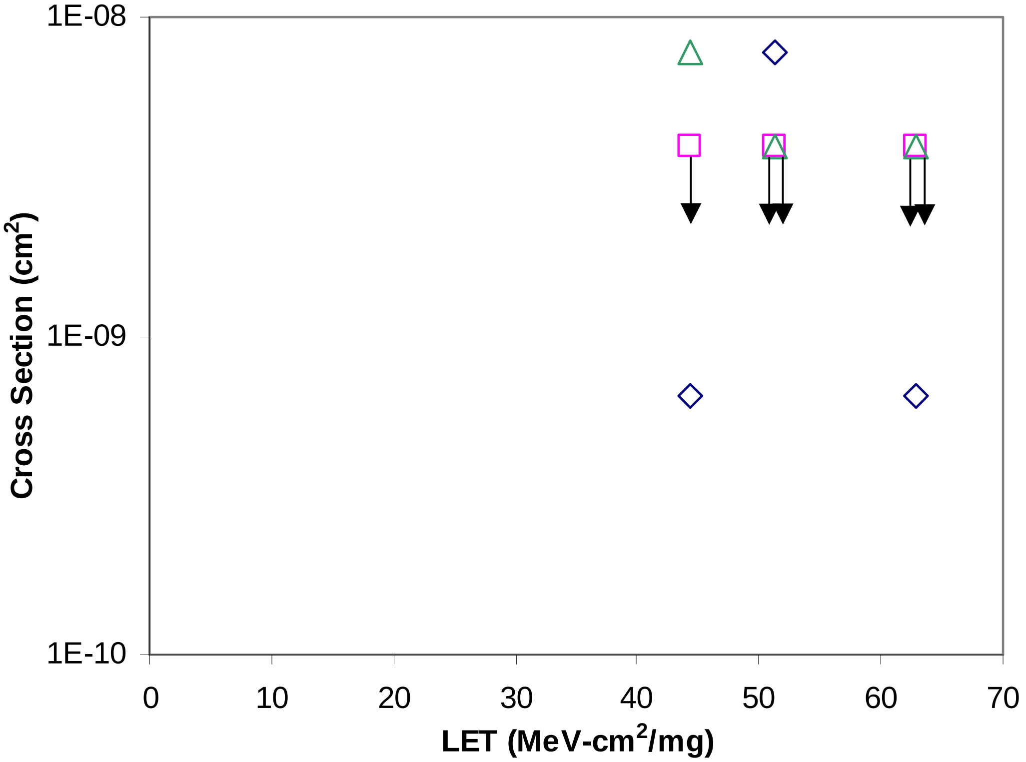


Figure 3: Plot showing the SEU cross-section per word versus LET for EDAC-RAM, the data points come from those runs using 2 MHz scrubbing in Table IV.

C. EDAC-RAM SEU Rate dependence on Scrubbing Rate

To further prove the efficacy of the scrubbing function, the clock frequency is varied to vary the refresh period for observing the SEU dependence on the scrubbing-rate dependence. Runs 40 to 45 in Table IV show the raw data; the word-upset with respect to the scrubbing rate, or refresh period is shown in Table V. As expected, the word-upsets exhibit a clear dependence on the refresh period, and word-upsets increase with the refresh period. Also tabulated are word-upsets derived from the experimental single bit-upset data. While for higher refresh periods the corroboration is very good, for lower refresh periods the results obtained from the direct experiment are higher than the derived results. As mentioned in section IIIA, the noise and SET induced error are speculated as the probable causes.

Table V SEU Dependence on Scrubbing Rate

Clock Freq	Refresh Period	Word-Upset	Derived
2MHz	512µs	1	0.00265
100kHz	10ms	2	0.0529
10kHz	0.1s	5	0.529
1kHz	1s	8	5.29
100Hz	10s	54	52.9
No Scrub	100s	150	166