TOTAL IONIZING DOSE TEST REPORT

No. 04T-RTSX32S(U)-D110A1
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si) after room temperature annealing
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 60 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 15 days room temperature annealing: average I_{CCA} = 102 mA, and average I_{CCI} = 71.4 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) for 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement provides lower noise, better accuracy and more flexibility. The bench measurement samples pins for some measurements (e.g. threshold voltage measurement). However, since the tolerance is determined by the most degraded parameter, which is I_{CC} or propagation delay, sampling the pins for measuring non-critical parameters is appropriate.

A. Device Under Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

|	
Part Number	RTSX32S(U)
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 μm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	D110A1
Quantity Tested	5
Serial Number	40678, 40693, 40699, 40724, 40777
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method
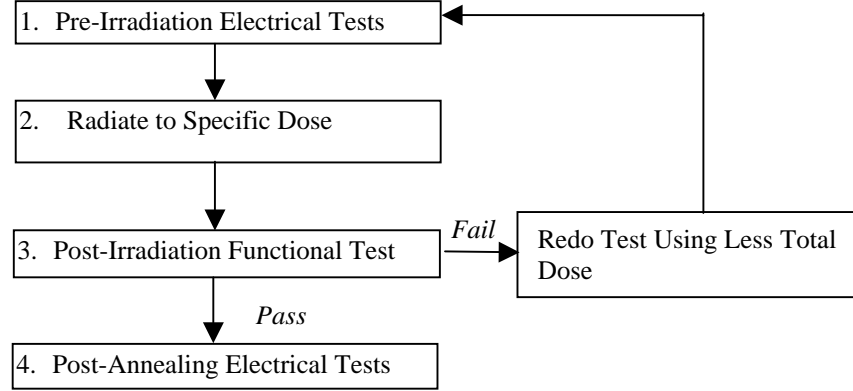
Figure 1   Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs are biased annealed for 15 days after the 100-krad (Si) irradiations.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 616 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 512 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 6 basically show the radiation-induced leakage current. For every DUT, the logic array current, I_{CCA} exhibits a transition just above 60 krad. This transition is due to the temporary shutdown of the charge pump because the radiation-induced leakage current overloads the charge pump. The array logic changes to another state and causes the I_{CCA} transition. However, the temporary showdown of the charge pump is only a testing artifact because a short room temperature annealing for few hours recovers the charge pump.

By technicality, TM1019 doesn't allow the irradiation after functional failure. But the shutdown of charge pump does not vary the testing validity in this case because the device logic state is well defined even after the shutdown of the charge pump; every CMOS circuit in the device is at a fixed state and irradiated at the power supply bias. Nevertheless, DUTs 40699, 40724 and 40777 are irradiated in two steps: the first step goes to 60 krad, and then the charge pump is verified to be functional; the second step continues the irradiation to 100 krad. The time separation between the end of the first step and the start of the second step is about 5 min. After 100 krad and few hours of room temperature annealing, the charge pump in every DUT is recovered; then DUTs are biased and annealed at room temperature for 15 days.

The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	I_{CCA} (mA)		I_{CCI} (mA)	
	Post-rad	Post-ann	Post-rad	Post-ann
40678	273	116	214	75
40693	271	88	216	59
40699	156	104	247	88
40724	253	100	203	59
40777	300	102	228	76

An empirical equation is used to extract the total dose tolerance. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA is obtained from the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are in-flux currents when total dose equals to γ. Using the-worst-case in-flux currents degradation, which is DUT 40777 (Figure 6), the tolerance ($\gamma_{critical}$) is obtained as approximately 60 krad (Si). This equation produces a conservative tolerance because the process of a high-dose-rate irradiation plus annealing produces an I_{CC} higher than the I_{CC} produced by a consistent low-dose-rate irradiation process.
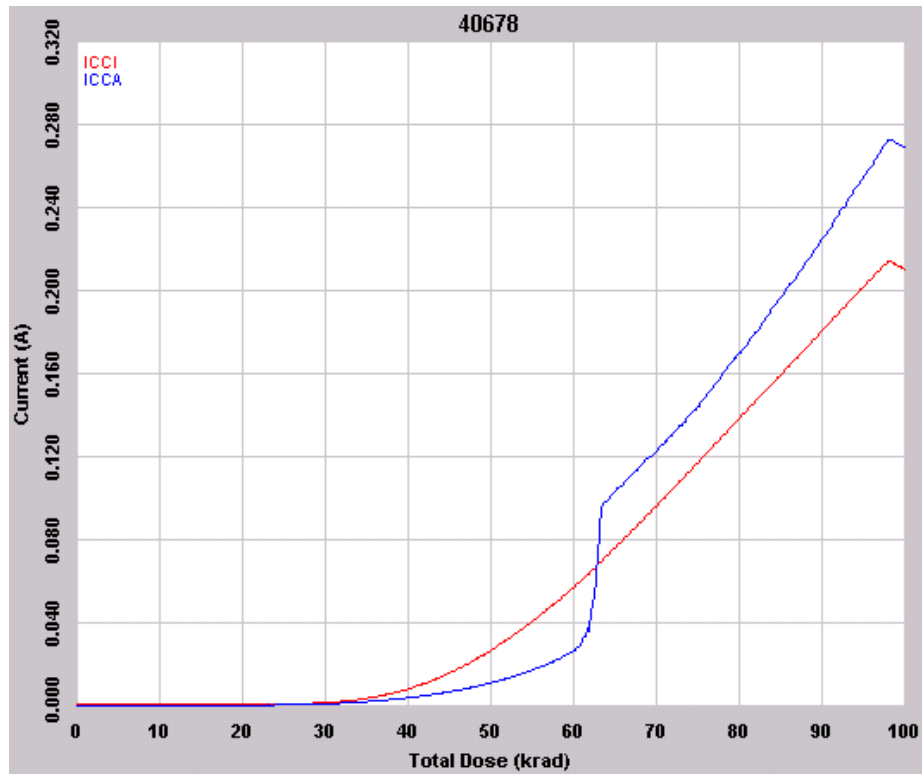
Figure 2   DUT 40468 in-flux I_{CCA} and I_{CCI}, I_{CCA} shows a transition near 62 krad that indicates the shutdown of the charge pump.
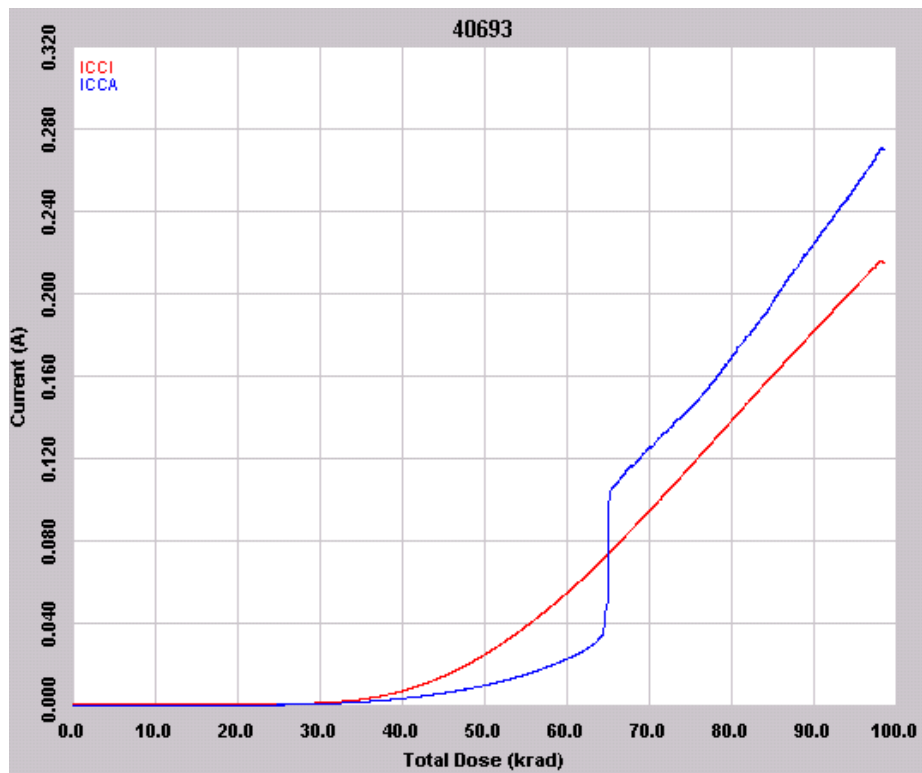

Figure 3   DUT 40693 in-flux I_{CCA} and I_{CCI}, I_{CCA} shows a transition near 65 krad that indicates the shutdown of the charge pump.
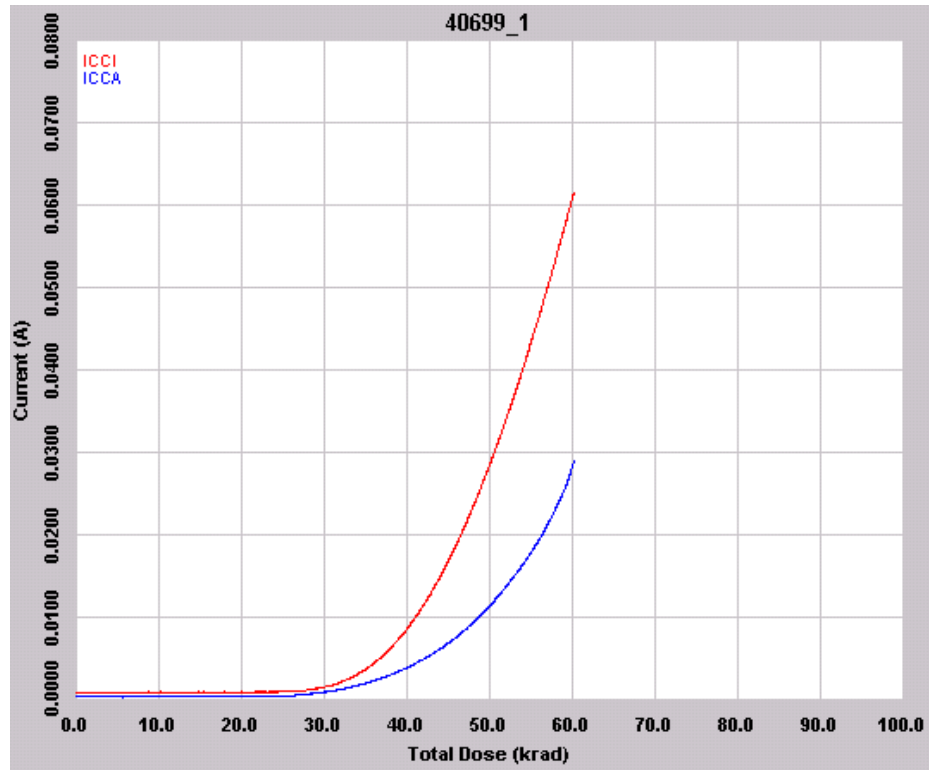
4

Figure 4(a)   DUT 40699 in-flux I_{CCA} and I_{CCI} for irradiation from 0 krad to 60 krad
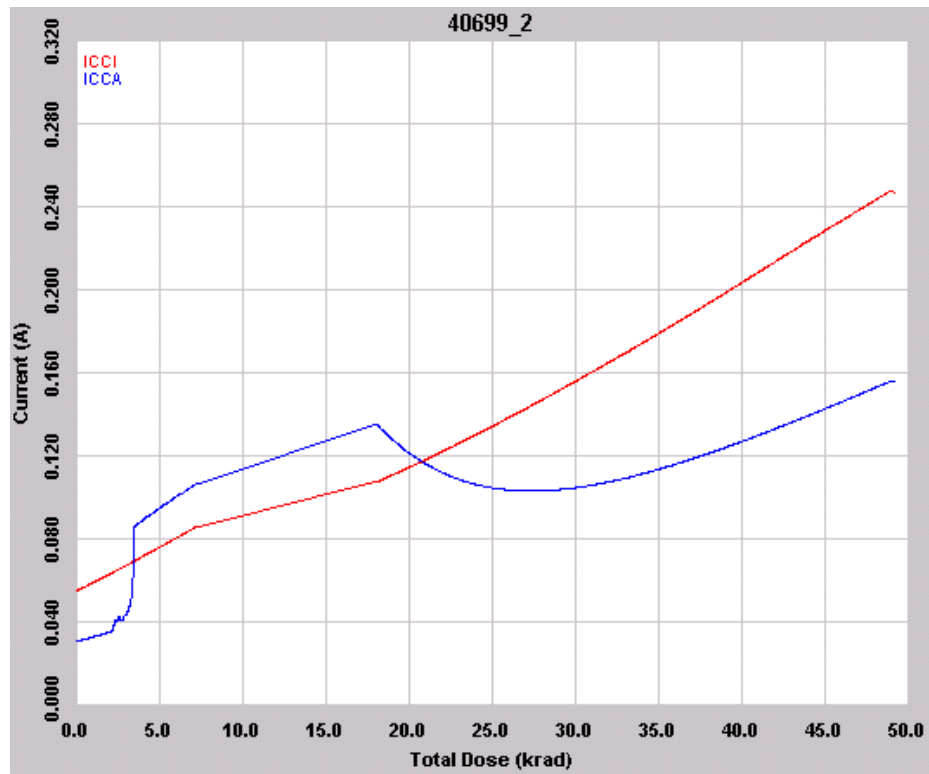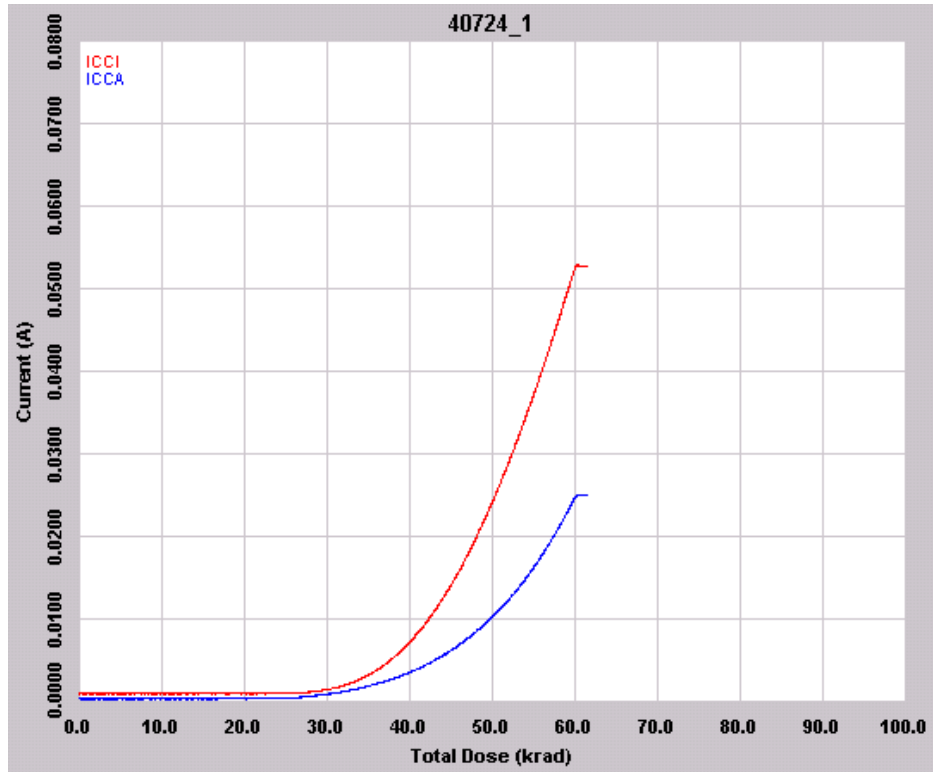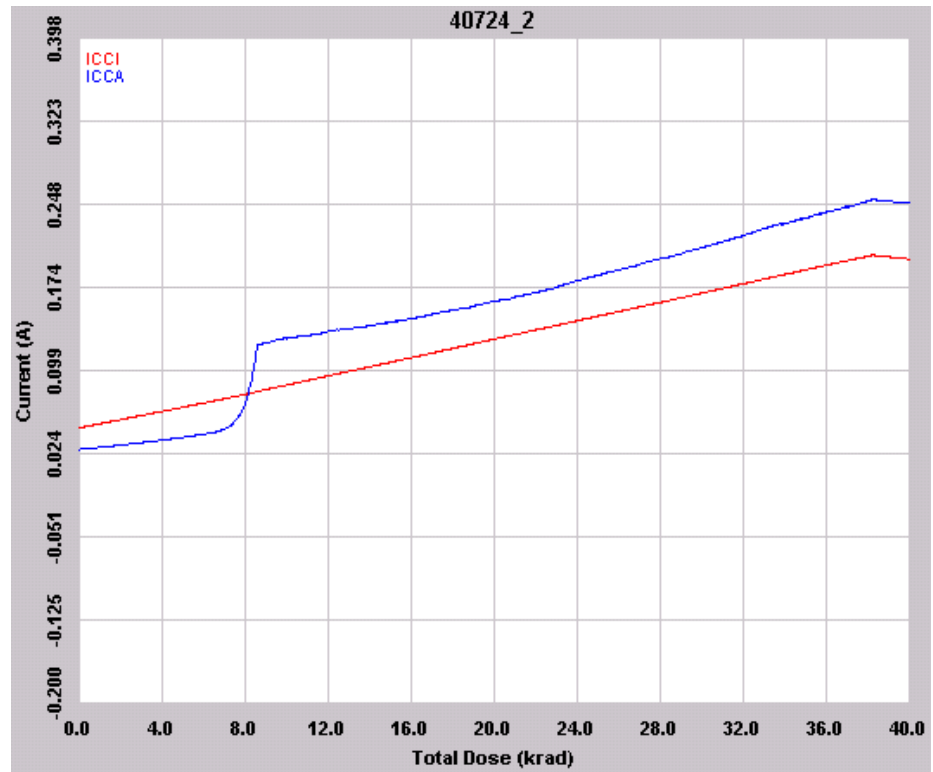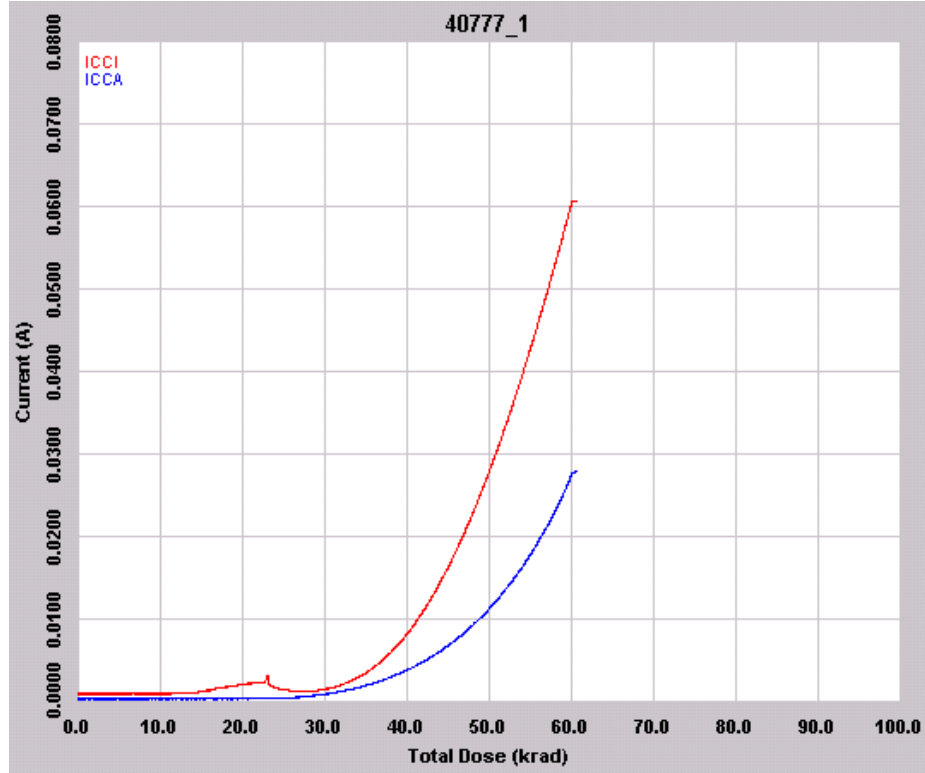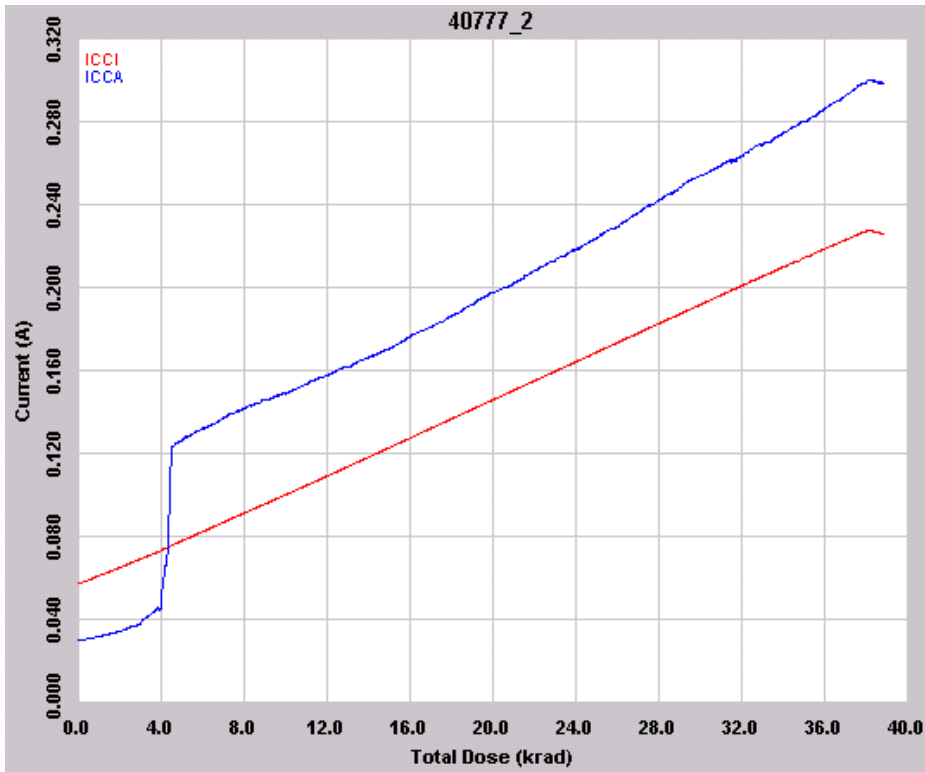

Figure 4(b)   DUT 40699 in-flux I_{CCA} and I_{CCI} for irradiation from 60 krad to 110 krad, I_{CCA} shows a transition near 63 krad that indicates the shutdown of the charge pump.

Figure 5(a)   DUT 40724 in-flux I_{CCA} and I_{CCI} for irradiation from 0 krad to 60 krad

Figure 5(b)   DUT 40724 in-flux I_{CCA} and I_{CCI} for irradiation from 60 krad to 100 krad, ICCA shows a transition near 68 krad that indicates the shutdown of the charge pump.

Figure 6(a)   DUT 40777 in-flux I_{CCA} and I_{CCI} for irradiation from 0 krad to 60 krad

Figure 6(b)   DUT 40777 in-flux I_{CCA} and I_{CCI} for irradiation from 60 krad to 100 krad, ICCA shows a transition near 65 krad that indicates the shutdown of the charge pump.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
40678	1.24	1.48	1.20	1.45
40693	1.25	1.49	1.20	1.46
40699	1.26	1.46	1.20	1.44
40724	1.25	1.47	1.19	1.45
40777	1.24	1.46	1.20	1.44

D. *Output-Drive Voltage (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
40678	0.009	0.009	0.102	0.106	0.170	0.177	0.430	0.446	0.886	0.917
40693	0.008	0.009	0.101	0.105	0.168	0.174	0.425	0.439	0.875	0.904
40699	0.008	0.009	0.100	0.105	0.167	0.175	0.422	0.441	0.868	0.909
40724	0.009	0.010	0.108	0.110	0.180	0.184	0.454	0.463	0.932	0.952
40777	0.009	0.009	0.102	0.107	0.170	0.179	0.429	0.451	0.884	0.930

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
40678	4.99	4.99	4.86	4.87	4.65	4.69	4.08	4.12	2.82	2.94
40693	4.98	4.98	4.87	4.87	4.65	4.67	4.09	4.14	2.88	3.01
40699	4.99	4.99	4.86	4.87	4.65	4.67	4.07	4.12	2.79	2.90
40724	4.98	4.99	4.86	4.87	4.66	4.67	4.09	4.14	2.87	3.00
40777	4.98	4.99	4.86	4.87	4.65	4.67	4.08	4.12	2.85	2.94

E. *Propagation Delay*

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. DUT 40678 has the worst degradation of 2.94%.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Pre-Irradiation	Post-Annealing	Degradation
40678	592.4	610.0	2.94%
40693	568.7	579.5	1.84%
40699	587.5	601.4	2.34%
40724	590.0	605.7	2.62%
40777	582.0	591.2	1.55%

F.   Transition Time

Figures 6 to 15 show the pre-irradiation and post-annealing transition edges.   In each case, the radiation-induced transition time degradation is not significant.
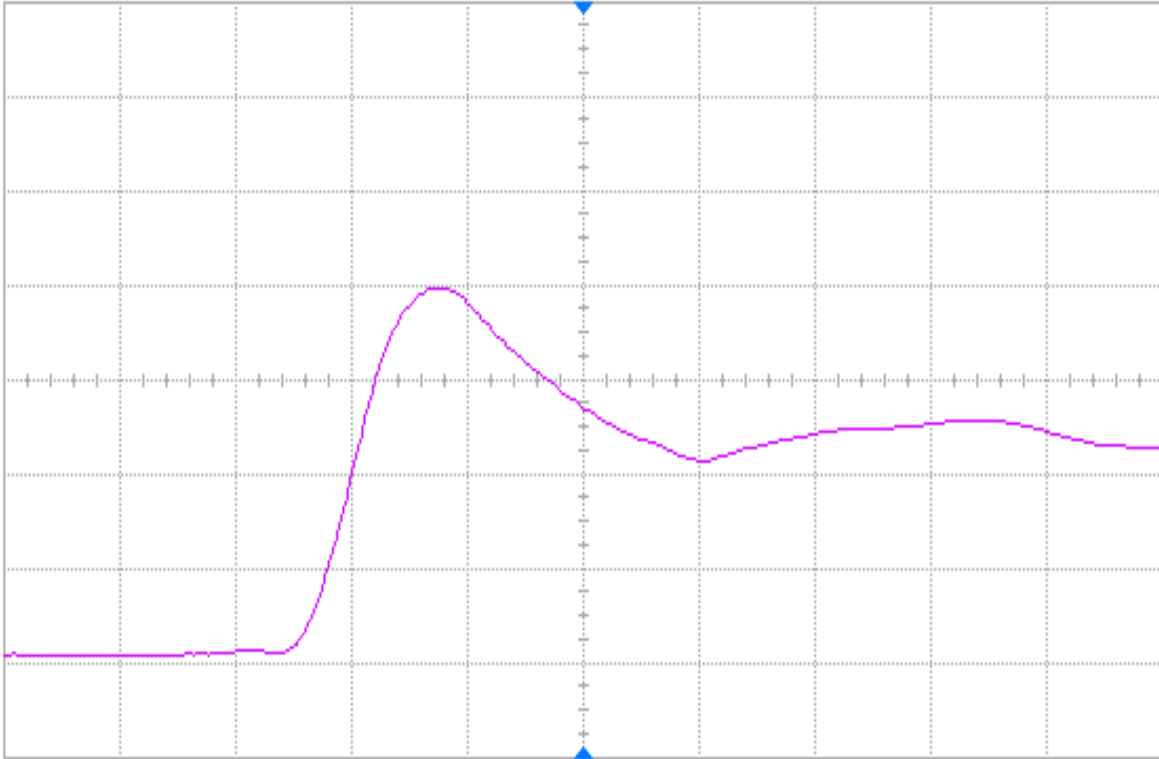
Figure 6(a)   DUT 40678 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
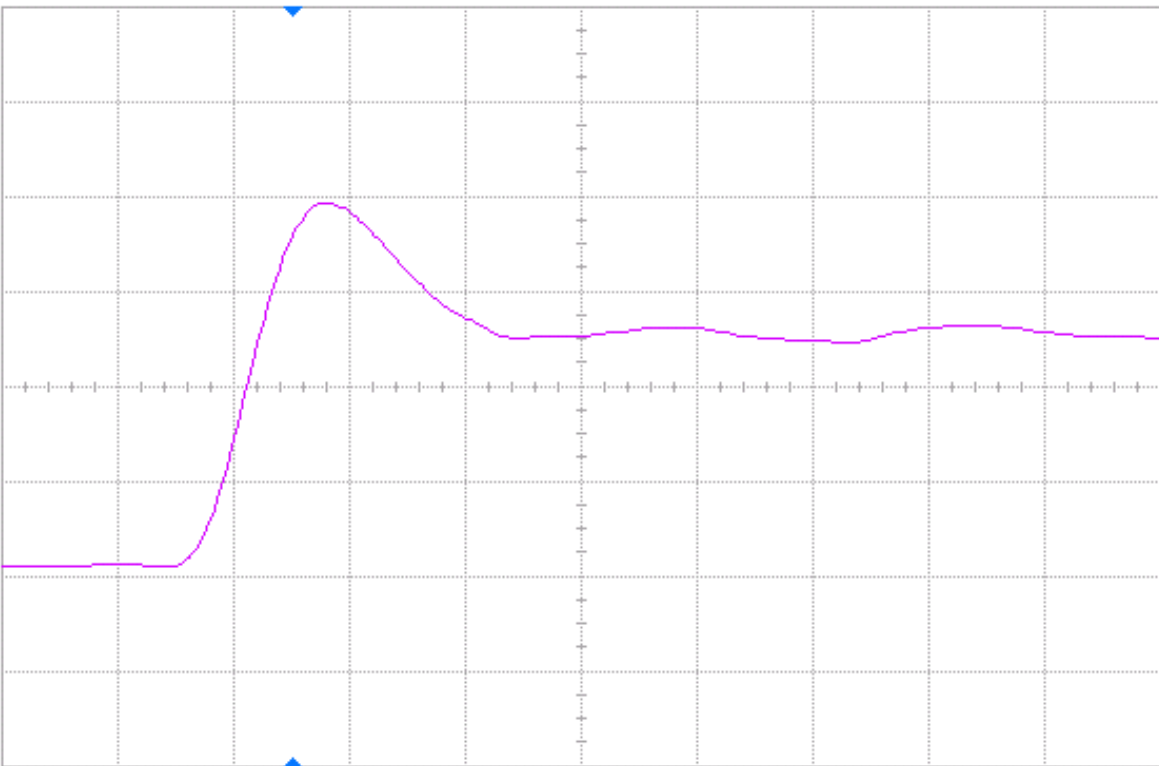

Figure 6(b)   DUT 40678 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
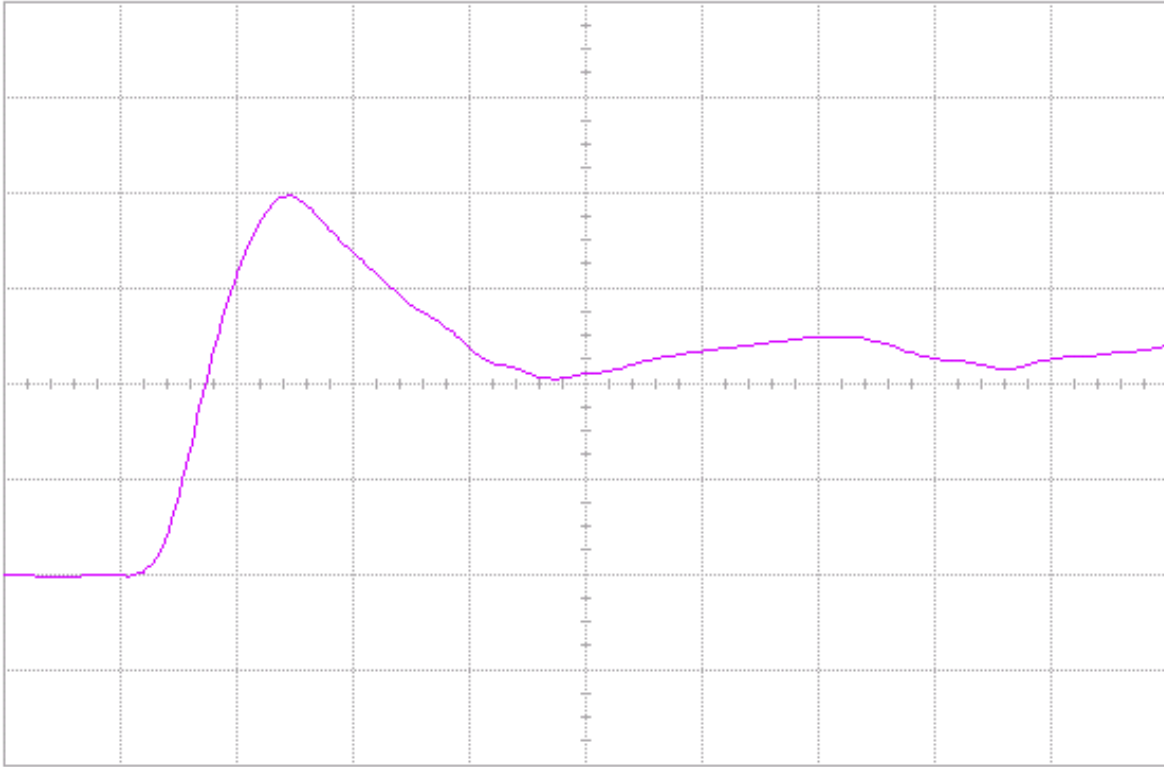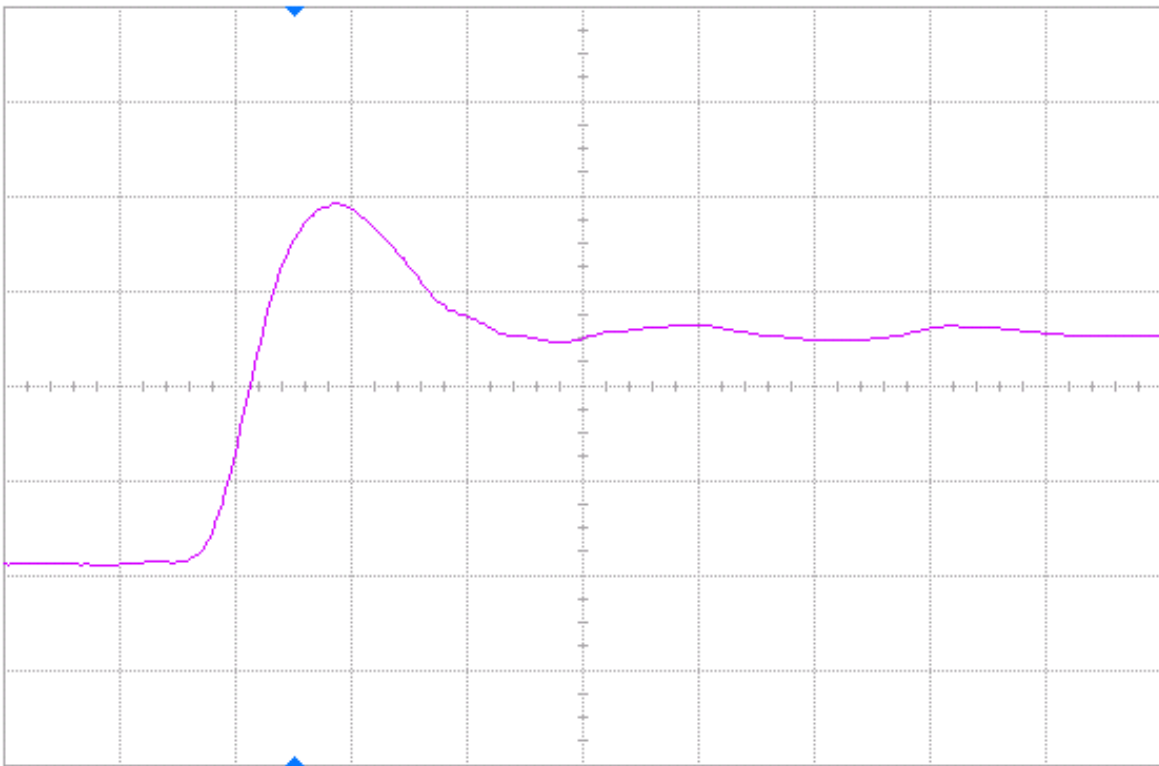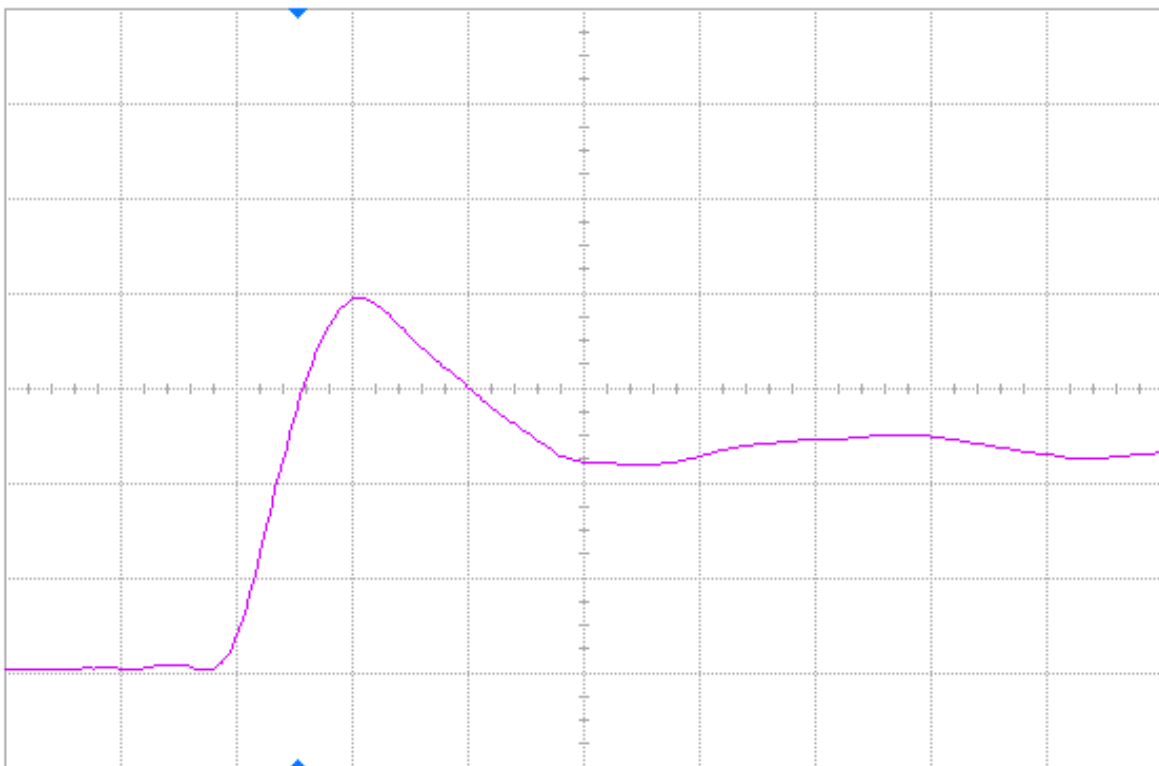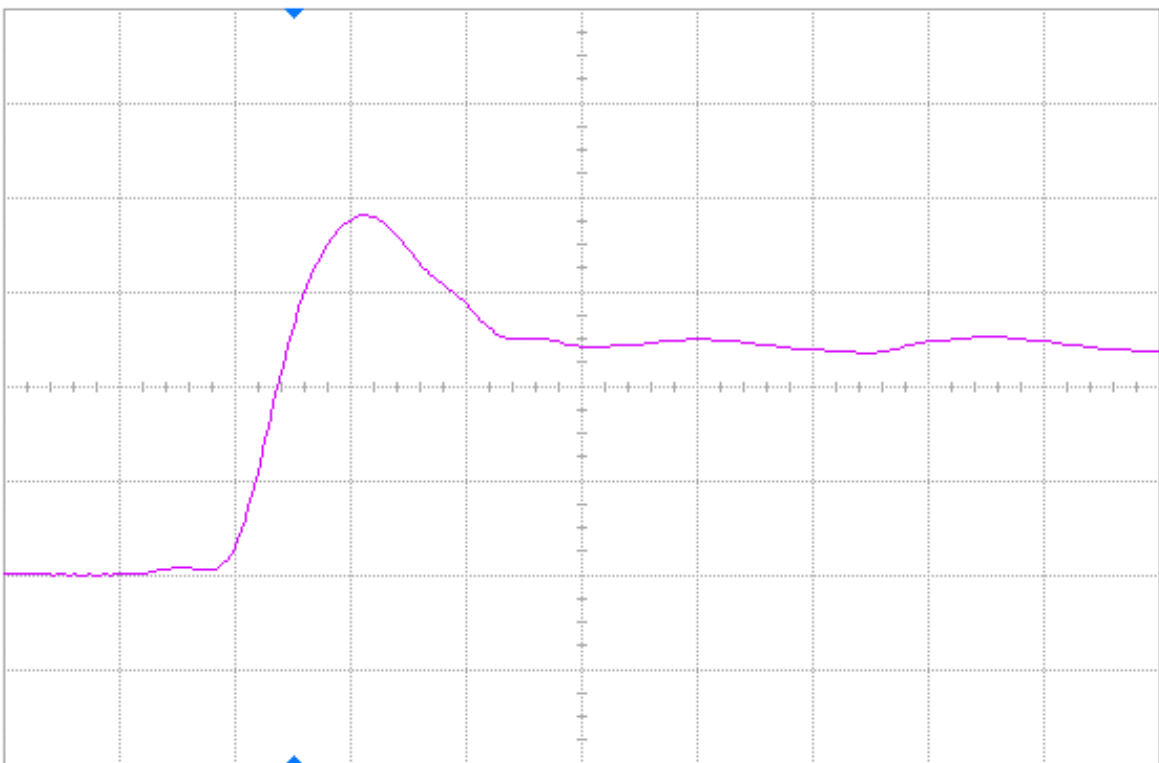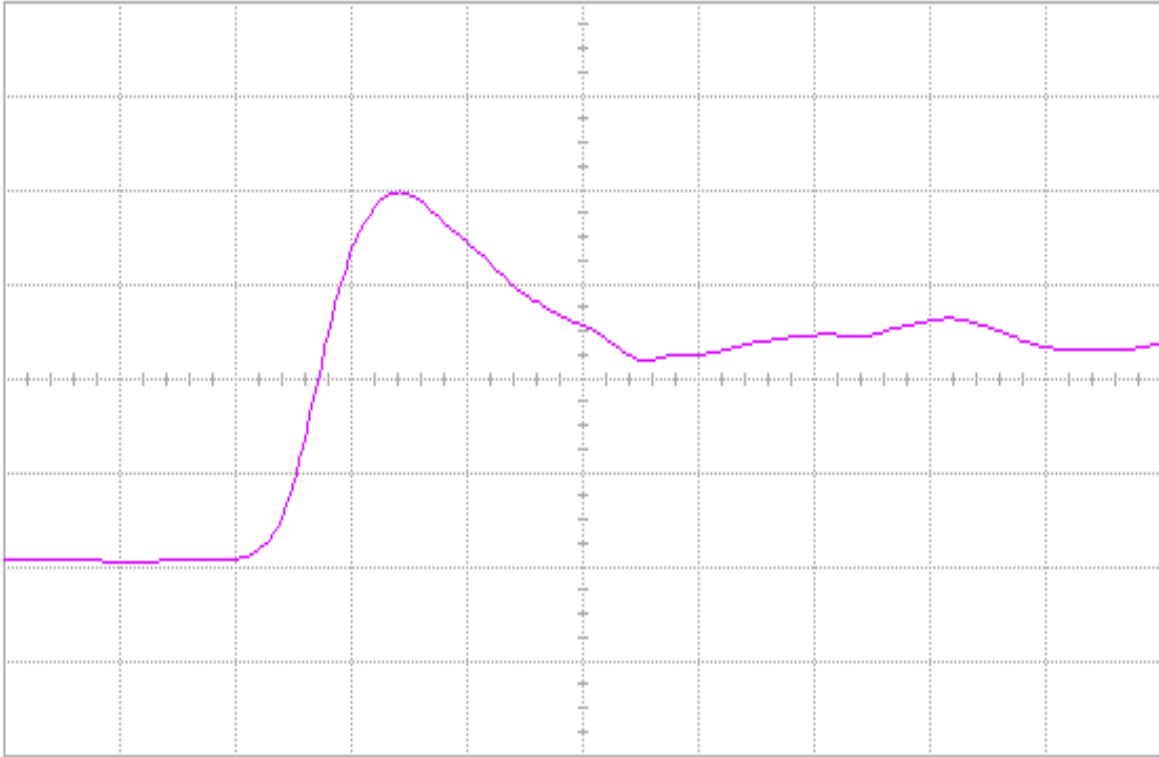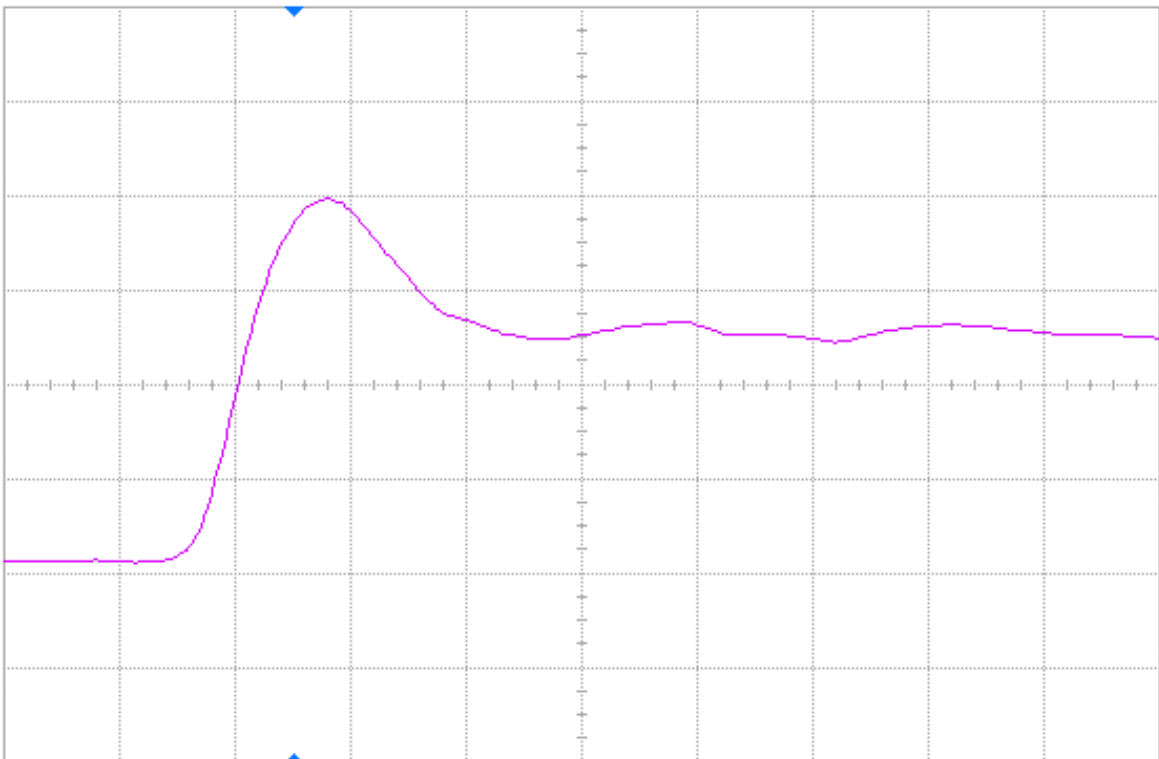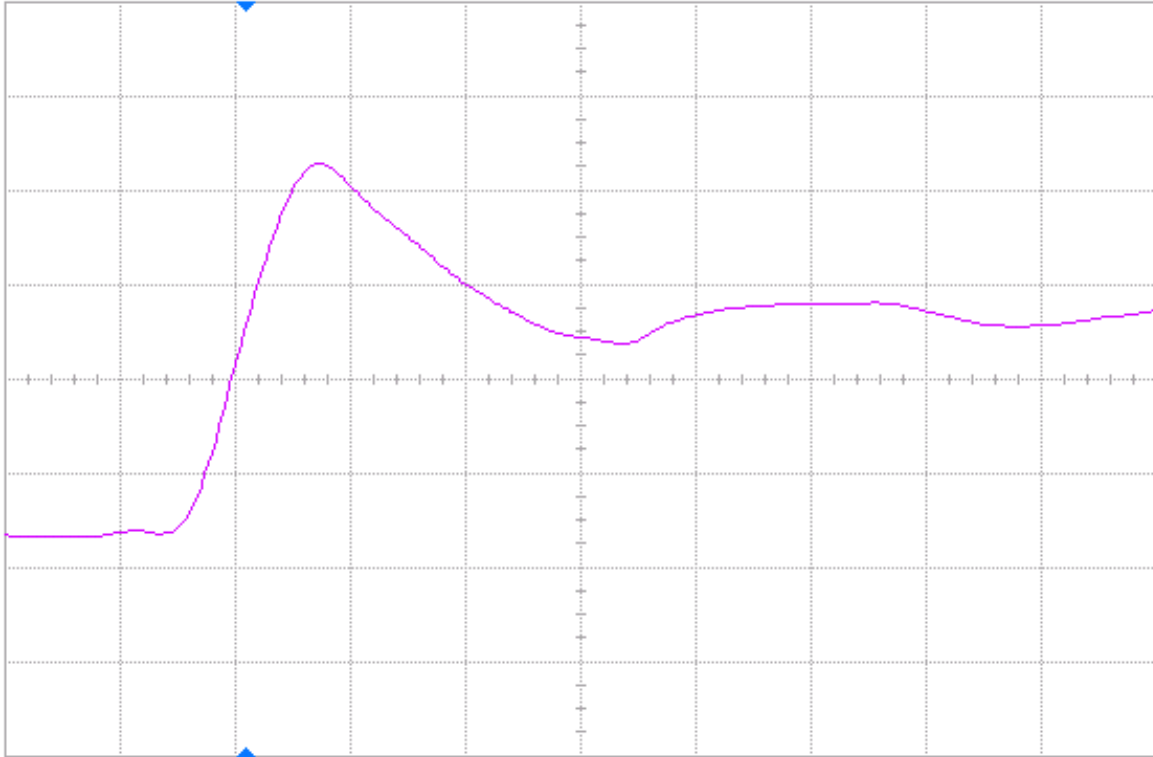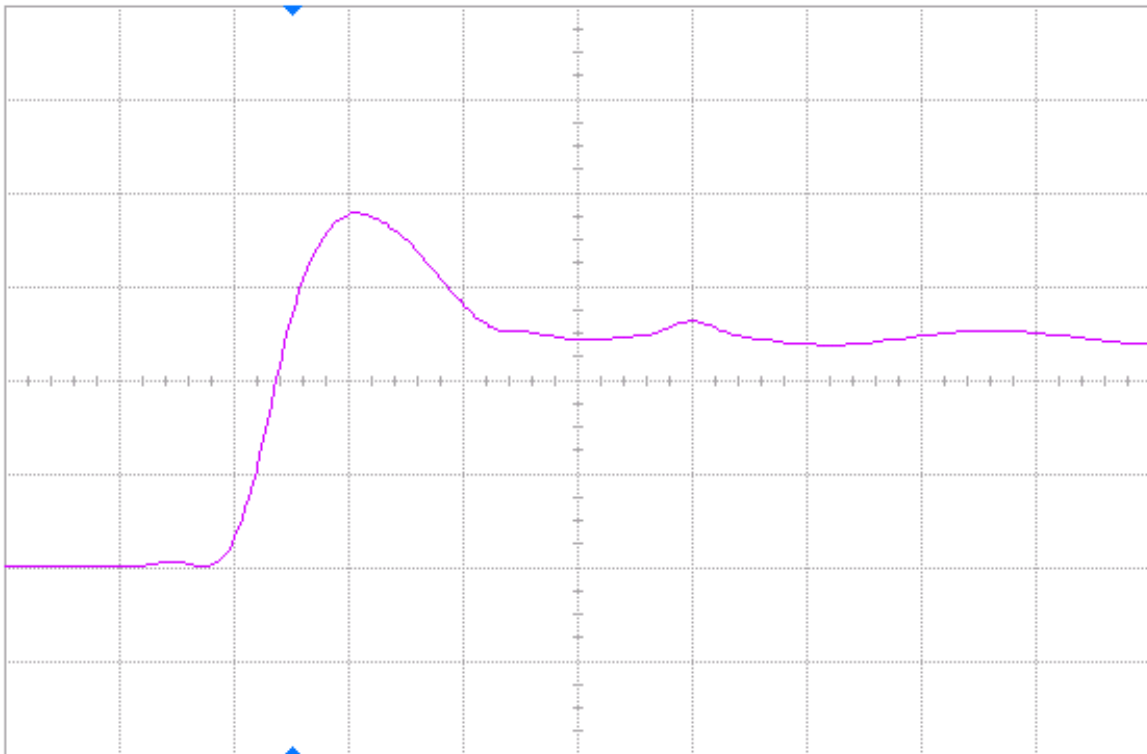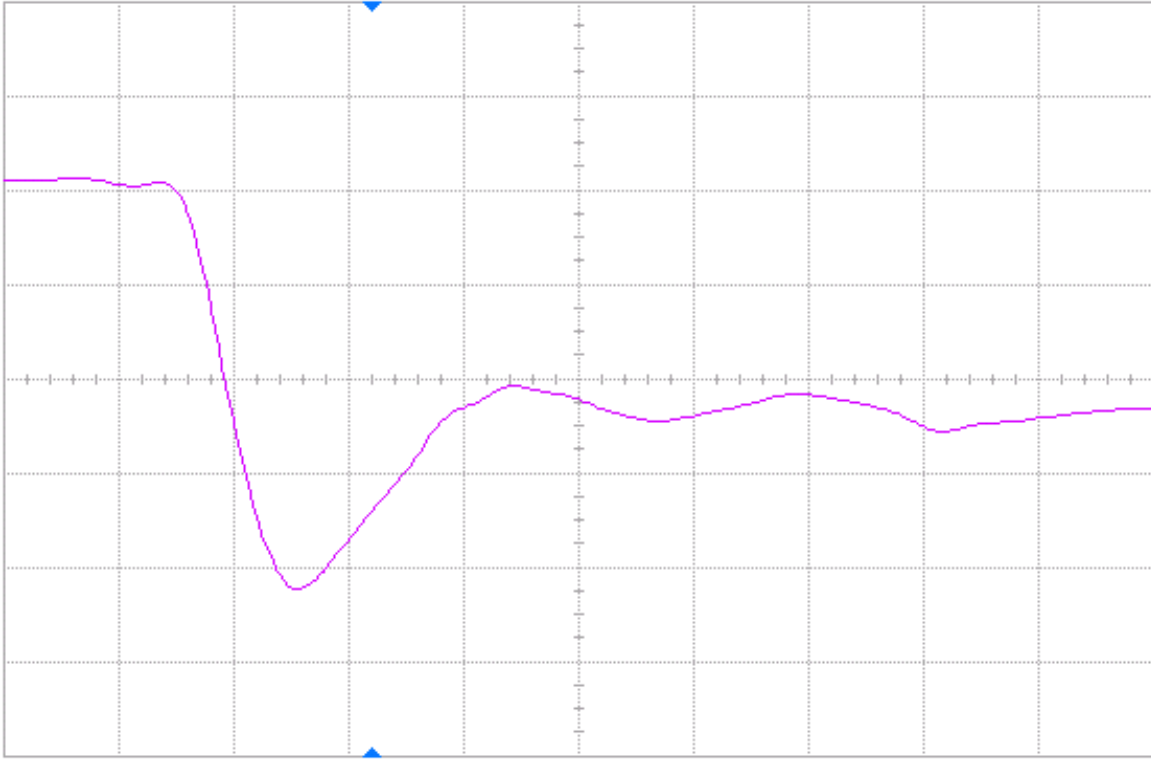
Figure 7(a)   DUT 40693 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 7(b)   DUT 40678 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
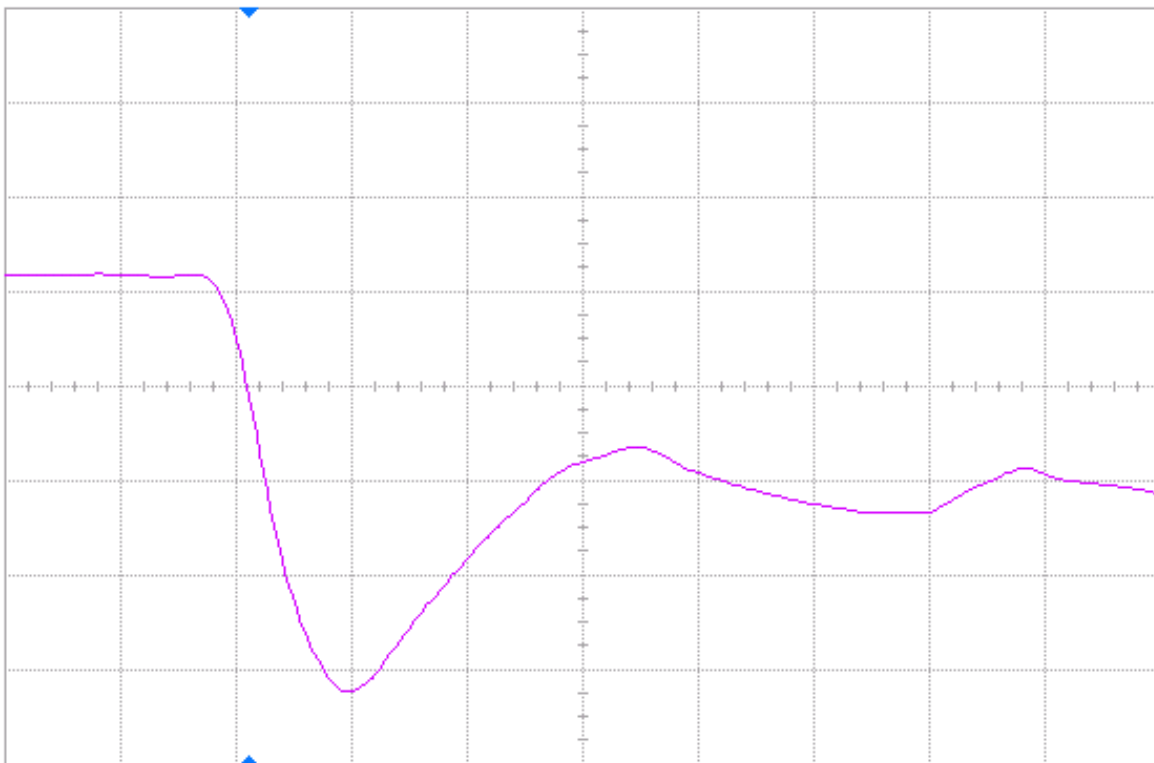
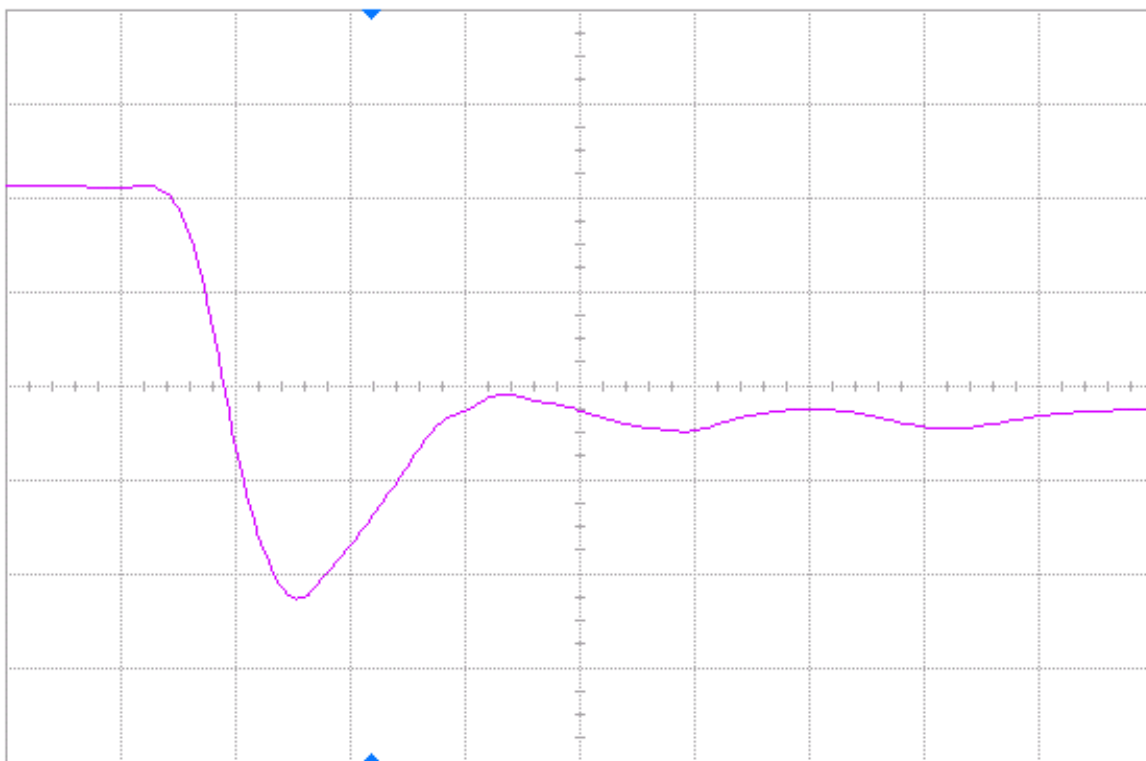Figure 8(a)   DUT 40699 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 8(b)   DUT 40699 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 9(a)   DUT 40724 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

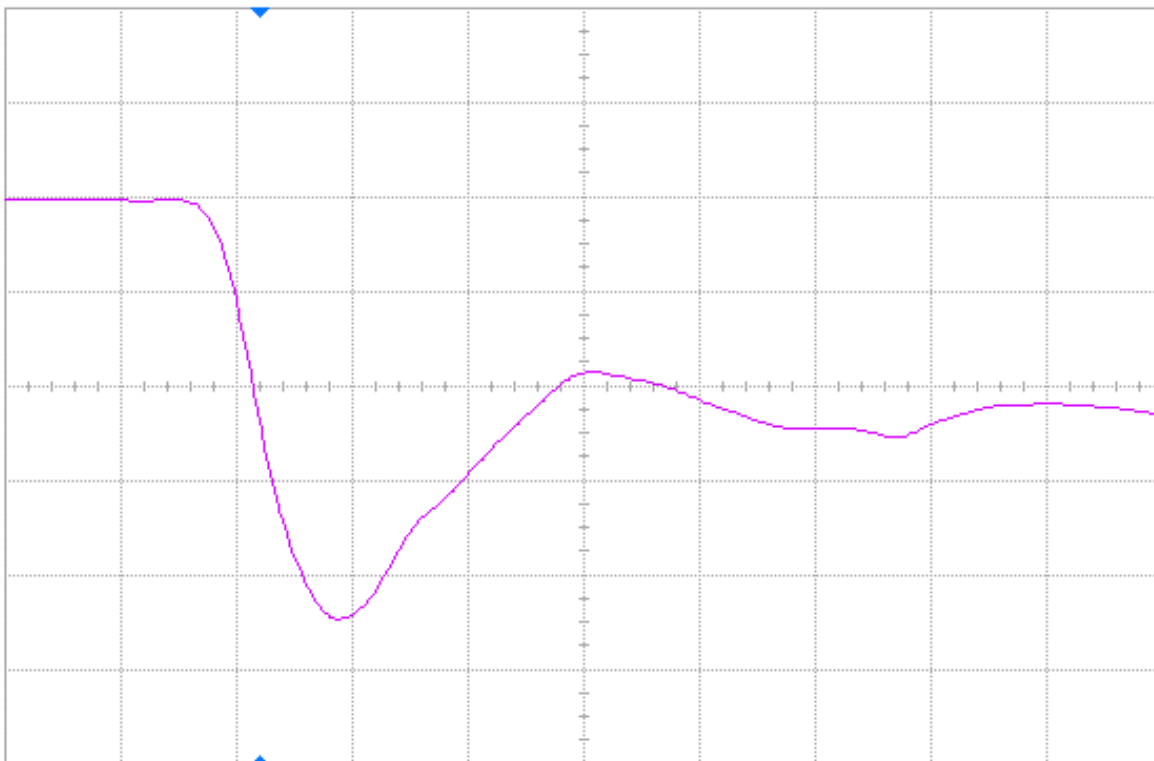Figure 9(b)   DUT 40724 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 10(a) DUT 40777 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div

Figure 10(b) DUT 40777 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 11   DUT 40678 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 12(a) DUT 40693 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
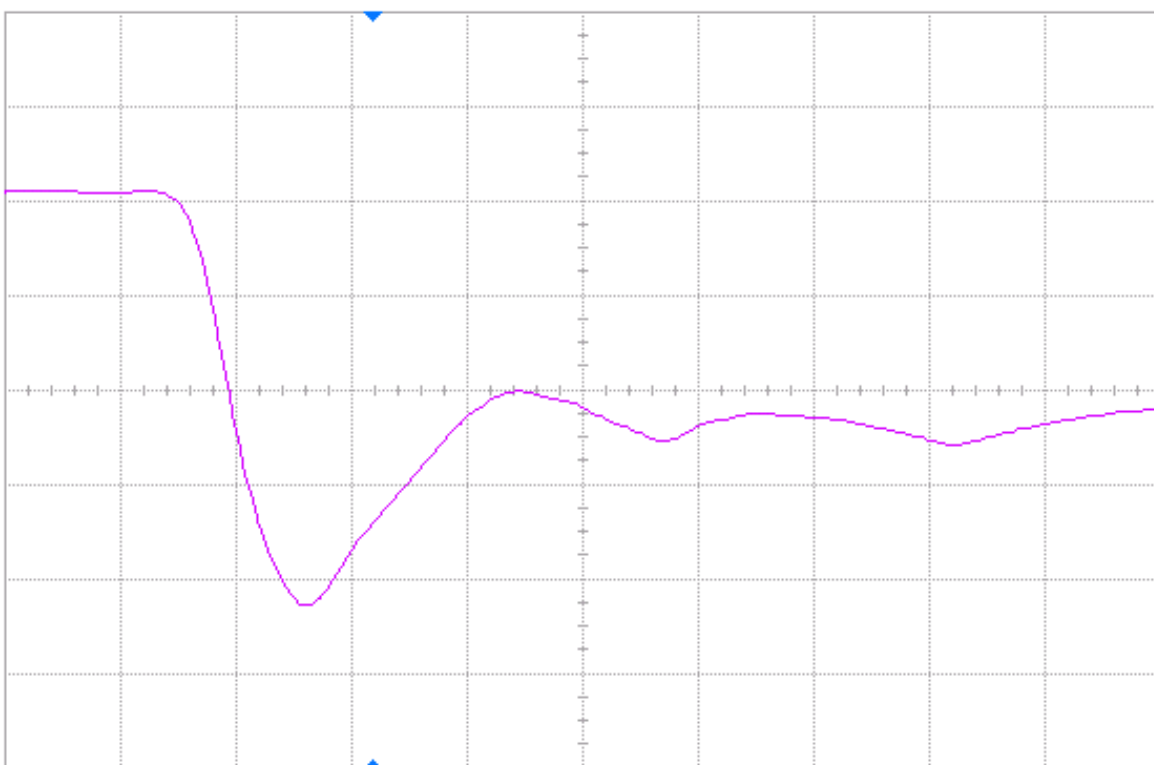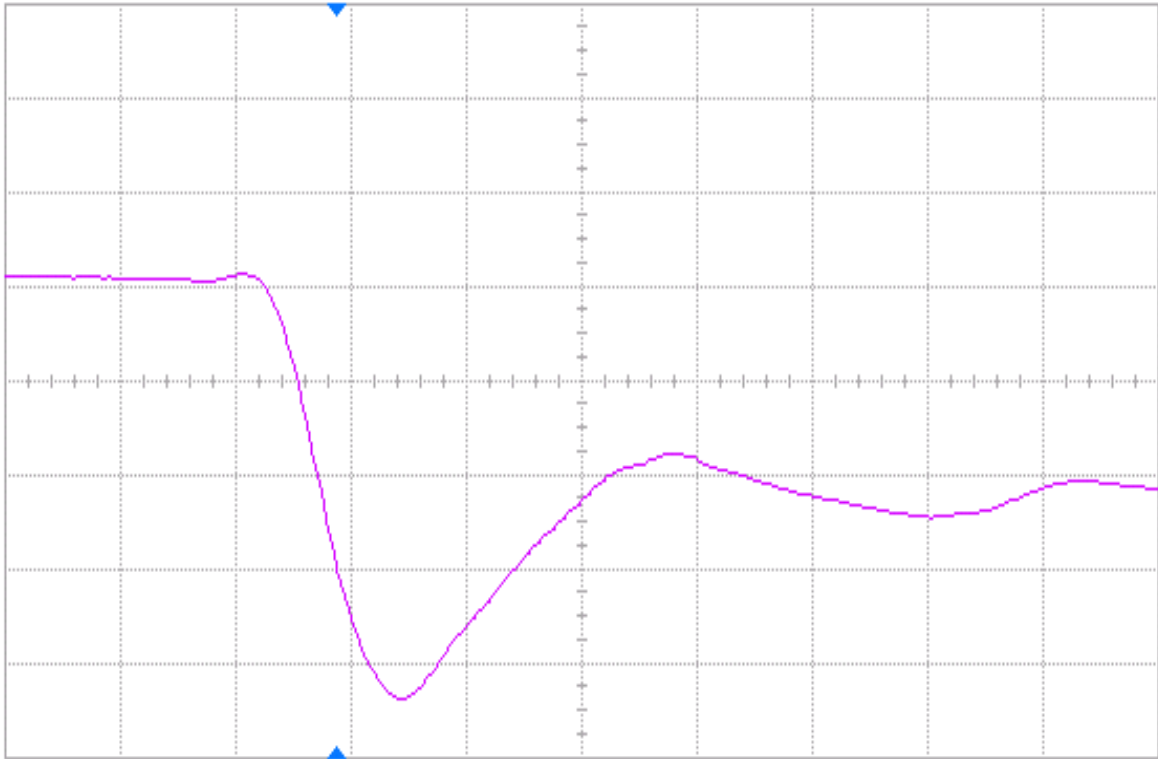

Figure 12(b) DUT 40693 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 13(a) DUT 40699 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
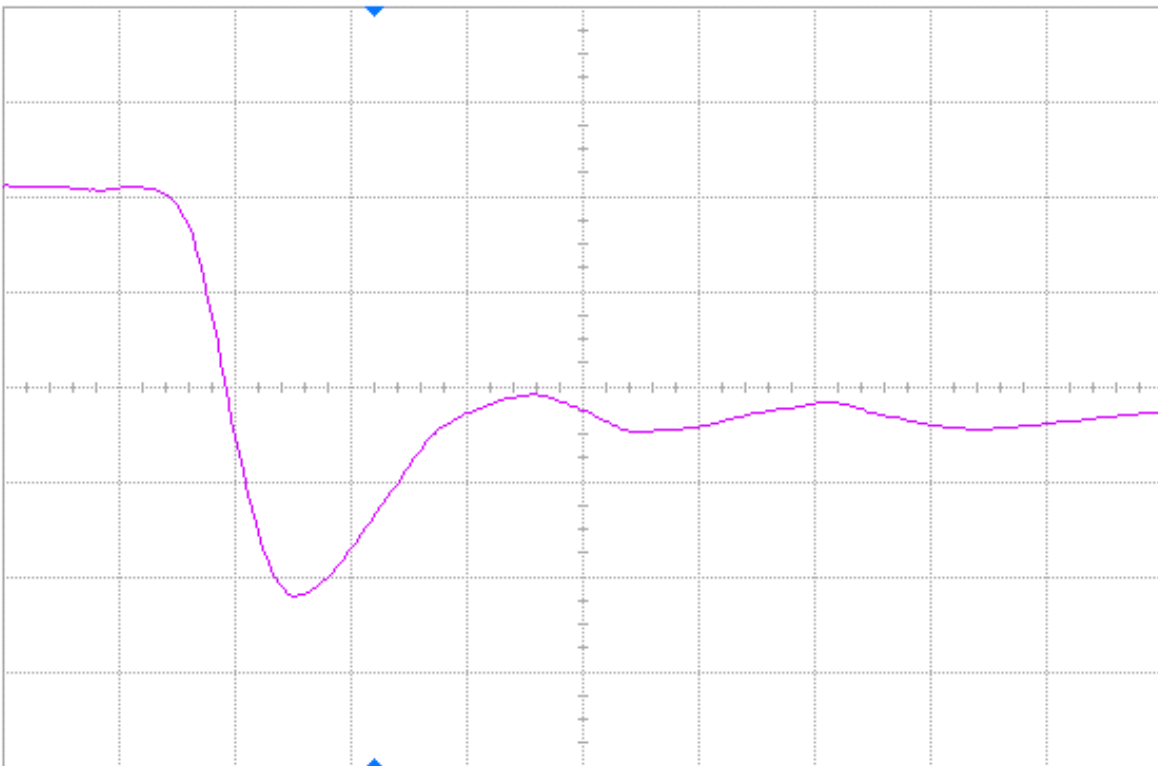

Figure 13(b) DUT 40699 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
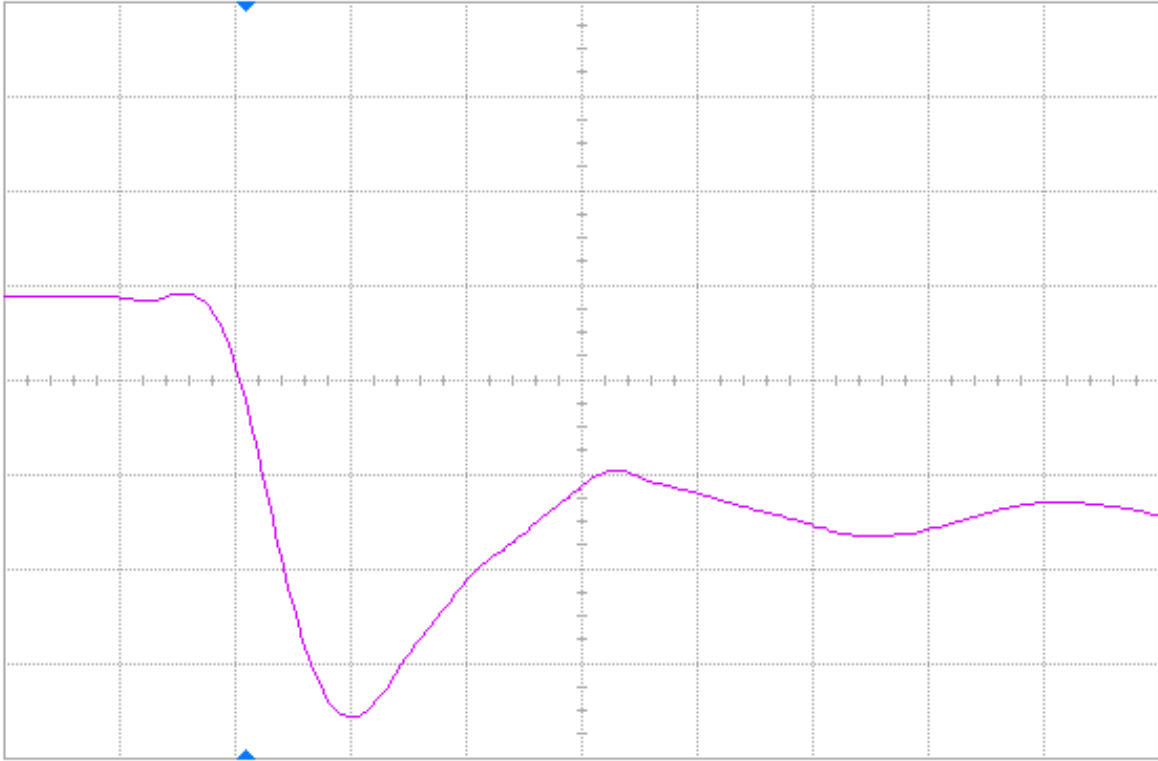
Figure 14(a) DUT 40724 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 14(b) DUT 40724 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 15(a) DUT 40777 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
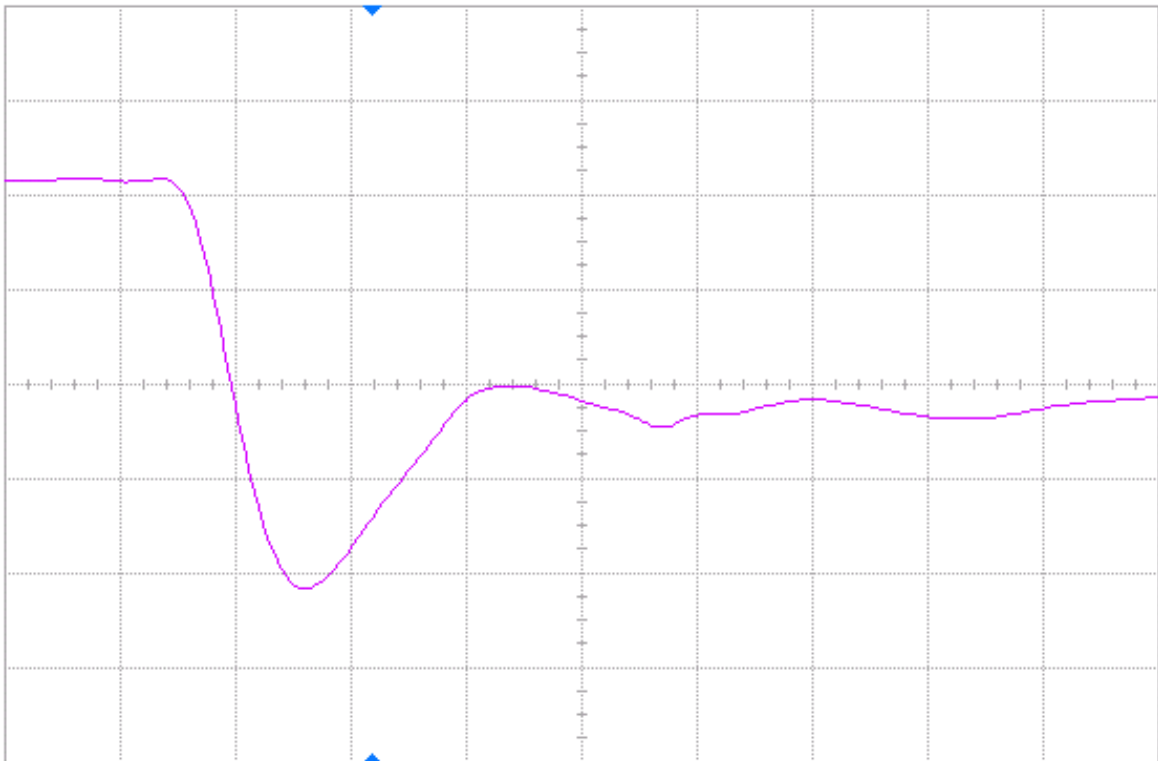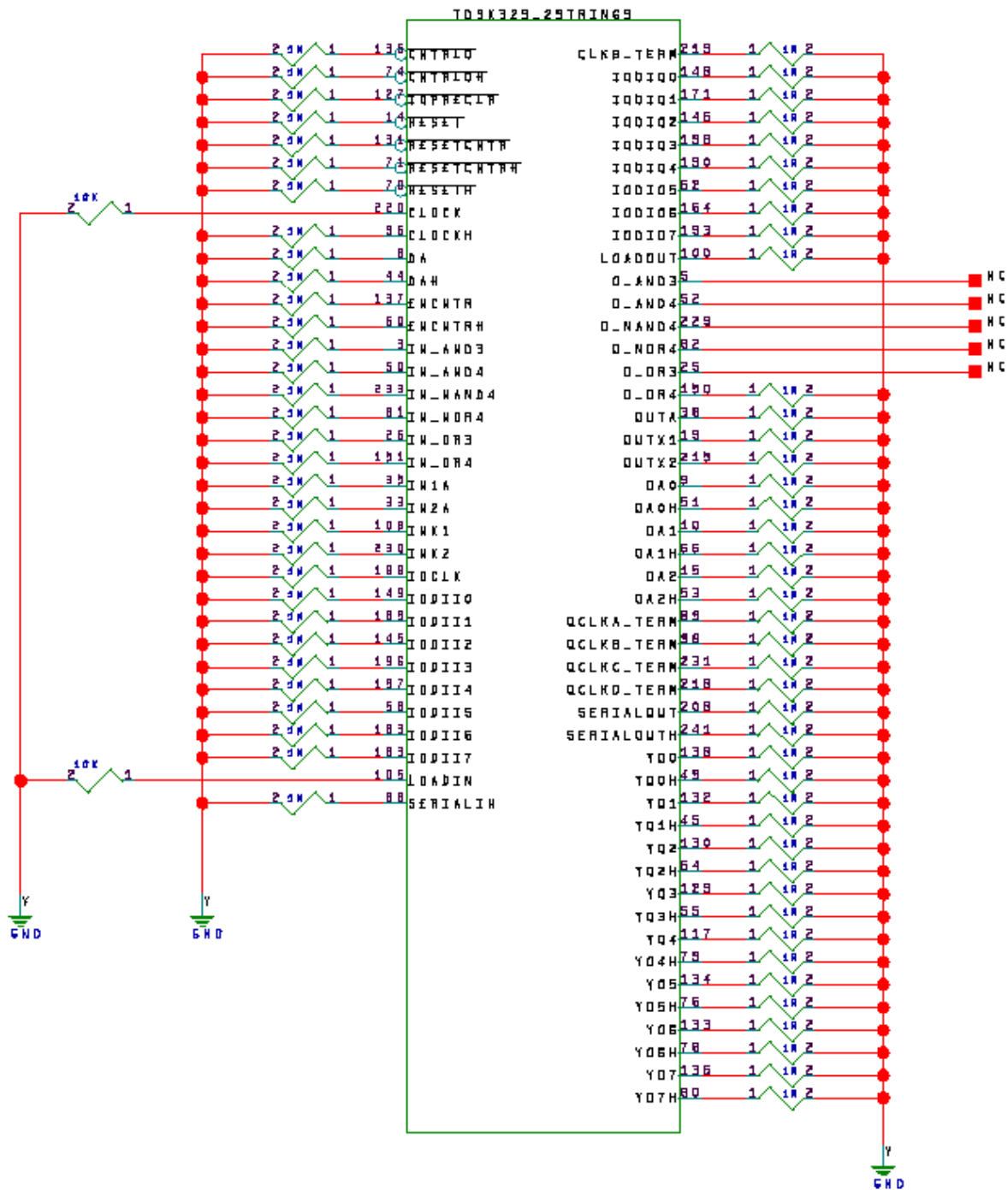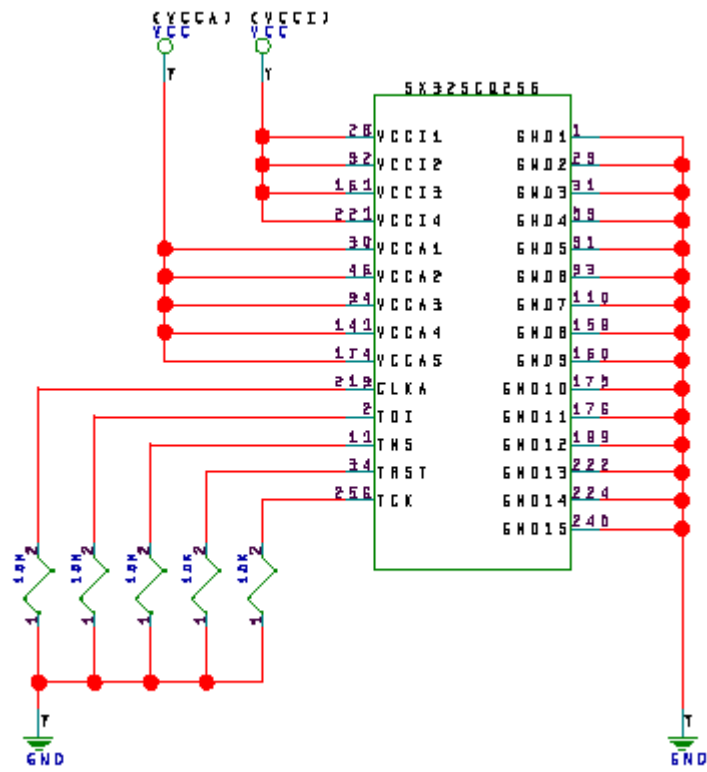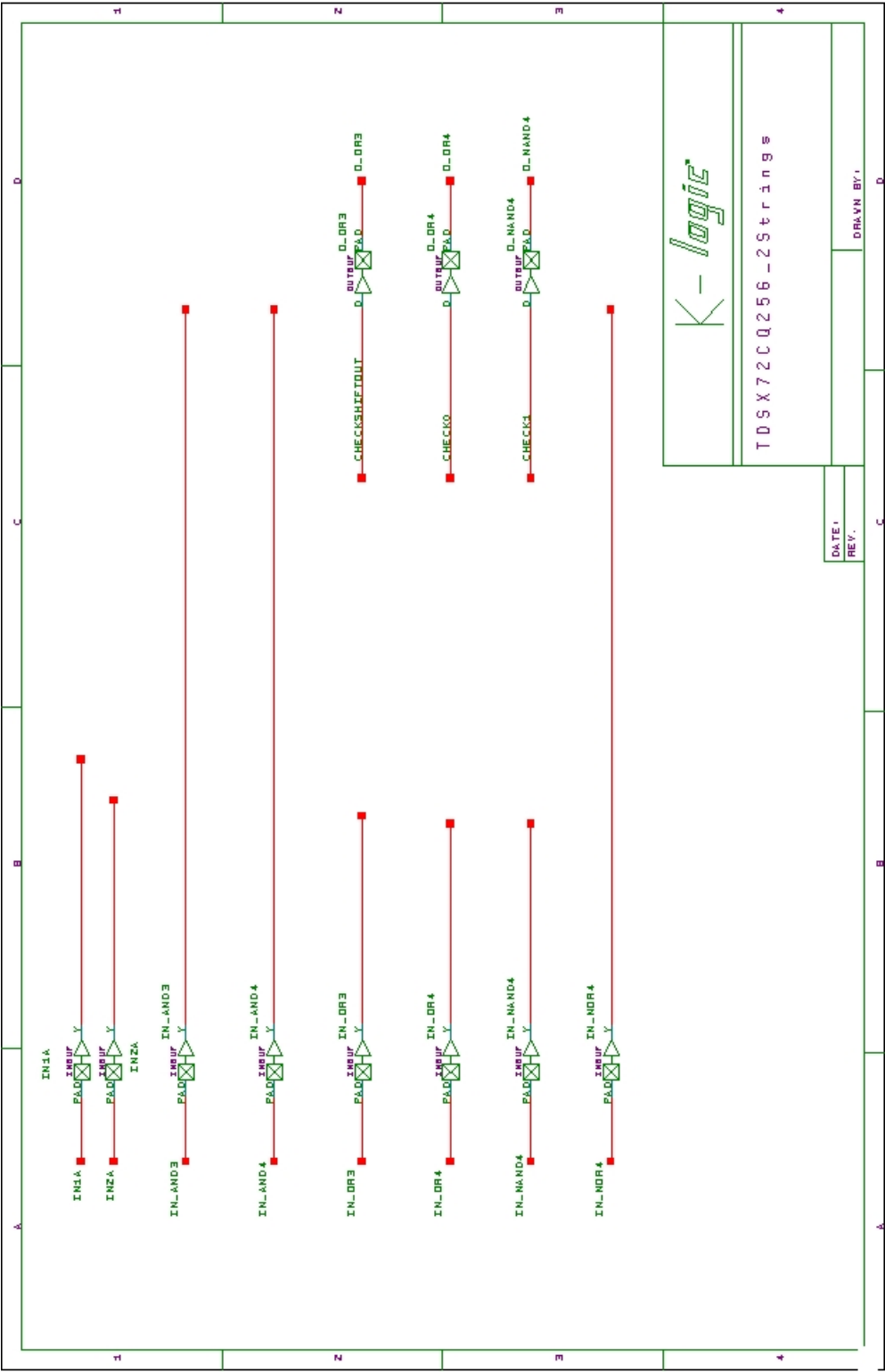

Figure 15(b) DUT 40777 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

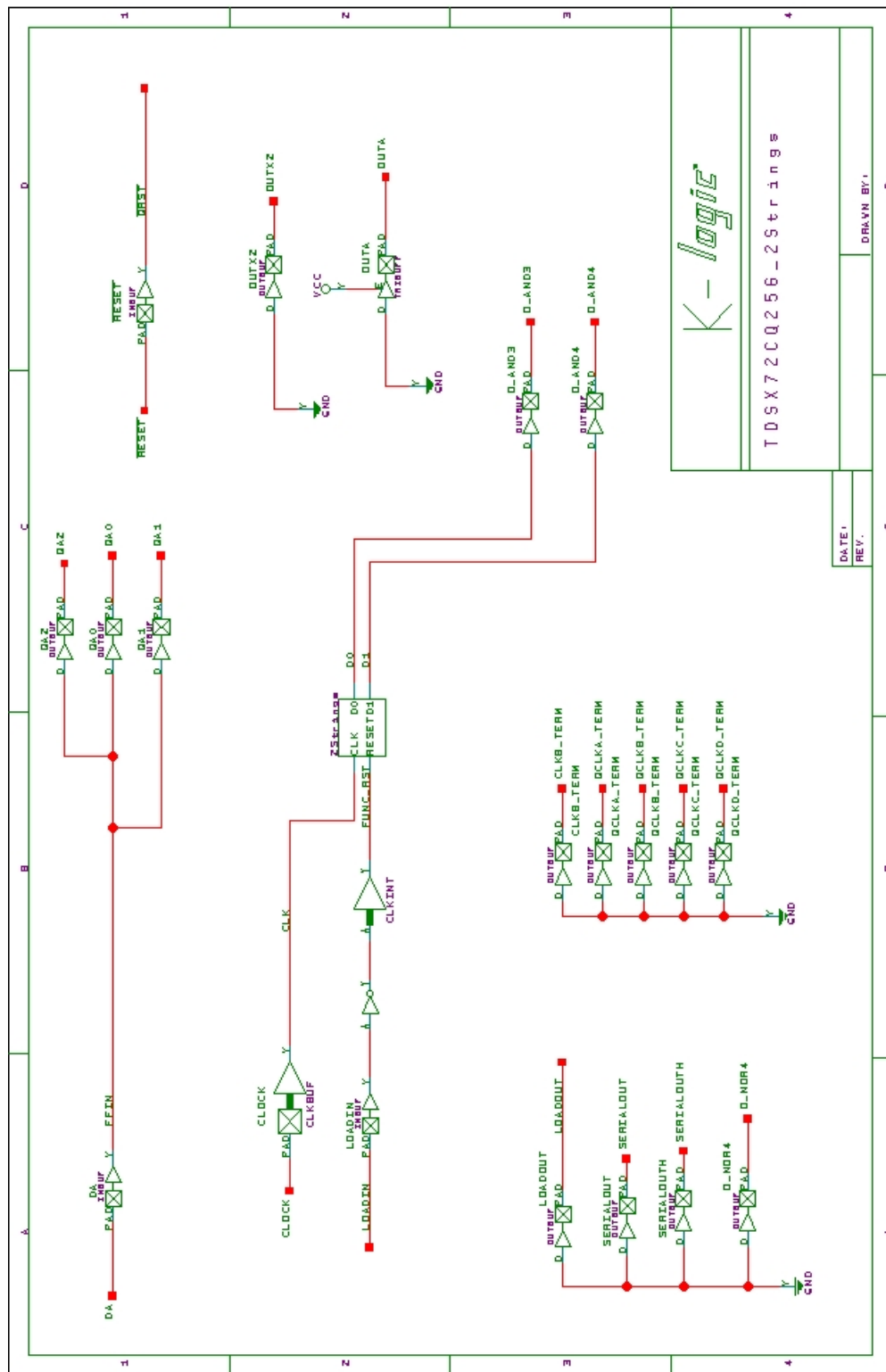Appendix A DUT Bias

A<small>PPENDIX</small> B   DUT D<small>ESIGN</small> S<small>CHEMATICS</small> (TDSX32CQ256_2STRINGS is the same as TDSX72CQ256_2STRINGS except the sizes of buffer strings and shift registers)

STRING 0: NON-INVERTING STRING, 1000 STAGES
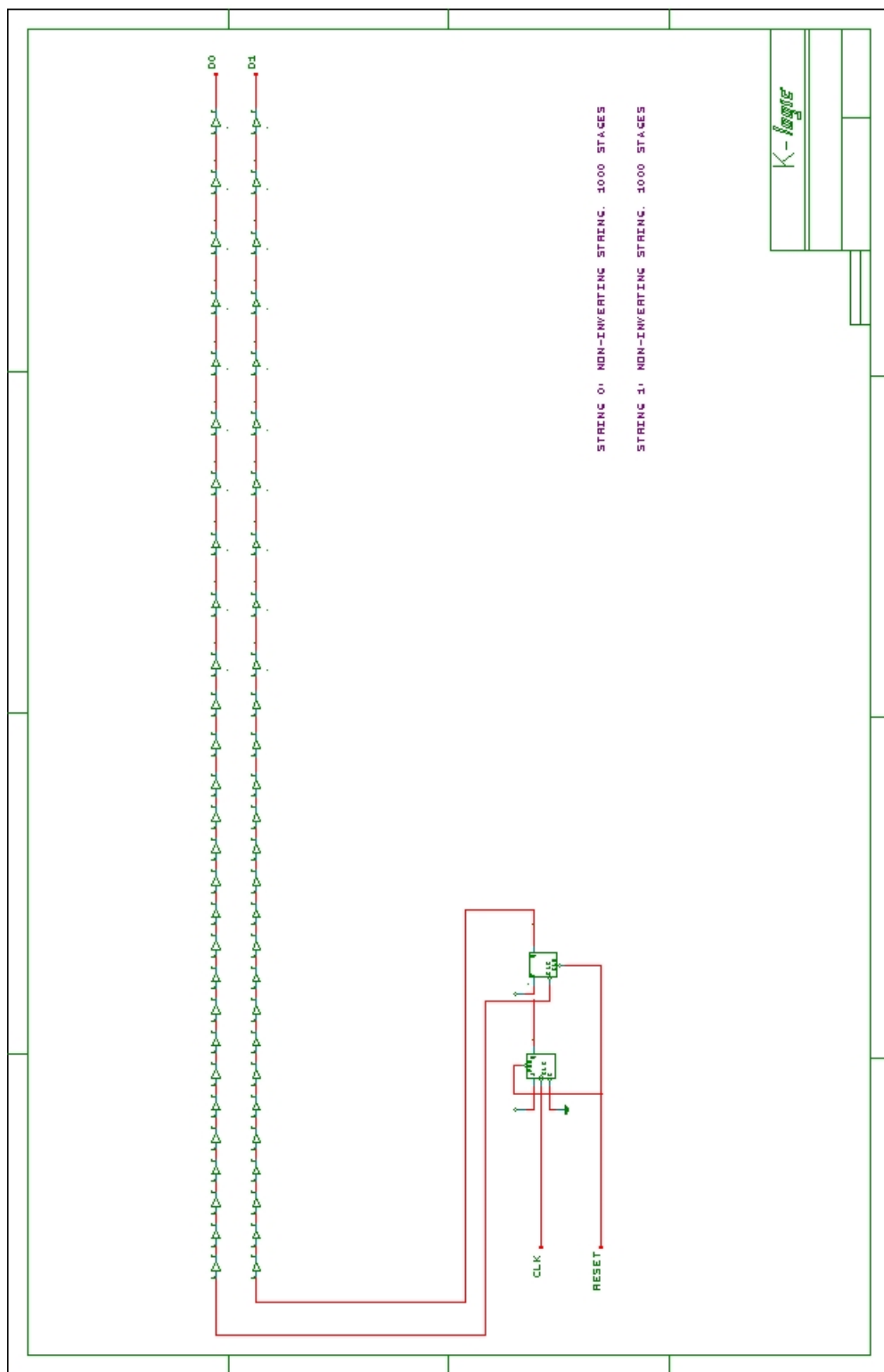
STRING 1: NON-INVERTING STRING, 1000 STAGES

D0

D1

CLK

RESET

K-logic

Y PRESERVE

K-logic®

TDSX72CQ256_2Strings

K-logic

TDSX72CQ256_2Strings

DATE:
REV.

DRAWN BY:

INX1
INBUF
PA...
Y
INX1

INX2
INBUF
PA...
Y
INX2

K-logic

TDSX72CQ256_2Strings

DRAWN BY:

DATE:
REV.

K-logic

TDSX72CQ256_2Strings

DRAWN BY:

DATE:
REV.

K - logic

TDSX72CQ256_2Strings

DRAWN BY:

DATE:
REV.

YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H

RESETCNTRH
ENCNTRH

CNTRLDH

34

TAKE NOTE OF THIS

NOT USED FOR SX

IODIO7
IODIO7
OUTBUF
PAD
IODIO7

IODII7
IMBUF
PAD
Y
IODII7

IOPRECLR
IOPRECLRDUMMY
IOPRECLR
IMBUF
PAD
Y
IOPRECLR

IOCLK
IMBUF
PAD
Y
IOCLK

^IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on Sx16
will have to make pin 127 on the Sx32 pattern

IODIO0 IODIO0 OUTBUF PAD IODIO0
IODIO1 IODIO1 OUTBUF PAD IODIO1
IODIO2 IODIO2 OUTBUF PAD IODIO2
IODIO3 IODIO3 OUTBUF PAD IODIO3
IODIO4 IODIO4 OUTBUF PAD IODIO4
IODIO5 IODIO5 OUTBUF PAD IODIO5
IODIO6 IODIO6 OUTBUF PAD IODIO6

IODII0 IMBUF PAD Y IODII0
IODII1 IMBUF PAD Y IODII1
IODII2 IMBUF PAD Y IODII2
IODII3 IMBUF PAD Y IODII3
IODII4 IMBUF PAD Y IODII4
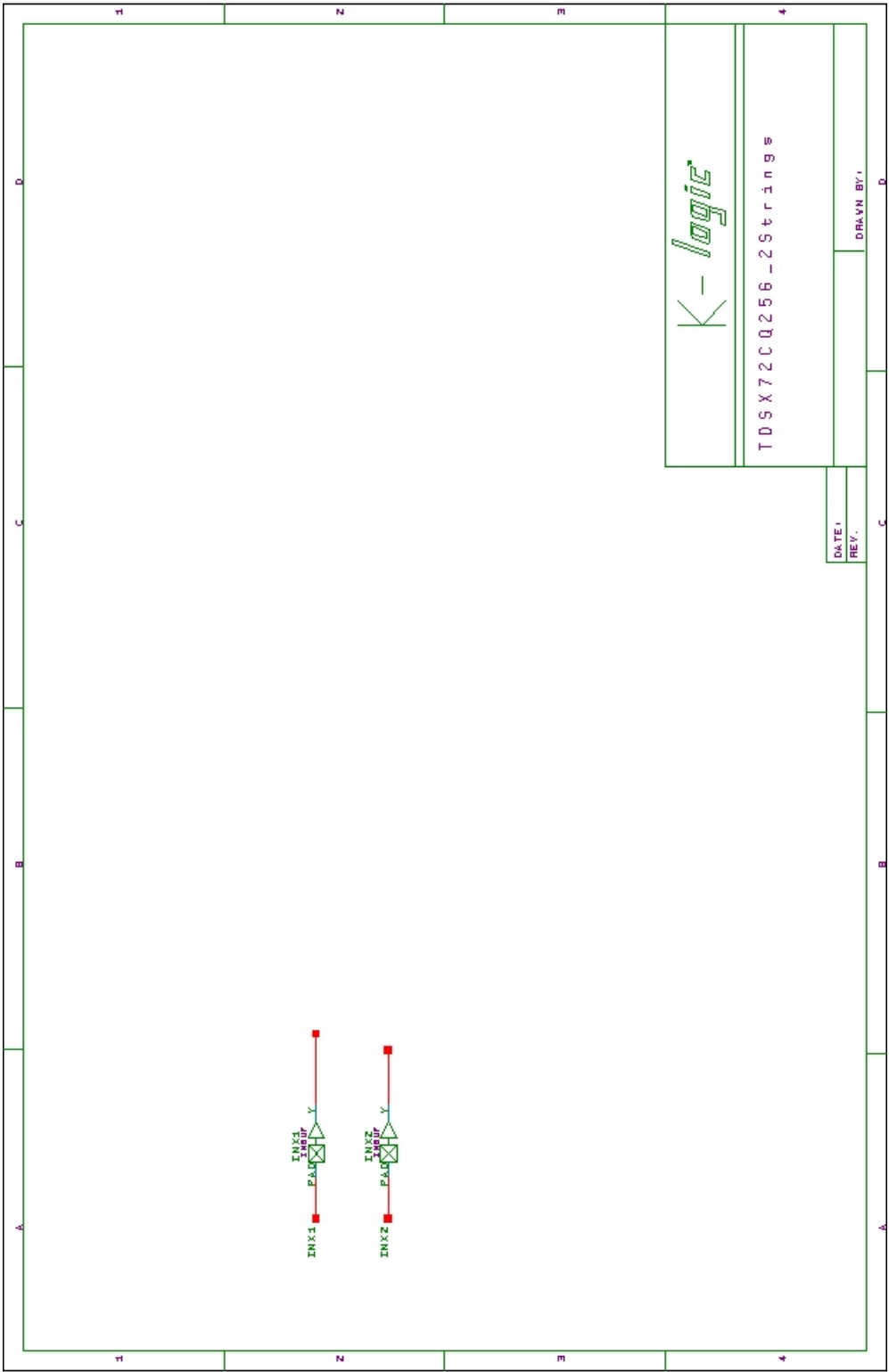IODII5 IMBUF PAD Y IODII5
IODII6 IMBUF PAD Y IODII6

K-logic

TDSX72CQ256_2Strings

DATE:
REV.

DRAWN BY:

K-logic

TDSX72CQ256_2Strings
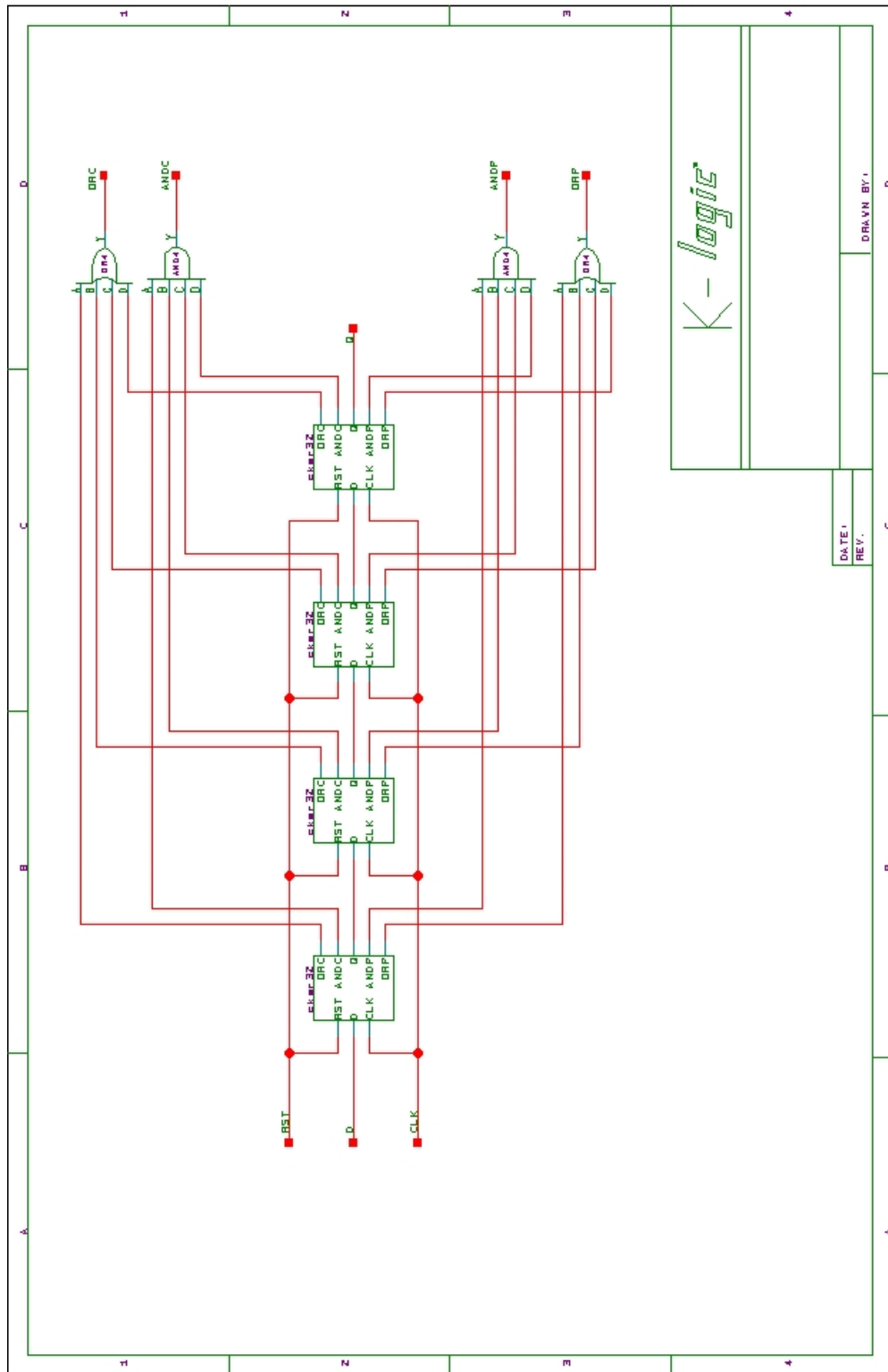
DRAWN BY:

DATE:
REV.

SERIALIN
INBUF
SERIALIN PADO Y SERIN

OUT x1

OUT x1
OUTPUT
D   PAD

Y
GND

K-logic

TDSX72CQ256_2Strings

DRAWN BY:

DATE:
REV.