TOTAL IONIZING DOSE TEST REPORT

No. 04T-RT54SX72S(U)-D0Y311
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 62.6 krad (Si) using 25-mA spec. Post 100 krad (Si) and after 90 days room temperature annealing: average I_{CCA} = 100 mA, and average I_{CCI} = 48.3 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) for 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

The present testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement provides lower noise, better accuracy and more flexibility. The bench measurement samples pins for some measurements (e.g. threshold voltage measurement). However, since the tolerance is determined by the most degraded parameter, which is I_{CC} or propagation delay, sampling the pins for measuring non-critical parameters is appropriate.

A. Device Under Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

|	
Part Number	RT54SX72S
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 μm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	DOY311-003
Quantity Tested	4
Serial Number	37467, 37468, 37471, 37473
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method
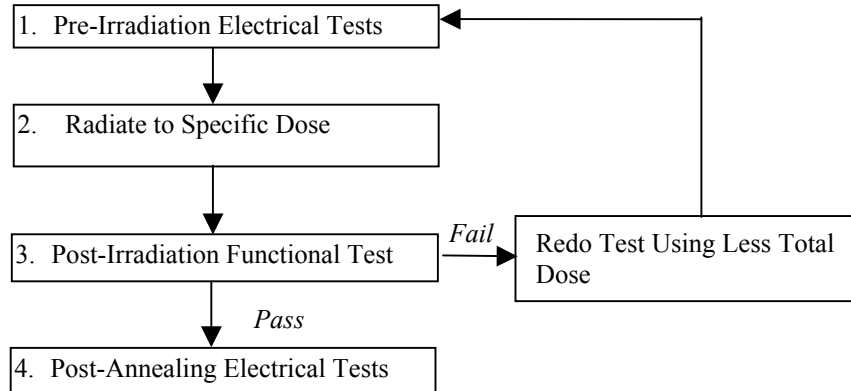
Figure 1   Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs are biased annealed for 90 days after the 100-krad (Si) irradiations.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX32CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots of the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. *Functionality*

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 5 basically show the radiation-induced leakage current. The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3. Post Irradiation and Post-Annealing I_{CC}

DUT	I_{CCA} (mA)		I_{CCI} (mA)	
	Post-rad	Post-ann	Post-rad	Post-ann
37467	318	97	236	66
37468	258	94	186	40
37471	266	101	181	40
37473	282	108	207	47

An empirical equation is used to extract the total dose tolerance. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA is obtained from the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are in-flux currents when total dose equals to γ. Using the-worst-case in-flux currents degradation, which is DUT 37467 (Figure 2), the tolerance ($\gamma_{critical}$) is obtained as approximately 62.6 krad (Si). This equation produces a conservative tolerance because the process of a high-dose-rate irradiation plus annealing produces an I_{CC} higher than the I_{CC} produced by a consistent low-dose-rate irradiation process.
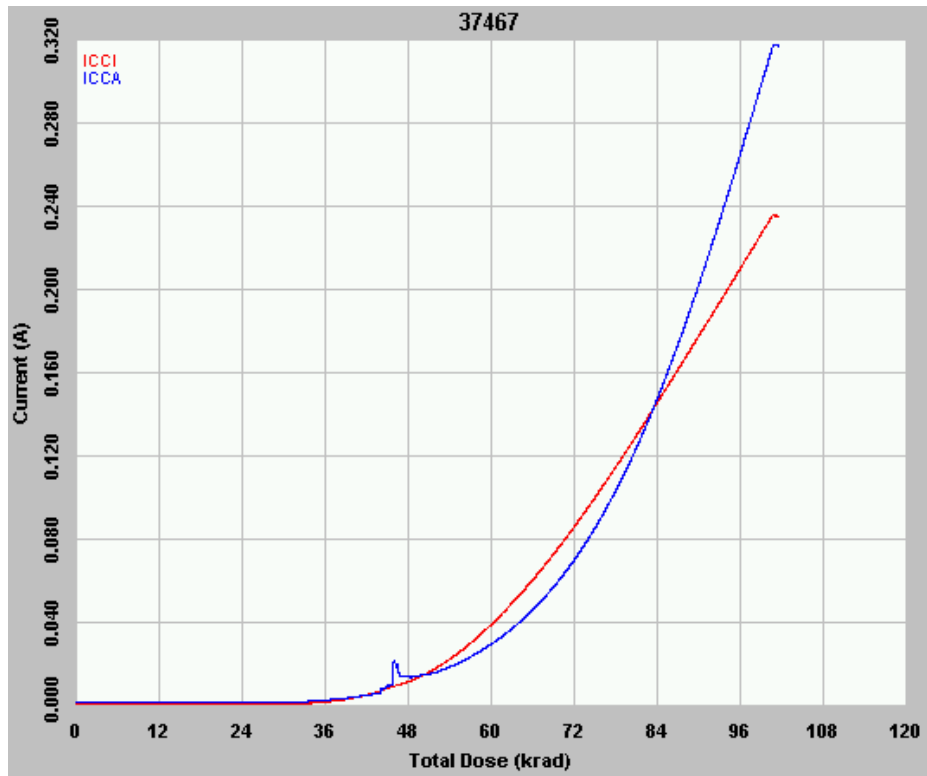
Figure 2   DUT 37467 in-flux I_{CCA} and I_{CCI}
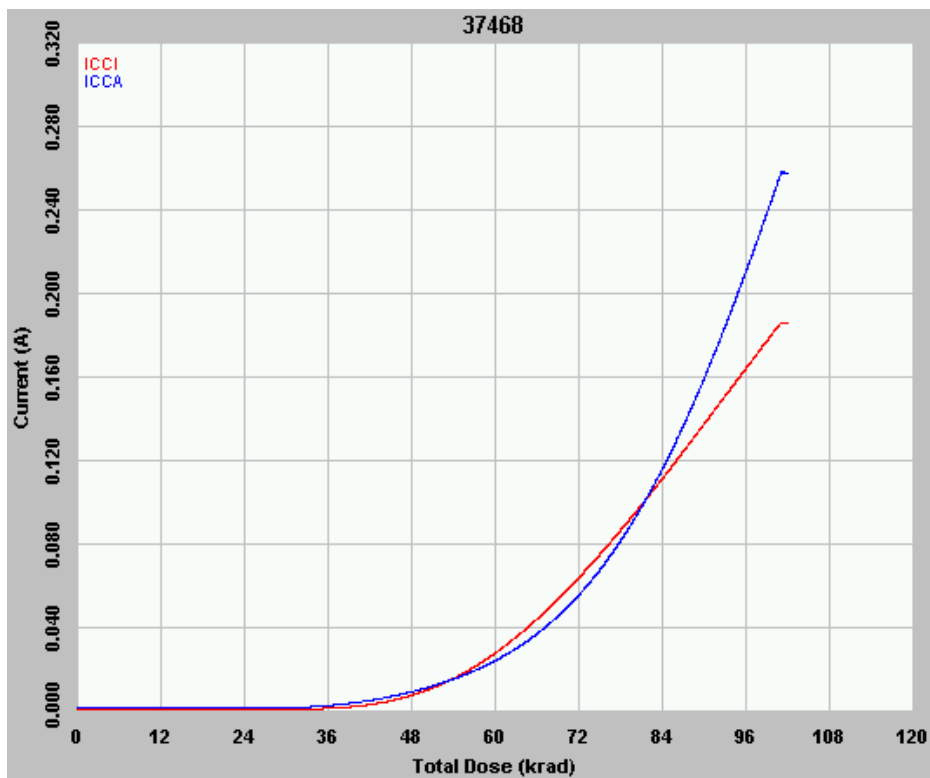
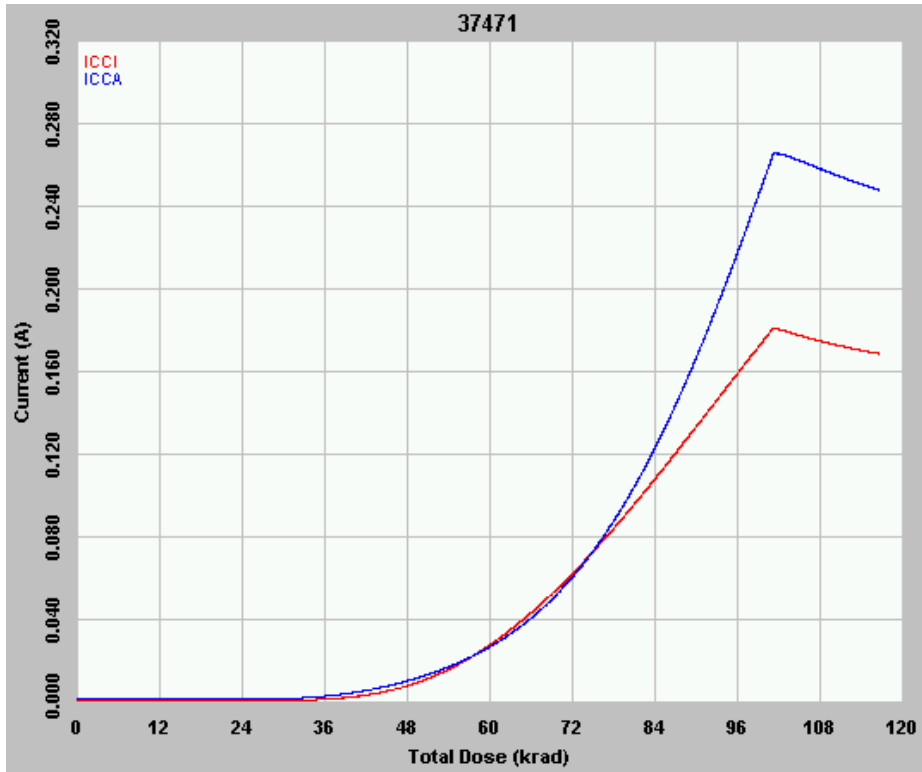Figure 3   DUT 37468 in-flux I_{CCA} and I_{CCI}

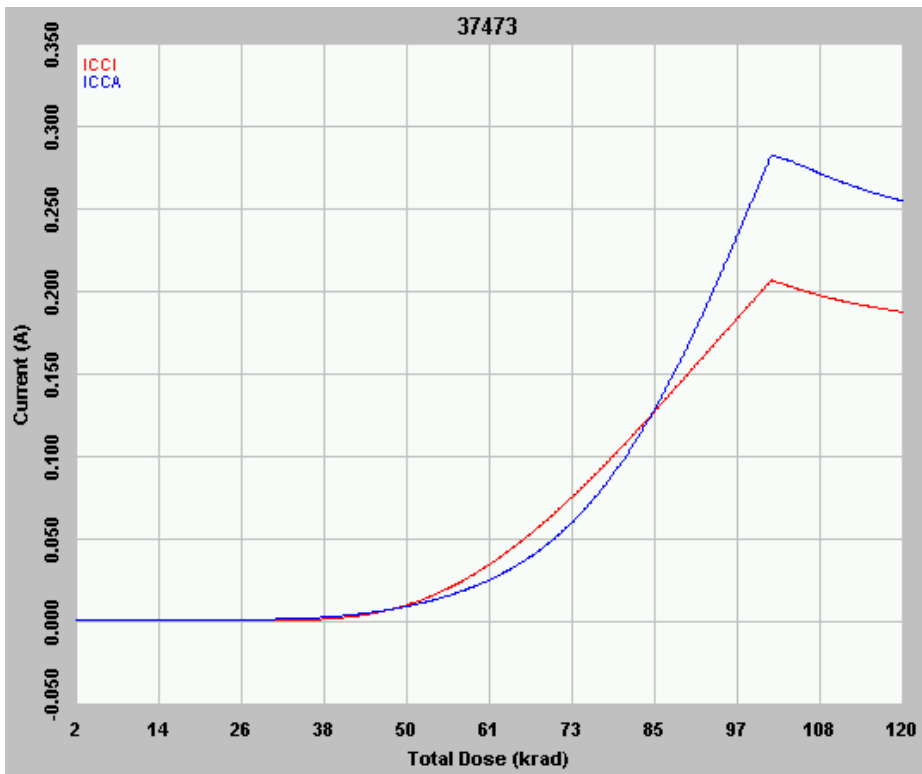Figure 4   DUT 37471 in-flux I_{CCA} and I_{CCI}

Figure 5   DUT 37473 in-flux I_{CCA} and I_{CCI}

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C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
37467	1.31	1.45	1.27	1.52
37468	1.32	1.46	1.27	1.51
37471	1.32	1.47	1.33	1.49
37473	1.31	1.45	1.23	1.47

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing number varies minutely with respect to the pre-irradiation number.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
37467	0.009	0.009	0.101	0.103	0.169	0.171	0.427	0.430	0.878	0.884
37468	0.009	0.009	0.101	0.103	0.169	0.171	0.426	0.430	0.876	0.887
37471	0.009	0.009	0.103	0.104	0.172	0.173	0.433	0.436	0.890	0.896
37473	0.009	0.009	0.102	0.104	0.171	0.173	0.431	0.436	0.885	0.897

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
37467	4.99	4.98	4.87	4.86	4.68	4.64	4.15	4.05	3.02	2.78
37468	4.99	4.98	4.88	4.86	4.68	4.65	4.16	4.08	3.09	2.85
37471	4.99	4.98	4.88	4.86	4.68	4.65	4.16	4.08	3.07	2.86
37473	4.99	4.98	4.87	4.86	4.67	4.66	4.13	4.09	3.00	2.90

E. Propagation Delay

Tables 7 and 8 list the pre-irradiation and post-annealing propagation delays, and also the radiation-induced degradations in percentage. DUT 37473 has the worst degradation of 10.08%.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Pre-Irradiation	Post-Annealing	Degradation
37467	1467.4	1557.8	6.16%
37468	1432.0	1466.2	2.39%
37471	1441.4	1482.1	2.83%
37473	1431.2	1575.4	10.08%

F. Transition Time

Figures 6 to 13 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition time degradation is not significant. Notice that in these Figures, the pre-irradiation time scale is different from the post-annealing time scale.
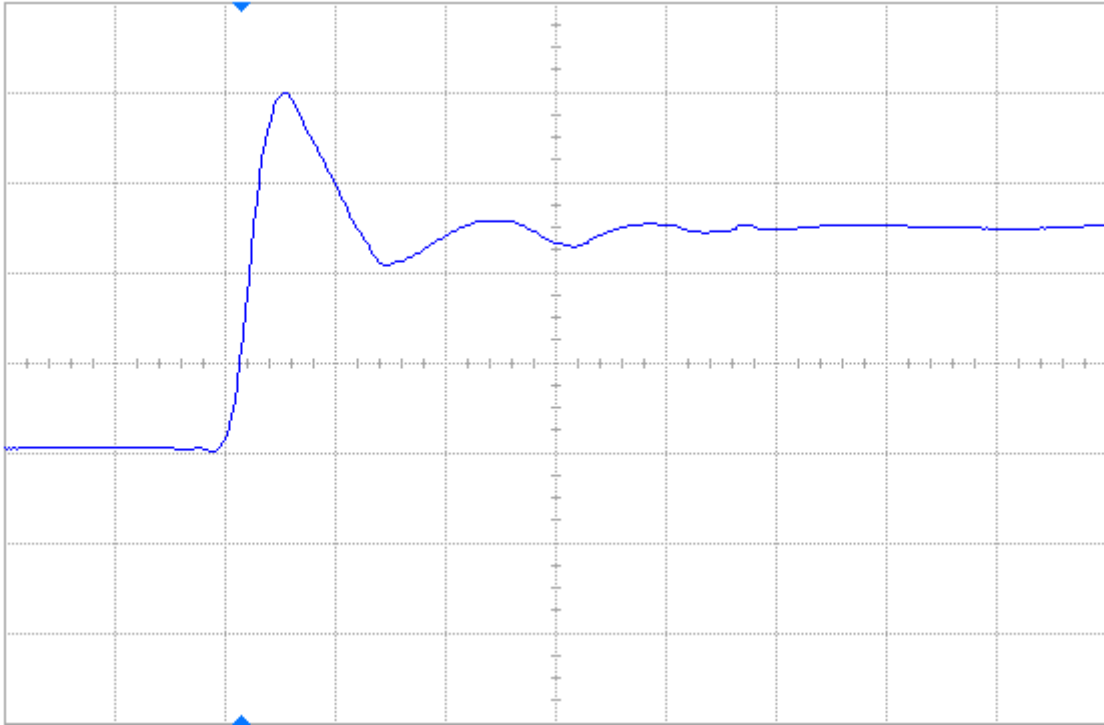
Figure 6(a)   DUT 37467 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.
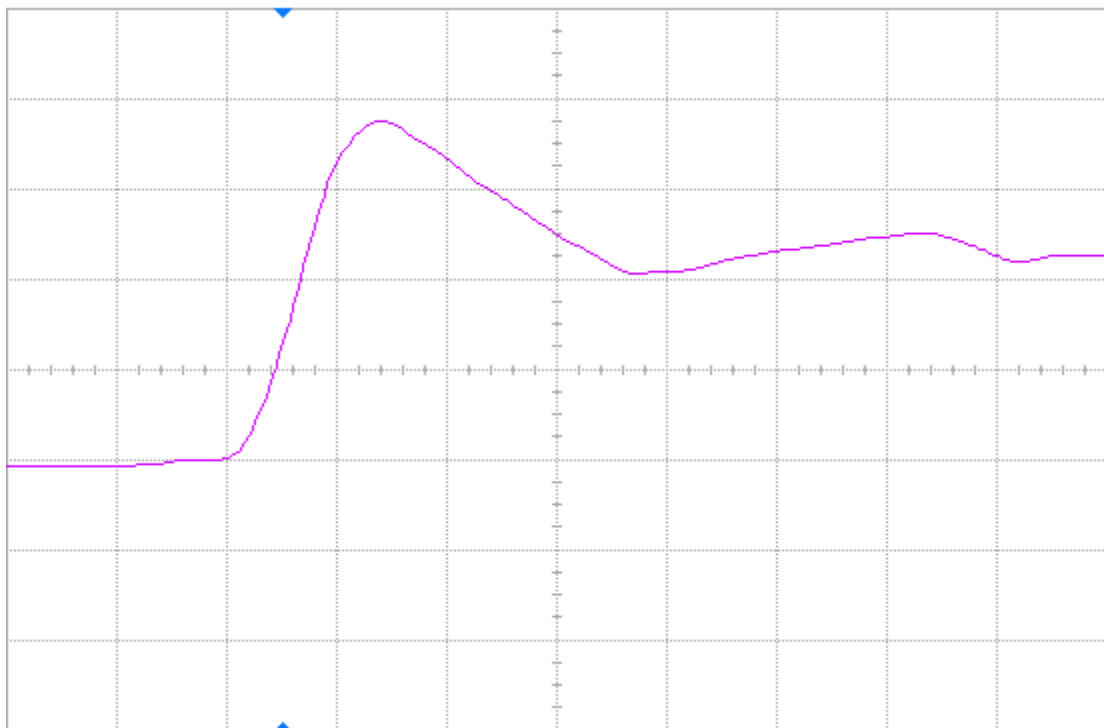
Figure 6(b)   DUT 37467 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
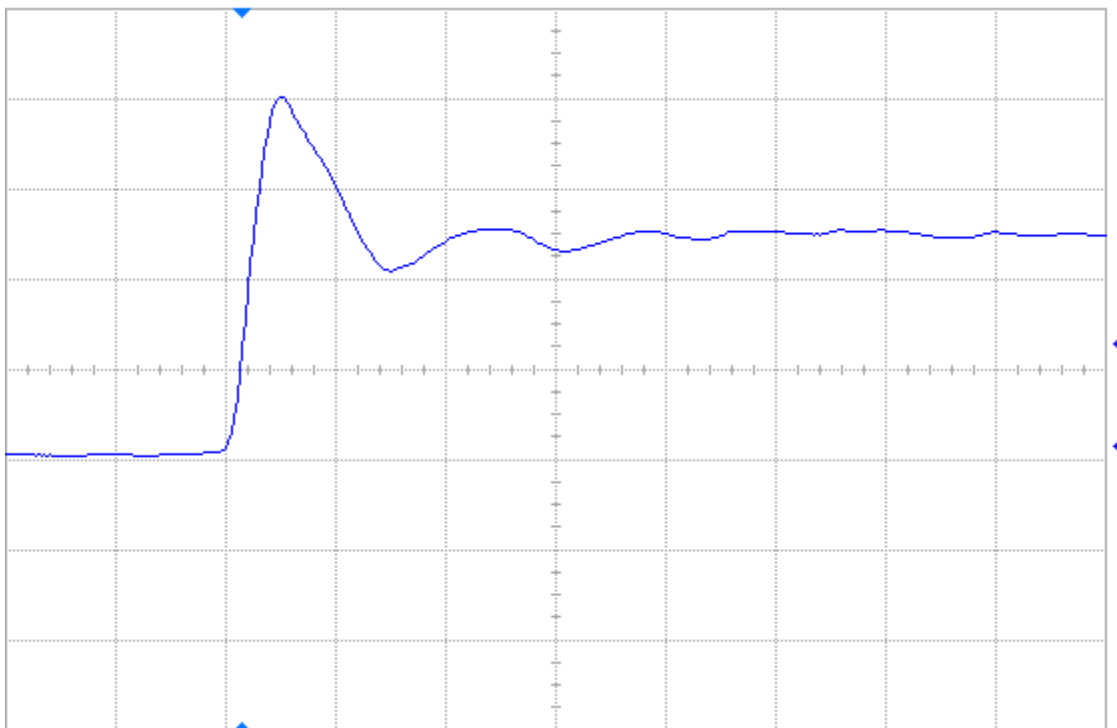
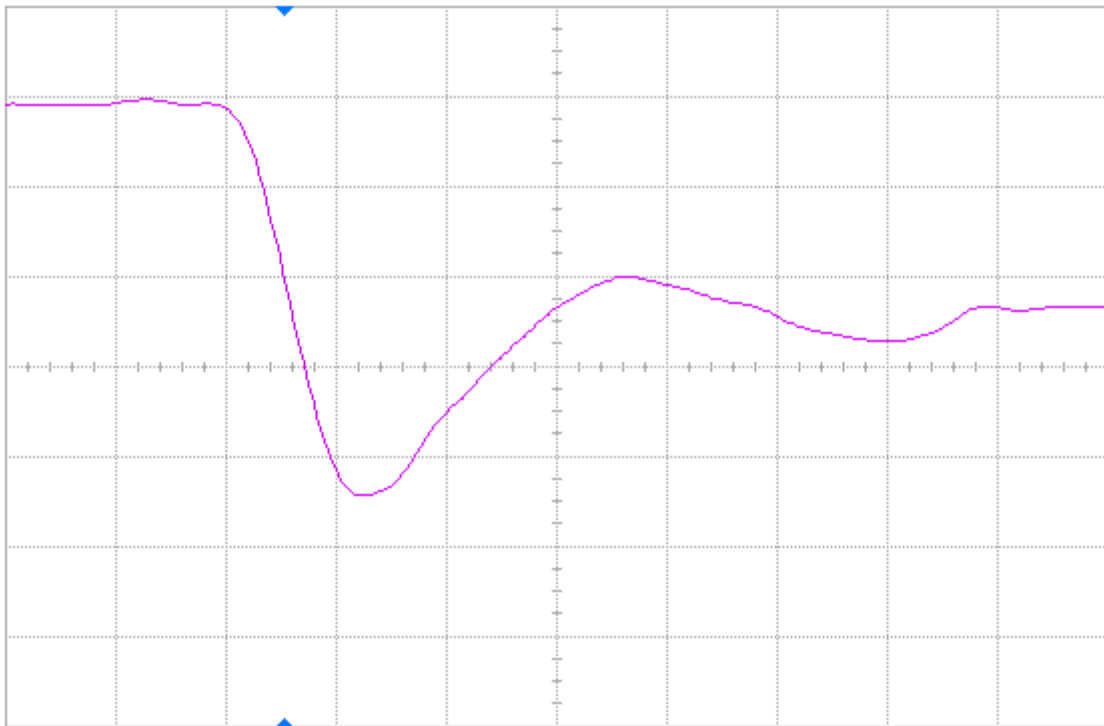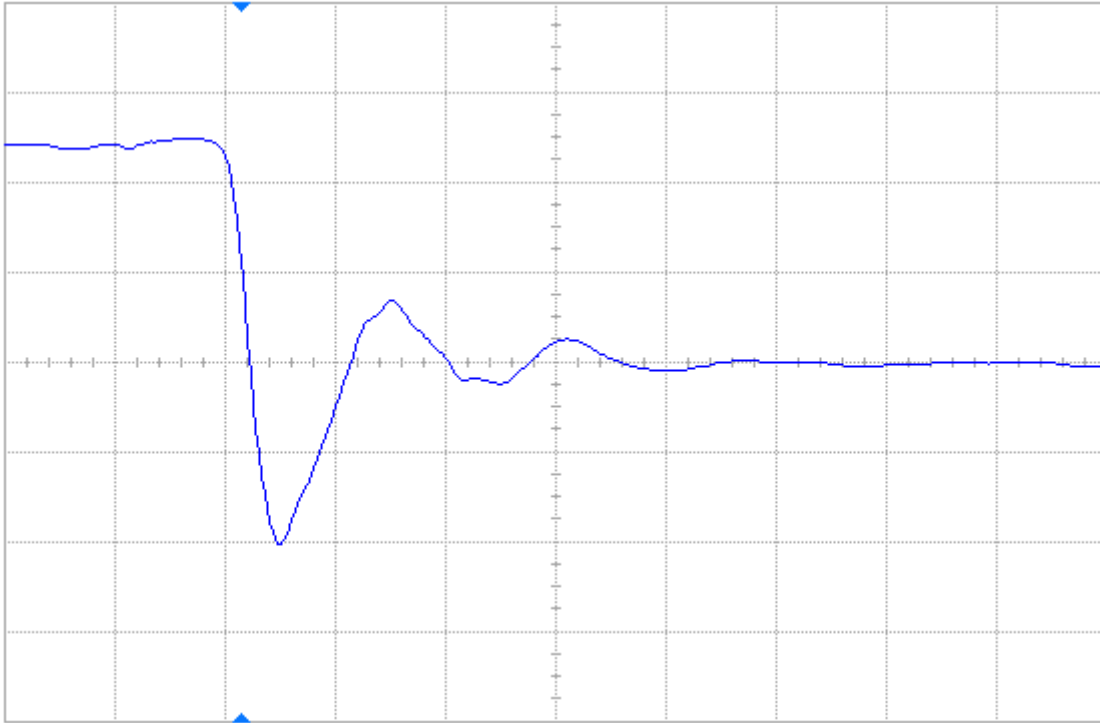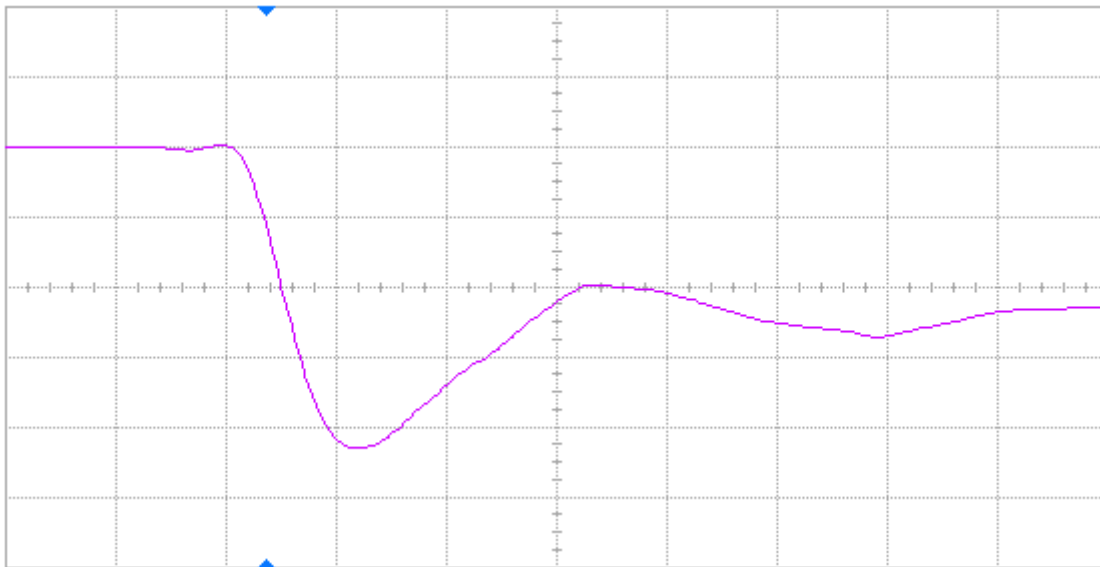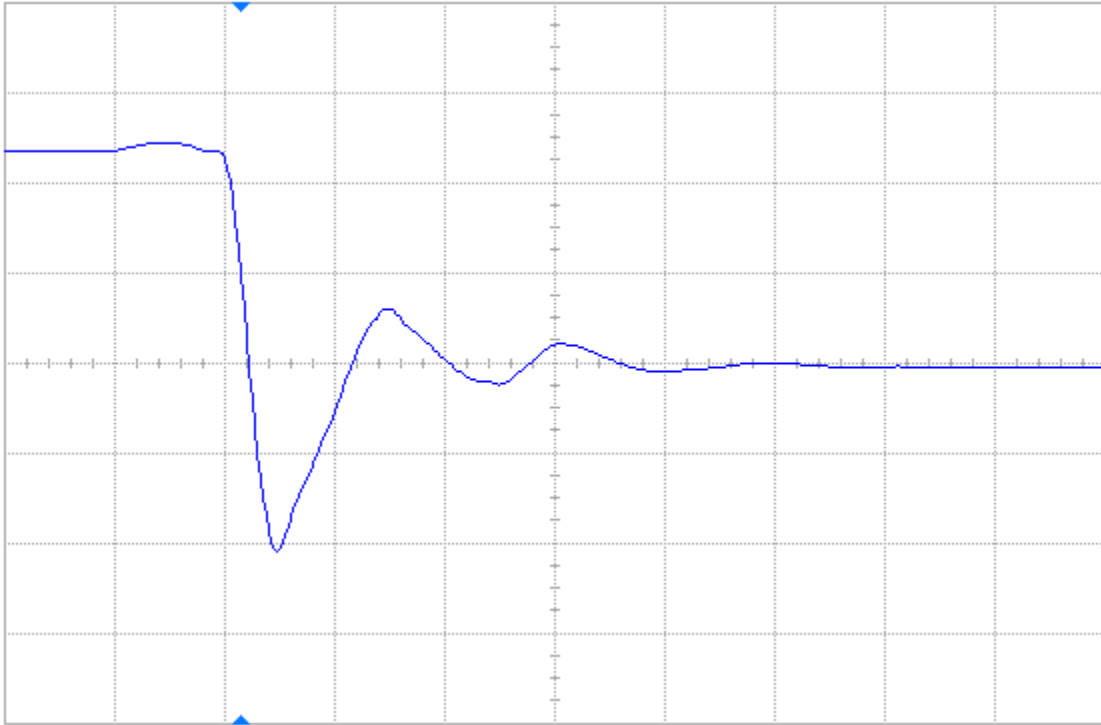Figure 7(a)   DUT 37468 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.
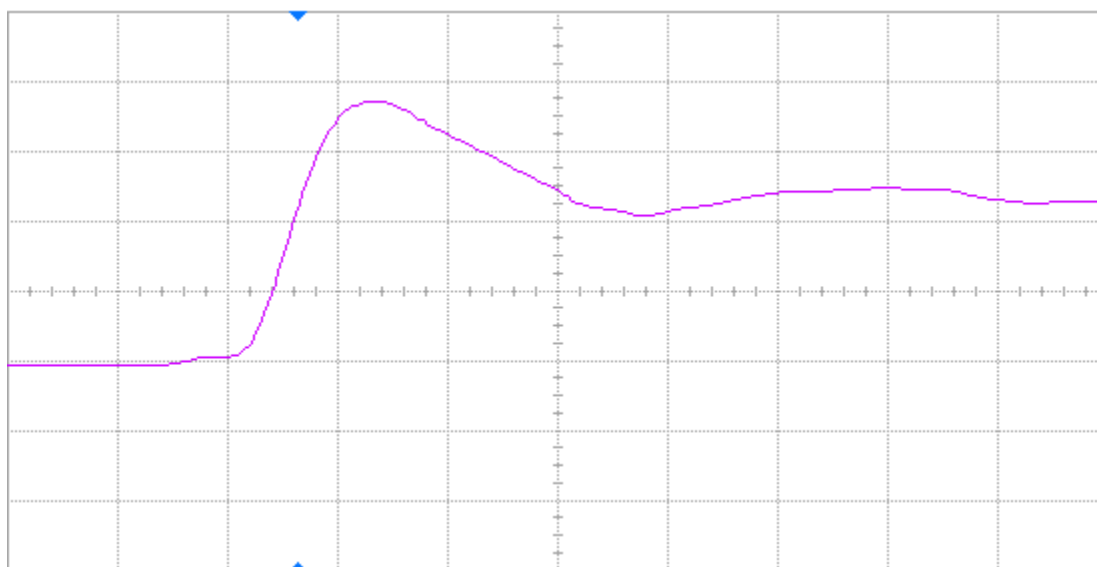
Figure 7(b)   DUT 37468 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
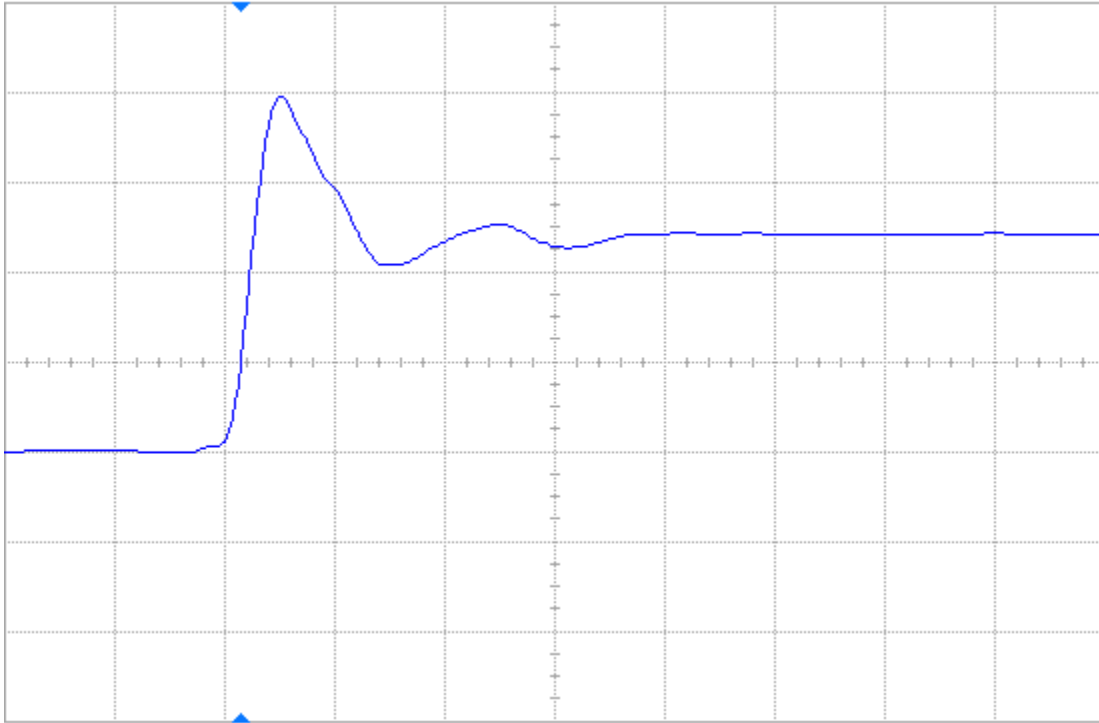
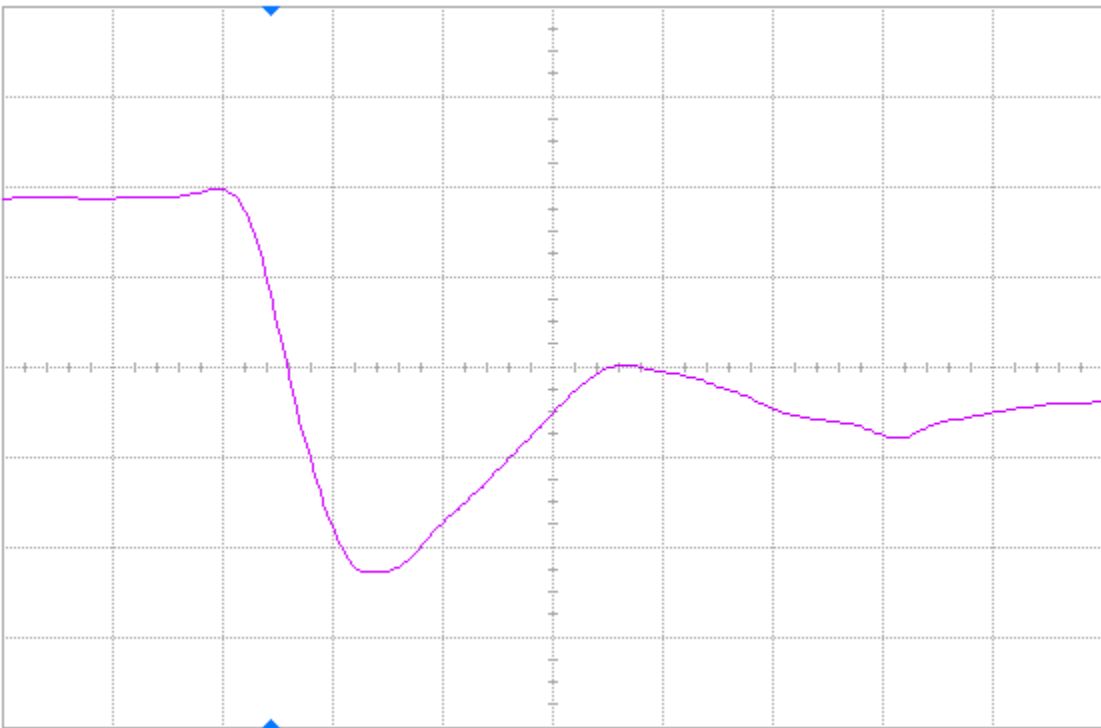Figure 8(a)   DUT 37471 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.
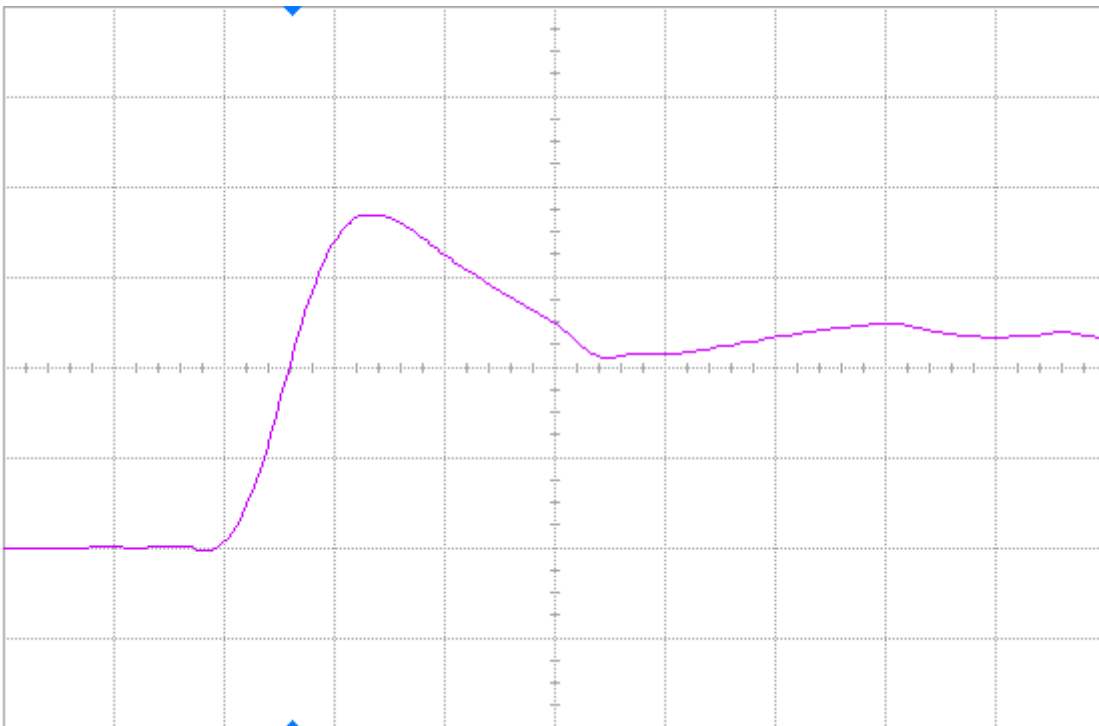
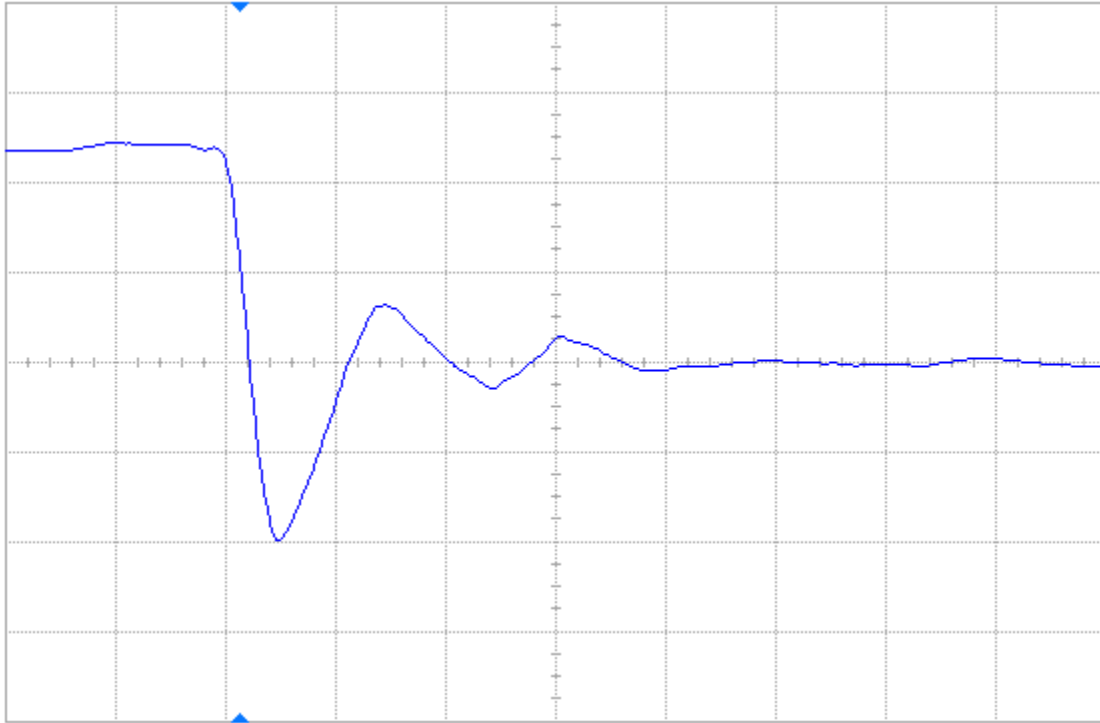Figure 8(b)   DUT 37471 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.
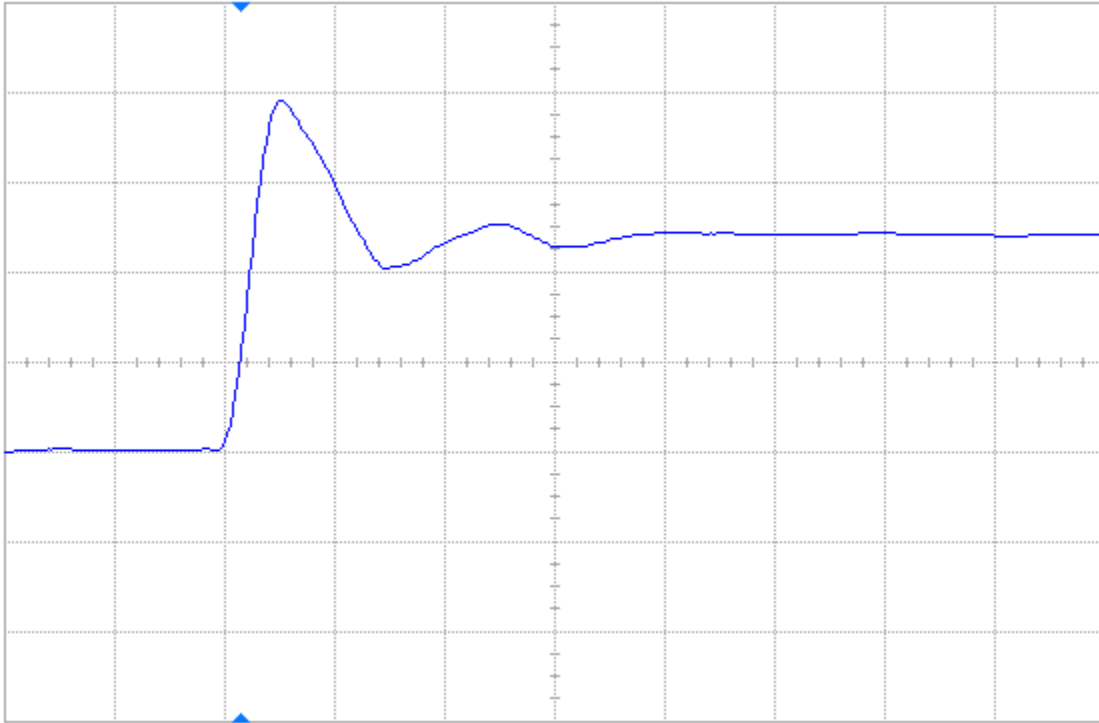
Figure 9(a)   DUT 37473 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.
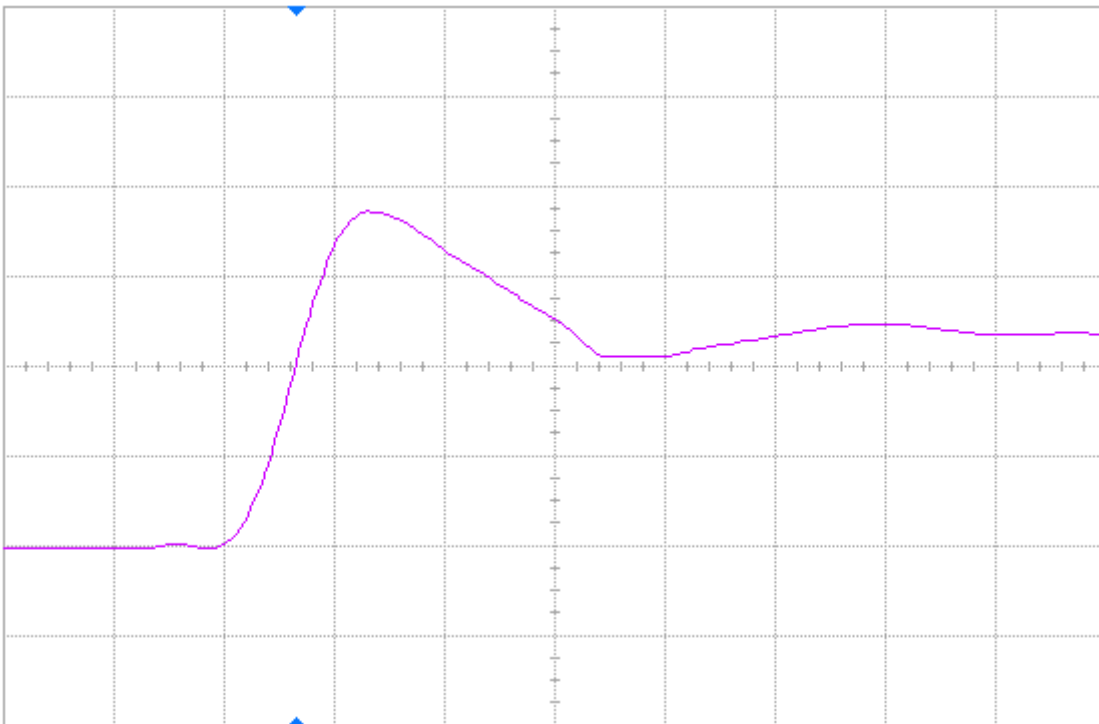
Figure 9(b)   DUT 37473 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

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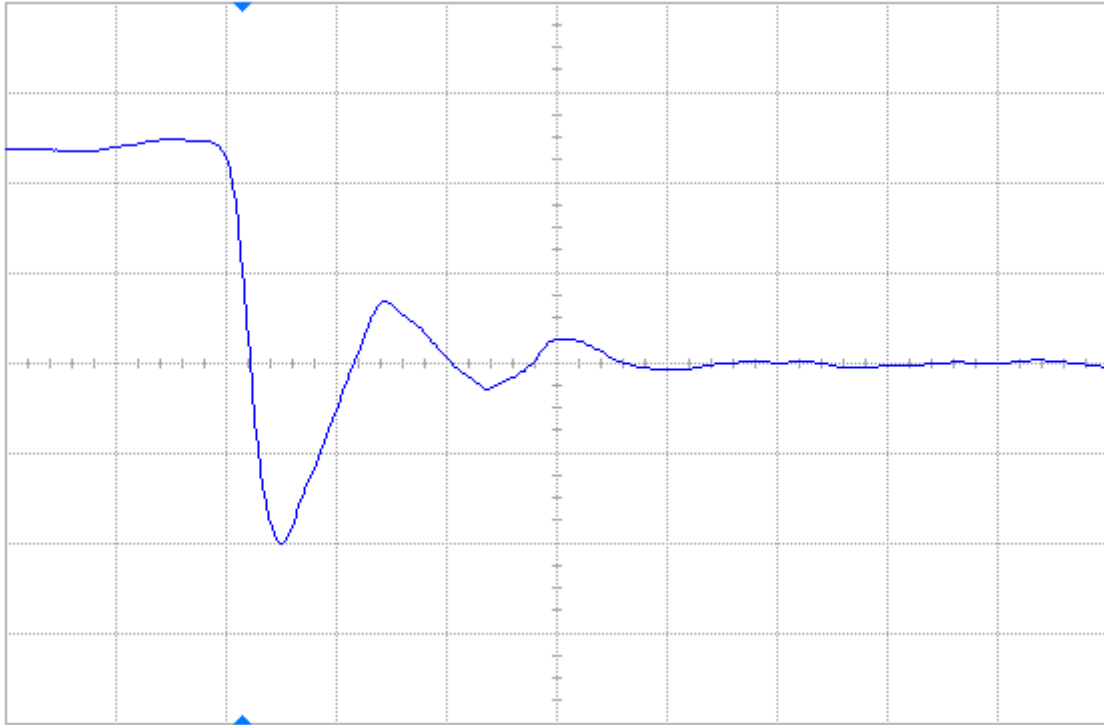
Figure 10(a) DUT 37467 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.
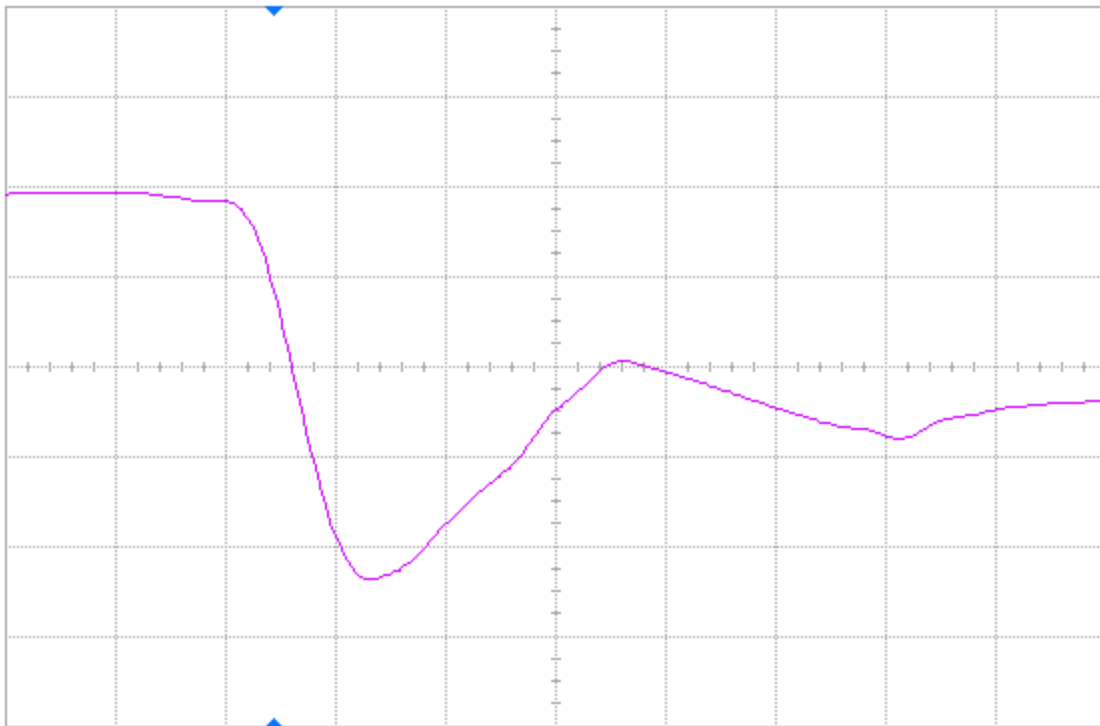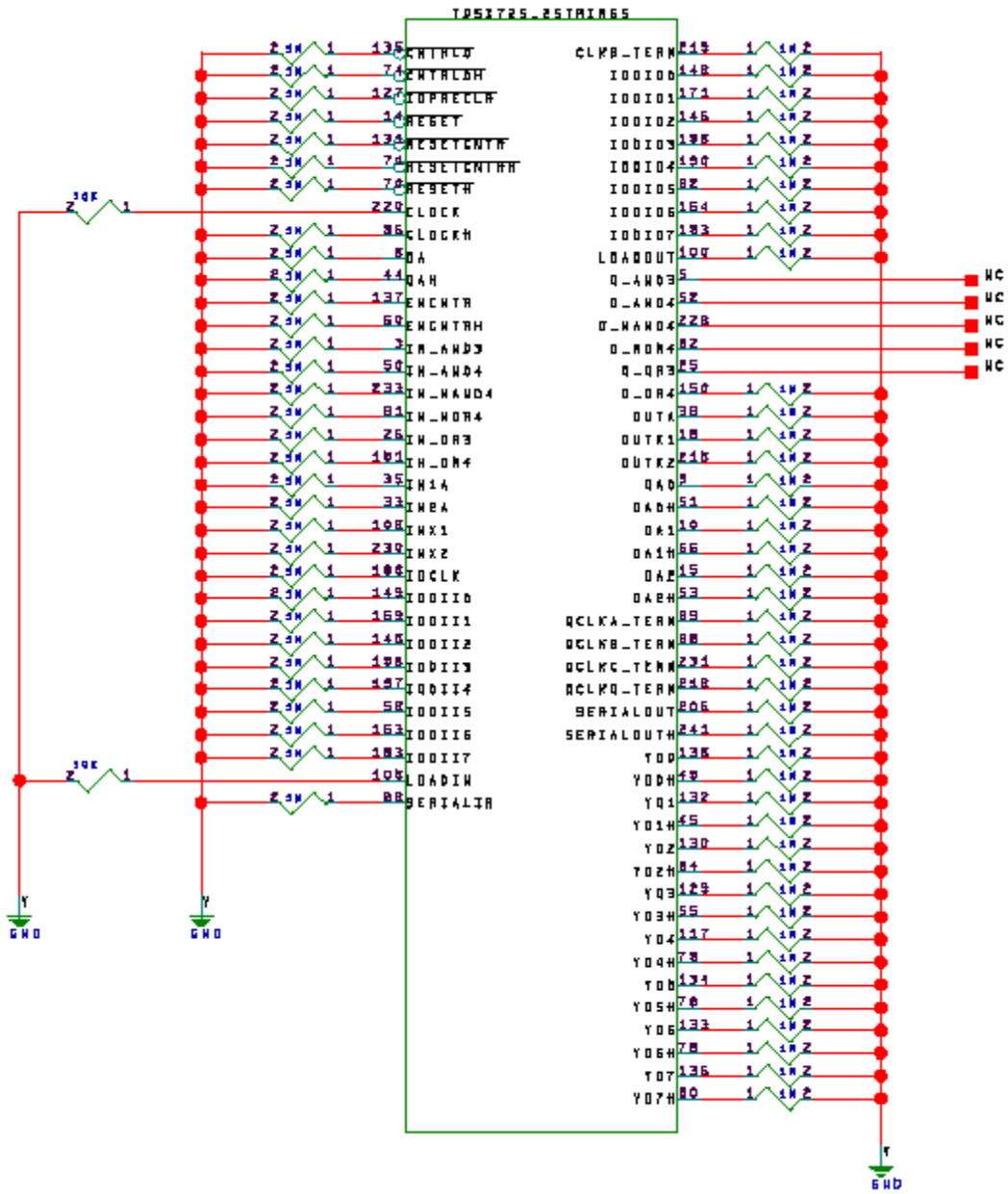

Figure 10(b) DUT 37467 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 11(a) DUT 37468 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.

Figure 11(b) DUT 37468 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 12(a) DUT 37471 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.

Figure 12(b) DUT 37471 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Figure 13(a) DUT 37473 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 5 ns/div.

Figure 13(b) DUT 37473 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

9K729CQ256

17	VCCI1	GND1 1
28	VCCI2	GND2 29
47	VCCI3	GND3 31
73	VCCI4	GND4 37
82	VCCI5	GND5 56
120	VCCI6	GND6 59
142	VCCI7	GND7 91
161	VCCI8	GND8 93
183	VCCI9	GND9 110
202	VCCI10	GND10 128
221	VCCI11	GND11 143
249	VCCI12	GND12 158
30	VCCA1	GND13 160
36	VCCA2	GND16 189
46	VCCA3	GND17 222
54	VCCA4	GND18 224
141	VCCA5	GND19 240
144	VCCA6	
162	VCCA7	
174	VCCA8	
228	VCCA9	
2	TDI	
11	TMS	
34	TRST	
256	TCK	

GND

GND

D0

D1

STRING 0: NON-INVERTING STRING, 1000 STAGES

STRING 1: NON-INVERTING STRING, 1000 STAGES

CLK

RESET

K-logic

K-logic

TDACT3SXCQ\BUF5ONINV

DRAWN BY: RBK

DATE:
REV.

INX1
INBUF
PAD

INX1

INX2
INBUF
PAD

INX2

TDSX72CQ256_2Strings

K-logic

DATE:
REV:

DRAWN BY:

CHECK0
CHECK1
CHECKSHIFTOUT

FUNC_RST
CLK

K-logic

TDSX72CQ256_2Strings

DRAWN BY:

DATE:
REV.

YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H

OUTBUF
OUTBUF
OUTBUF
OUTBUF
OUTBUF
OUTBUF
OUTBUF
OUTBUF

PAD
PAD
PAD
PAD
PAD
PAD
PAD
PAD

D
D
D
D
D
D
D
D

RESETCNTRH
INBUF
PAD

ENCNTRH
INBUF
PAD

Y

Y

RESETCNTRH

ENCNTRH

CNTRLDH
INBUF
PAD

Y

CNTRLDH
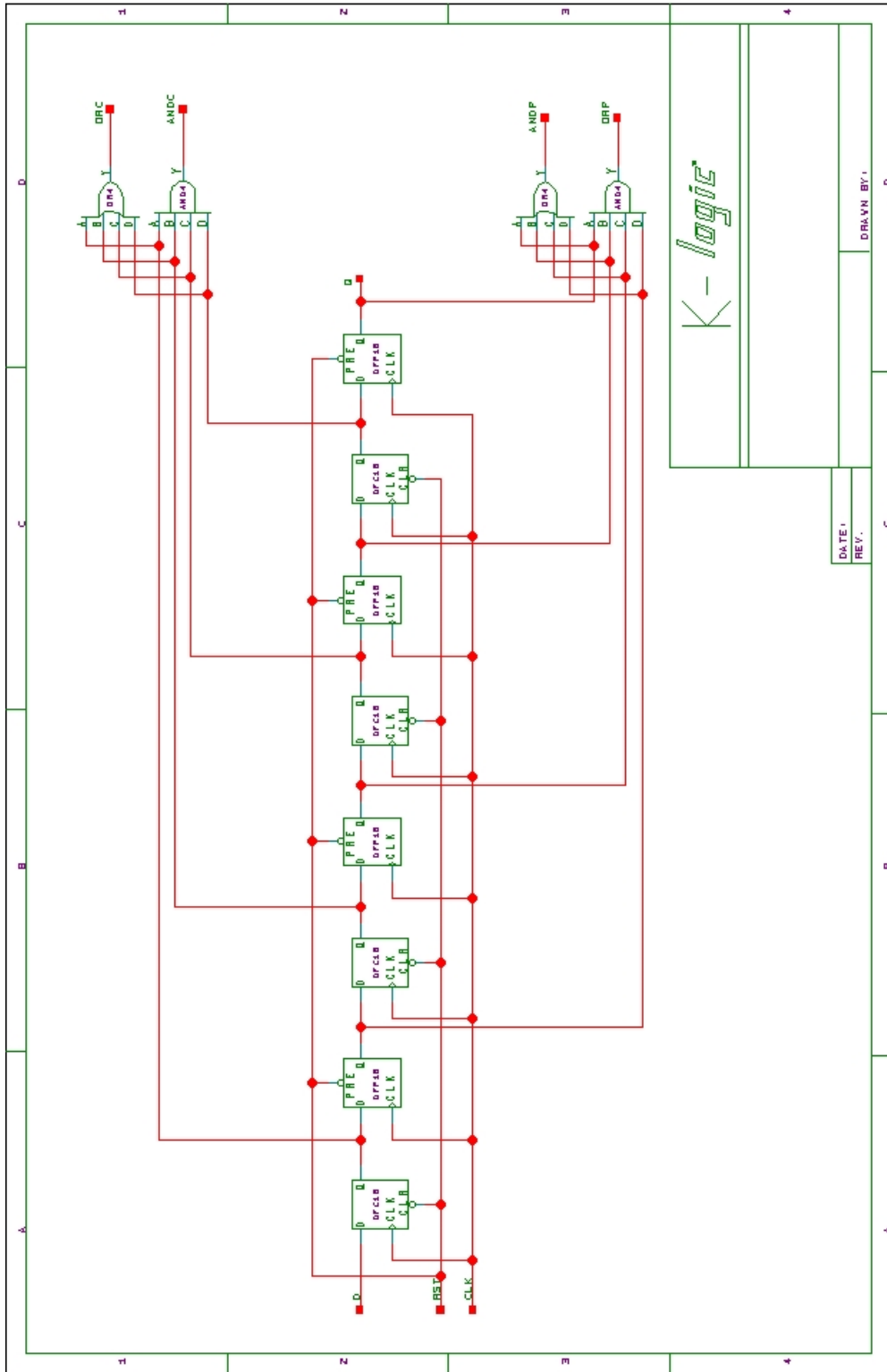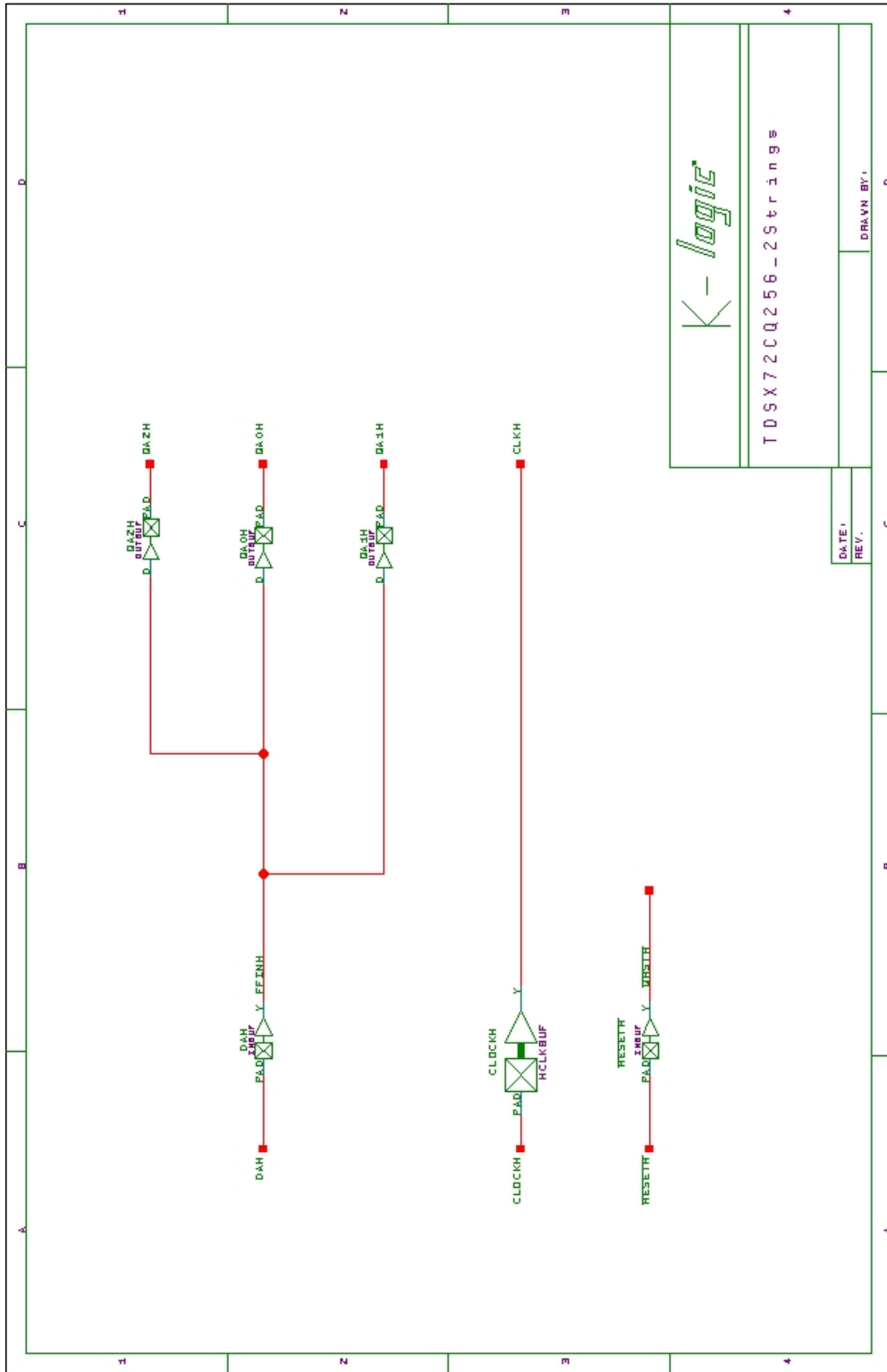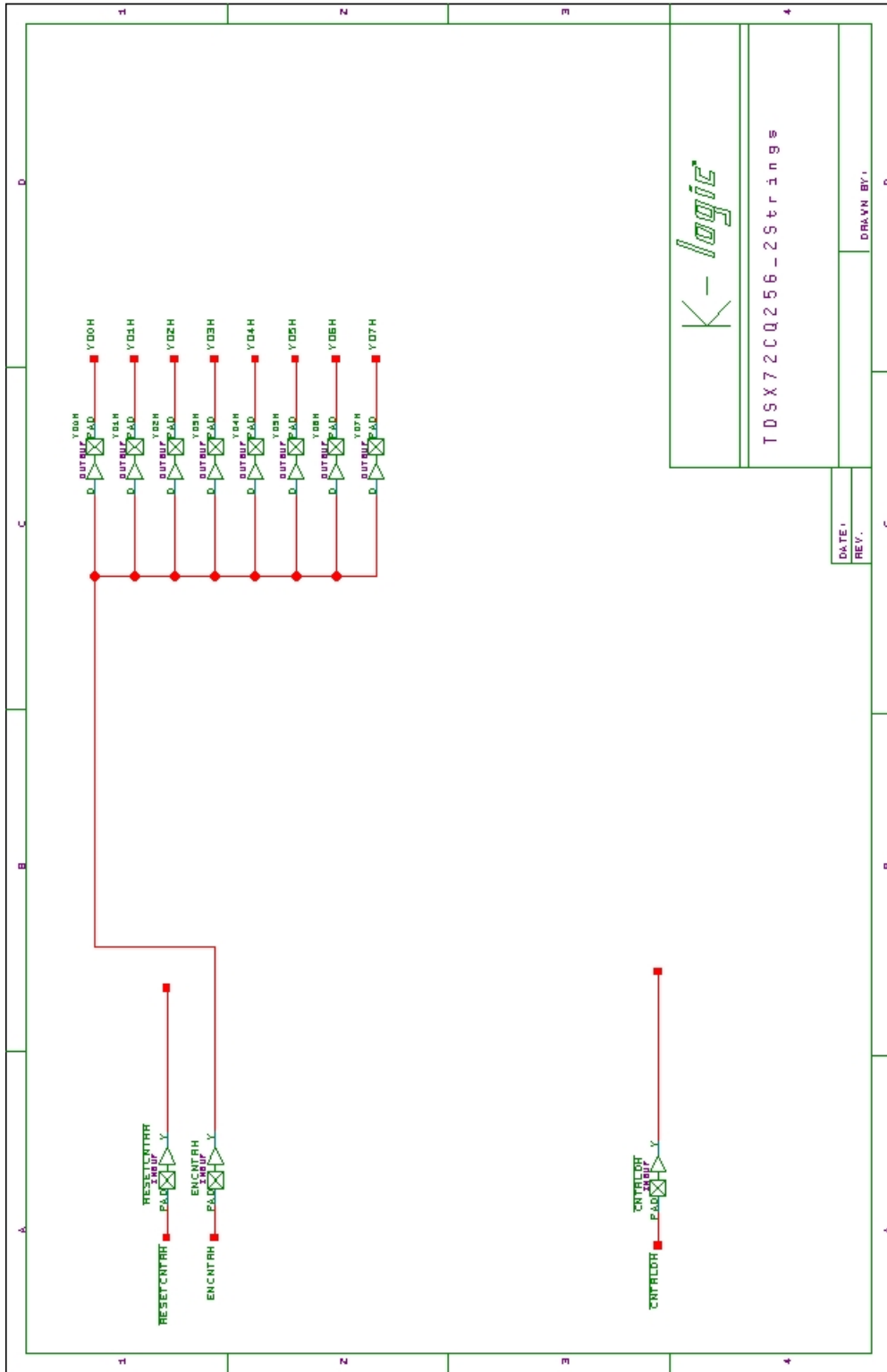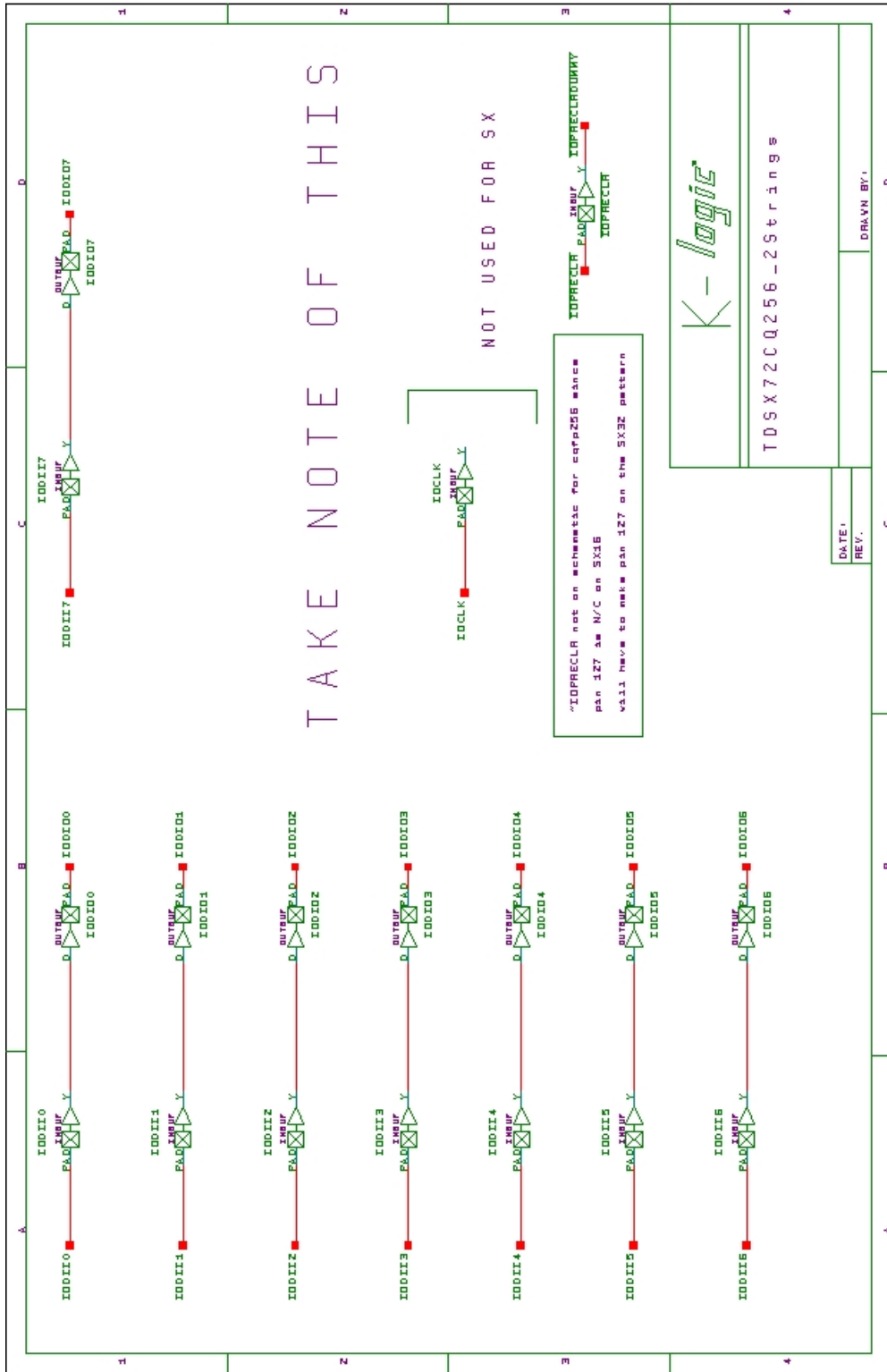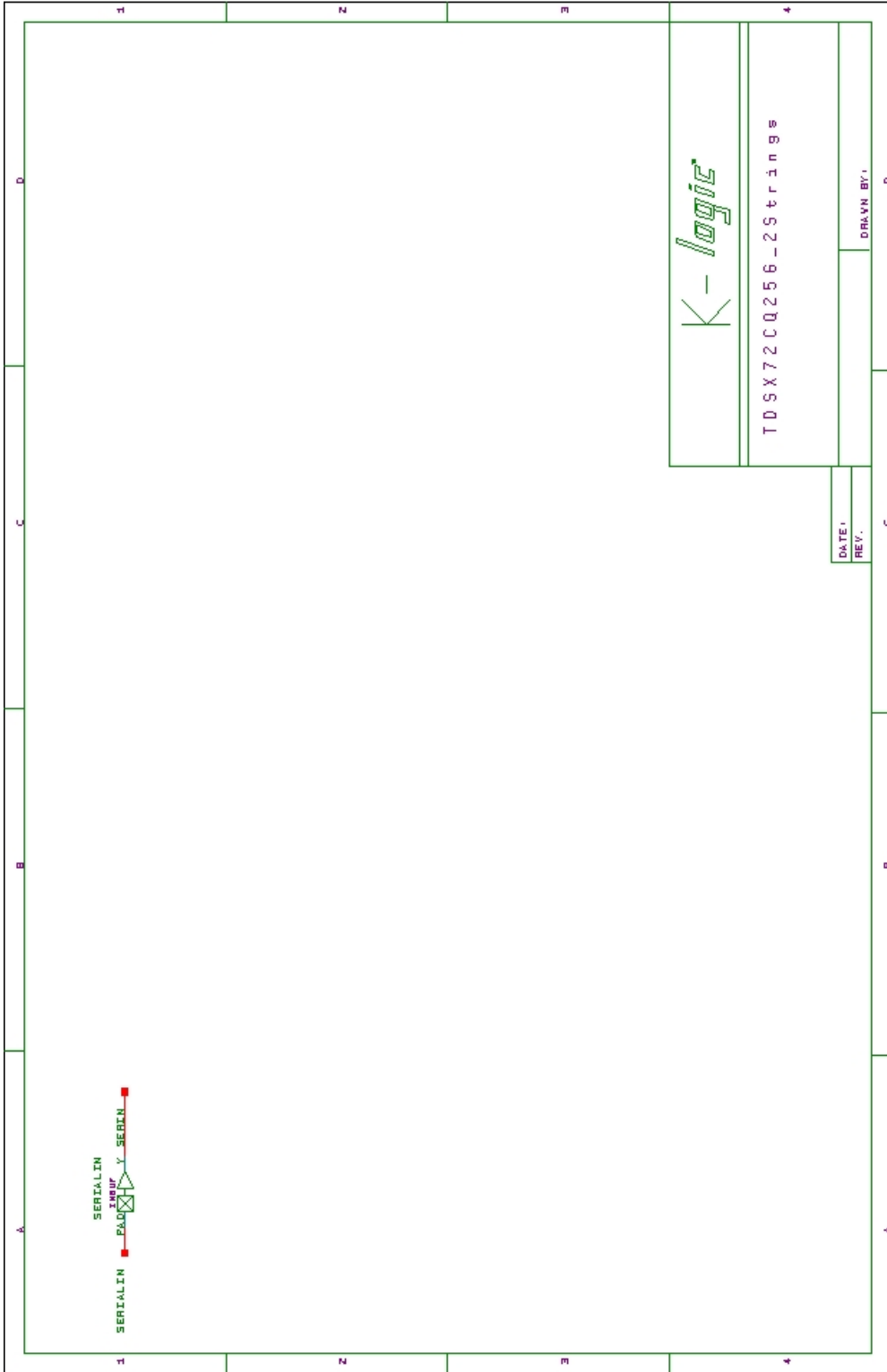
K-logic

TDSX72CQ256_2Strings

DATE:
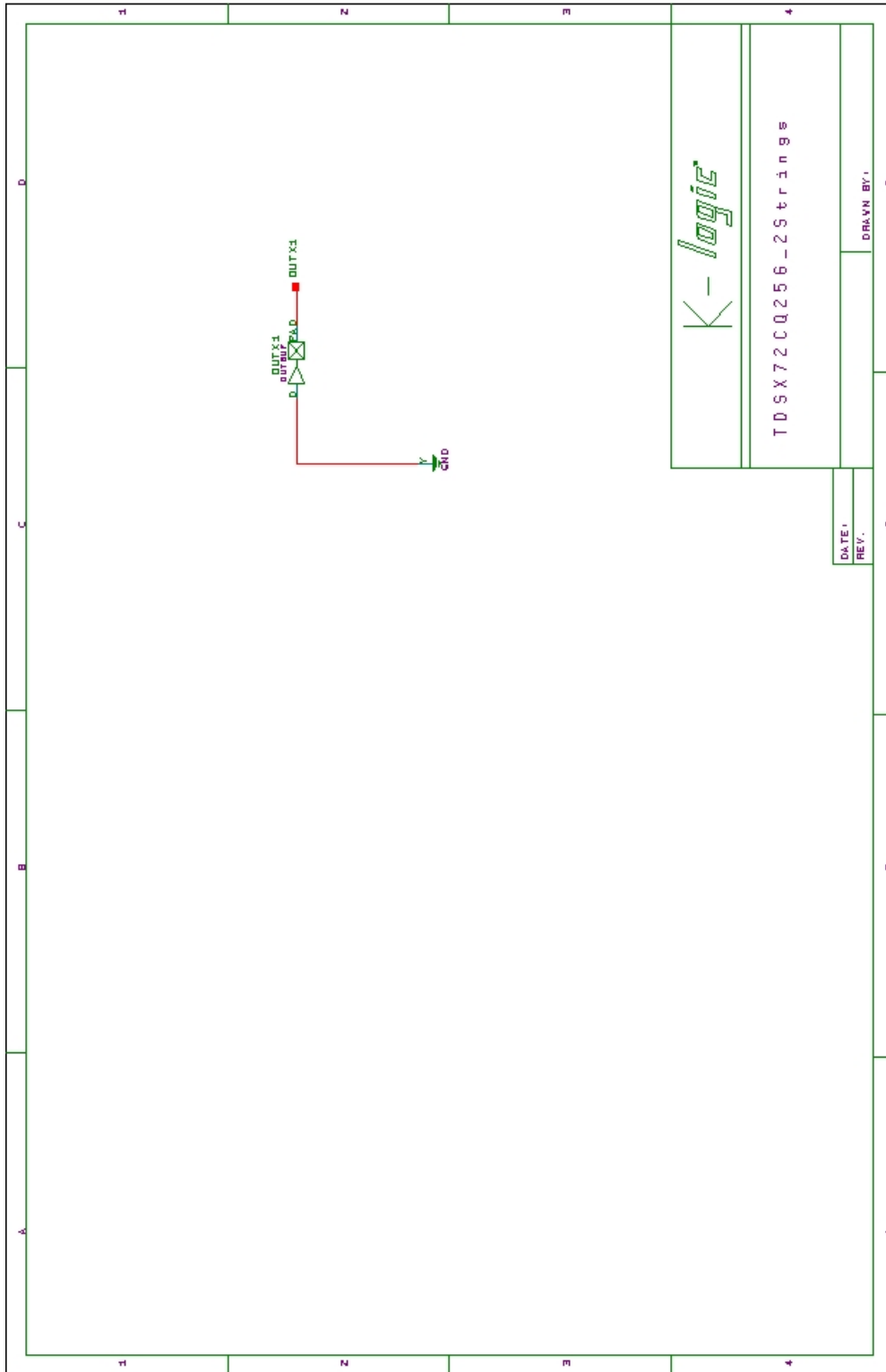REV.

DRAWN BY:

30

TAKE NOTE OF THIS

NOT USED FOR SX

IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on Sx16
will have to make pin 127 on the Sx32 pattern

K-logic

TDSX72CQ256_2Strings

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DATE:
REV:

IOCLK

IOPRECLR   IOPRECLRDUMMY
IOPRECLR

IODII7   IODIO7

IODII0 IODIO0
IODII1 IODIO1
IODII2 IODIO2
IODII3 IODIO3
IODII4 IODIO4
IODII5 IODIO5
IODII6 IODIO6

OUTx1

OUTx1
OUTBUF
PAD
D

Y
GND

OUTx1

K-logic

TDSX72CQ256_2Strings

DRAWN BY:

DATE:
REV.