TOTAL IONIZING DOSE TEST REPORT

No. 08T-RTAX4000S-CQ352-D31CF1
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I. Summary Table

Table 1 summarizes the TID tolerance for each tested parameter. The overall tolerance is limited by the standby power-supply current (I_{CC}). Because of logistical limitations, the room temperature annealing allowed by 1019.6 to anneal down I_{CC} is performed only for approximately 10 days. Every DUT passes the major specs listed in the table for 300 krad(SiO_2) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO_2)
2. Standby Power Supply Current (I_{CCA}/I_{CCI})	Passed 300 krad(SiO_2)
3. Input Switching Threshold (V_{IHL}/V_{ILH})	Passed 300 krad(SiO_2)
4. Output Threshold (V_{OL}/V_{OH})	Passed 300 krad(SiO_2)
5. Propagation Delay	Passed 300 krad(SiO_2) for ±10% degradation criterion
6. Transition Time	Passed 300 krad(SiO_2)

II. Total Ionizing Dose (TID) Testing

This section describes the device under test (DUT), irradiation facility and parameters, test method, test design, and electrical parameter measurements. This TID testing, in various slightly modified forms, has been used to build an extensive TID database for many generations of antifuse-based FPGAs. The link to access this TID database is attached in below:

http://www.actel.com/products/milaero/hireldata.aspx#tid

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation each input is grounded; during annealing each input or output is tied to the ground or V_{CCI} with a 2.7 k ohm resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Device	RTAX4000S
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 μm CMOS
DUT Design	Master_RTAX4000S_CQ352_Design
Die Lot Number	D31CF1
Quantity Tested	5
Serial Number	200 krad: 4918, 4930 300 krad: 4876, 4899, 4909
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL

B. Test Method

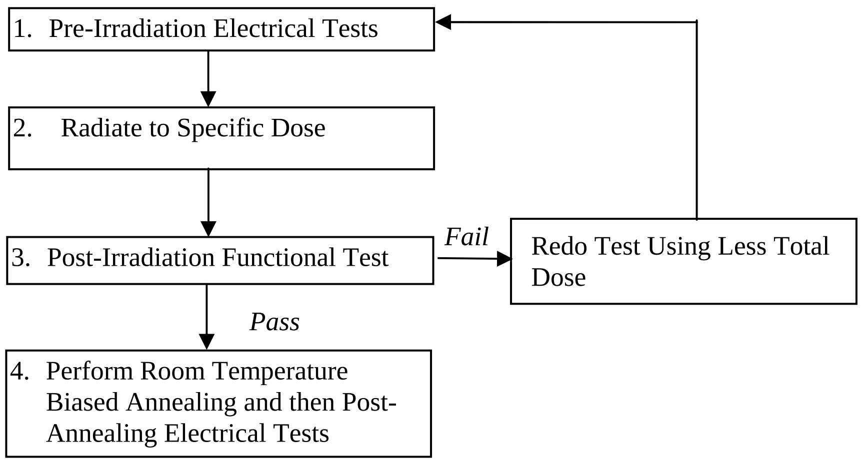

Figure 1 Parametric test flow chart

The test method is based on the military standard TM1019.6. Figure 1 shows the test flow. During irradiation, the DUT is statically biased with V_{CCI}/V_{CCA} = 3.3V/1.5V and all the inputs grounded. The accelerated annealing test in TM1019.6, section 3.12 had been done on samples of the RTAXS family, and the results indicate that post-irradiation annealing recovers the electrical characteristics rather than adversely affecting the electrical performance. This is consistent with the general belief that the dominant TID effects in deep submicron CMOS devices are due to oxide-trapped-hole induced leakage currents. These leakages decrease with the annealing temperature. Consequently, for this lot testing, the accelerated annealing test is omitted.

TM1019.6, Section 3.11 “Extended room temperature anneal test” has been applied for approximately 10-days of annealing. The data measured after this annealing is termed “Post Annealing” in section III, Test Results.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (Master_RTAX4000S_Design) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1MHz and 50MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-S/SL

SUPPLY VOLTAGE	MINIMUM	RECOMMENDE D	MAXIMUM
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V V_{CCDA} I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic threshold (V_{IL}/V_{IH}) is measured on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (V_{OL}/V_{OH}) is measured on single-ended outputs Global_Monitor_EAQ, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_1, Array_out_EAQ_1, Array_out_EAQ_2, PADN_LVPECL_1, PADN_LVPECL_0, PADP_LVPECL_1, PADP_LVPECL_0, Shiftout3, Shiftout7, and Shiftout8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{IL}/V_{IH})	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (V_{OL}/V_{OH})	Single-ended outputs (Global_Monitor_EAQ, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_1, Array_out_EAQ_1, Array_out_EAQ_2, PADN_LVPECL_1, PADN_LVPECL_0, PADP_LVPECL_1, PADP_LVPECL_0, Shiftout3, Shiftout7, Shiftout8)
5. Propagation Delay	String of NAND4-inverters. Measured from HClock1 input to delay_out_SEU0, delay_out_SEU1, delay_out_SEU2, delay_out_SEU3, and delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. *Functionality*

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. *Standby Power Supply Current (I_{CCA} and I_{CCI})*

The logic-array power supply (V_{CCA}) is 1.5V, and the IO power supply (V_{CCI}) is 3.3V. Their standby currents, I_{CCA} and I_{CCI}, are monitored in-flux. Figure 2-6 show the in-flux I_{CCA} and I_{CCI} versus total dose for the DUTs.

Referring to TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} should be defined as the addition of highest I_{CCI}, I_{CCDA} and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS spec sheet in the document posted on the Actel website; the link is

http://www.actel.com/documents/RTAXS_DS.pdf

Therefore, the PIPL for I_{CCA} is 500 mA, and the PIPL for I_{CCI} is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before annealing, and post-annealing I_{CCA} and I_{CCI} data: the post-annealing I_{CCA} of every DUT, either irradiated to 200 krad(SiO_2) or 300 krad(SiO_2) is below the PIPL, and the post-annealing I_{CCI} of every DUT irradiated to 200 krad(SiO_2) or 300 krad(SiO_2) is below the PIPL.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad(SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
4876	300	10	165	23	7	121	37
4899	300	10	177	25	7	118	36
4909	300	10	119	22	7	147	42
4918	200	10	20	13	7	58	23
4930	200	9	19	11	7	54	22

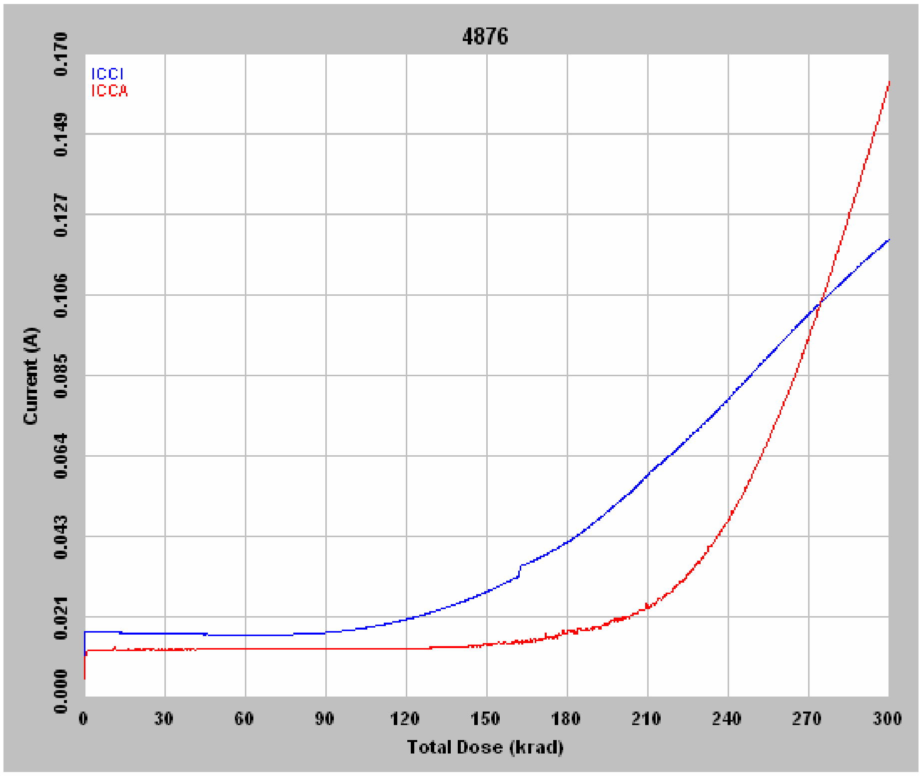

Figure 2 DUT 4876 in-flux I_{CCA} and I_{CCI}

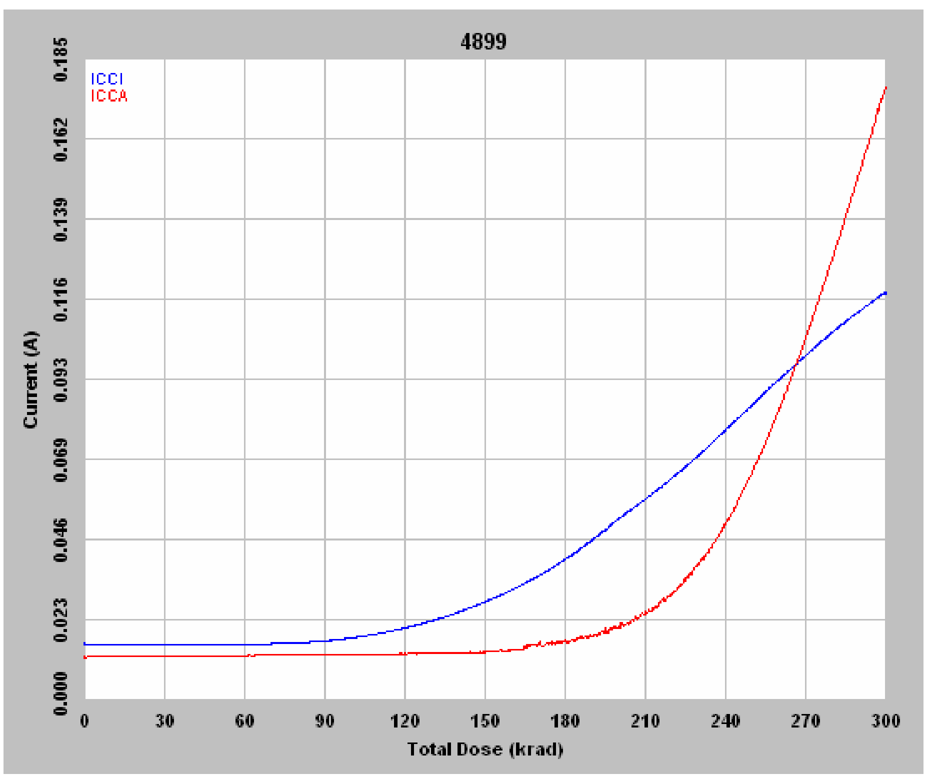

Figure 3 DUT 4899 in-flux I_{CCA} and I_{CCI}

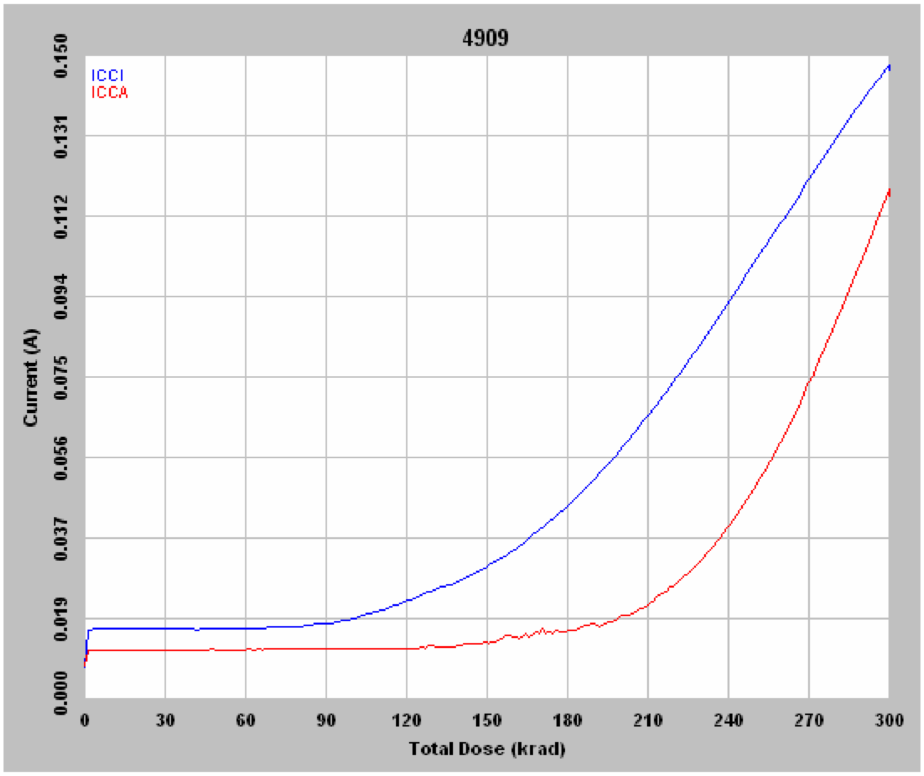

Figure 4 DUT 4909 in-flux I_{CCA} and I_{CCI}

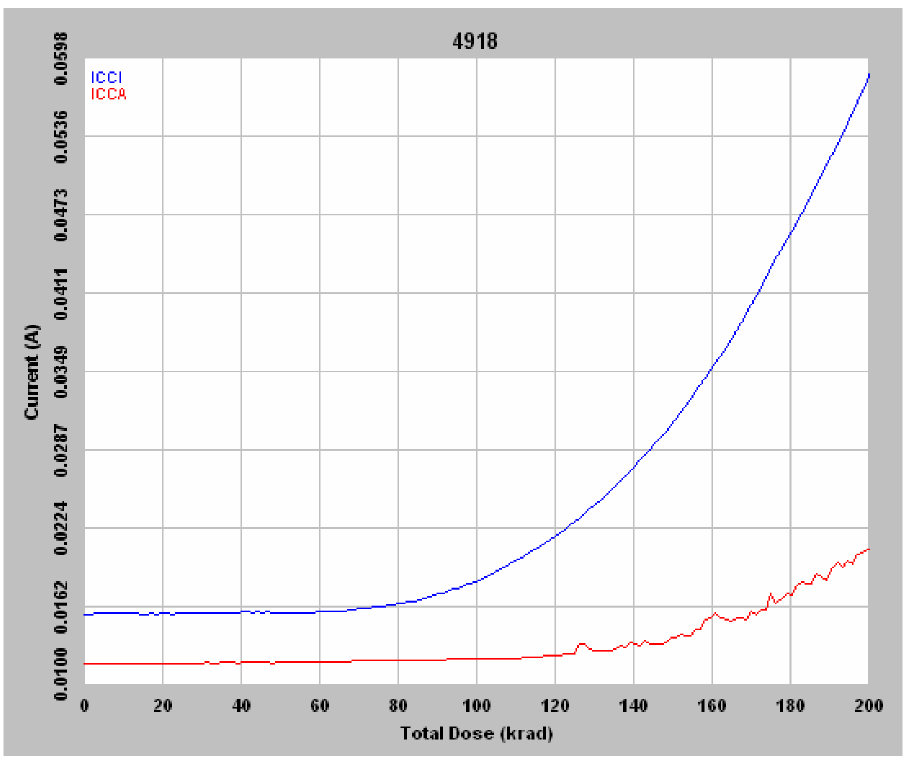

Figure 5 DUT 4918 in-flux I_{CCA} and I_{CCI}

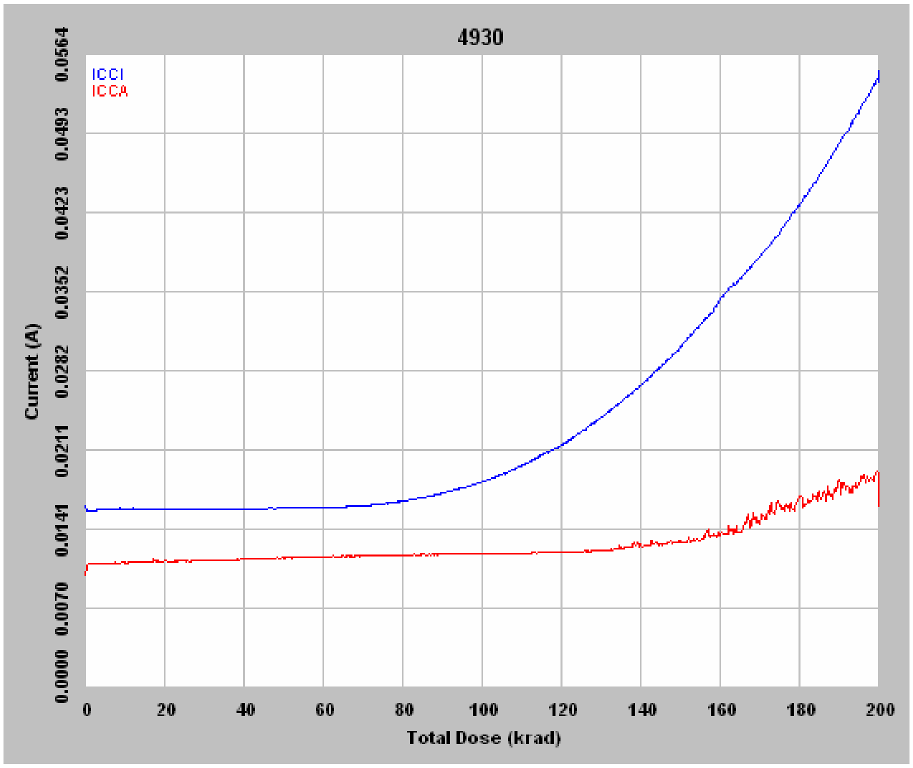

Figure 6 DUT 4930 in-flux I_{CCA} and I_{CCI}

C. *Single-Ended 3.3V-LVTTL V_{IHL}/V_{ILH}*

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design–often just input and output buffers–starts to switch: V_{IH} is the input trip point when the input is going high to low; V_{IL} is the input trip point when the input is going low to high.

Tables 6a and 6b list the pre-irradiation and post-annealing single-ended V_{IL}. In each case, the difference between the pre-irradiation and post-annealing data is negligibly small. Tables 7a and 7b show the pre-irradiation and post-annealing single-ended V_{IH}. Again, the difference between the pre-irradiation and post-annealing data is negligibly small.

Table 6a Pre-Irradiation and Post-Annealing Input Thresholds (V_{IL})

	4876		4899		4909	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.37	1.36	1.37	1.37	1.38	1.37
Shiftin7	1.36	1.35	1.36	1.35	1.37	1.36
Shiftin5	1.36	1.35	1.36	1.35	1.37	1.36
Shiftin4	1.37	1.36	1.37	1.37	1.37	1.37
Shiftin3	1.37	1.37	1.37	1.37	1.37	1.37
Shiftin2	1.36	1.34	1.36	1.35	1.36	1.35
Shiftin1	1.37	1.36	1.37	1.37	1.37	1.37
SEU_sel	1.36	1.35	1.36	1.35	1.37	1.36
zoom_sel_n_0	1.37	1.37	1.38	1.37	1.38	1.37
zoom_sel_n_1	1.38	1.37	1.38	1.37	1.38	1.38
zoom	1.38	1.37	1.37	1.37	1.38	1.37
TOG_n	1.36	1.35	1.36	1.35	1.37	1.36

	4918		4930	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.38	1.37	1.38	1.37
Shiftin7	1.37	1.36	1.36	1.35
Shiftin5	1.37	1.36	1.36	1.36
Shiftin4	1.37	1.37	1.37	1.37
Shiftin3	1.38	1.37	1.38	1.37
Shiftin2	1.37	1.36	1.36	1.35
Shiftin1	1.38	1.37	1.37	1.37
SEU_sel	1.37	1.36	1.37	1.36
zoom_sel_n_0	1.38	1.37	1.38	1.37
zoom_sel_n_1	1.38	1.37	1.38	1.37
zoom	1.38	1.37	1.37	1.37
TOG_n	1.36	1.35	1.36	1.35

Table 6b Pre-Irradiation and Post-Annealing Input Thresholds (V_{IL})

	4876		4899		4909	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.36	1.35	1.37	1.36	1.37	1.36
Resetn	1.37	1.36	1.37	1.37	1.38	1.37
oe_EAQ	1.37	1.36	1.37	1.37	1.37	1.37
enable_HSB	1.36	1.35	1.36	1.35	1.36	1.35
IO_Pattern_Length_1	1.38	1.37	1.38	1.37	1.38	1.37
IO_Pattern_Length_2	1.36	1.35	1.37	1.36	1.37	1.36
A_Pattern_Length_0	1.36	1.35	1.36	1.35	1.36	1.35
A_Pattern_Length_1	1.38	1.37	1.38	1.37	1.38	1.38
IO_Pattern_Length_0	1.37	1.36	1.38	1.37	1.38	1.37
ctest_done_sel_2	1.37	1.36	1.37	1.37	1.38	1.37
IO_Johnson	1.37	1.36	1.37	1.36	1.37	1.37
A_Johnson	1.36	1.35	1.36	1.35	1.36	1.35

	4918		4930	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.37	1.36	1.36	1.35
Resetn	1.37	1.37	1.37	1.37
oe_EAQ	1.38	1.37	1.38	1.37
enable_HSB	1.37	1.36	1.37	1.35
IO_Pattern_Length_1	1.38	1.37	1.37	1.37
IO_Pattern_Length_2	1.36	1.36	1.36	1.35
A_Pattern_Length_0	1.36	1.35	1.36	1.35
A_Pattern_Length_1	1.38	1.37	1.38	1.37
IO_Pattern_Length_0	1.38	1.37	1.37	1.37
ctest_done_sel_2	1.38	1.37	1.38	1.37
IO_Johnson	1.37	1.36	1.36	1.36
A_Johnson	1.36	1.35	1.36	1.35

Table 7a Pre-Irradiation and Post-Annealing Input Thresholds (V_{IH})

	4876		4899		4909	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.64	1.63	1.65	1.64	1.65	1.64
Shiftin7	1.63	1.62	1.64	1.62	1.64	1.63
Shiftin5	1.64	1.63	1.64	1.63	1.65	1.63
Shiftin4	1.65	1.64	1.65	1.64	1.65	1.64
Shiftin3	1.65	1.64	1.66	1.65	1.66	1.65
Shiftin2	1.63	1.62	1.64	1.63	1.64	1.63
Shiftin1	1.65	1.64	1.65	1.64	1.65	1.65
SEU_sel	1.63	1.62	1.64	1.62	1.64	1.63
zoom_sel_n_0	1.65	1.64	1.65	1.64	1.65	1.64
zoom_sel_n_1	1.65	1.64	1.65	1.64	1.66	1.65
zoom	1.65	1.64	1.65	1.64	1.65	1.64
TOG_n	1.64	1.63	1.64	1.63	1.65	1.64

	4918		4930	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.66	1.65	1.65	1.64
Shiftin7	1.64	1.63	1.64	1.63
Shiftin5	1.65	1.64	1.64	1.63
Shiftin4	1.65	1.65	1.65	1.64
Shiftin3	1.66	1.66	1.66	1.65
Shiftin2	1.65	1.64	1.64	1.63
Shiftin1	1.66	1.65	1.65	1.65
SEU_sel	1.64	1.63	1.64	1.63
zoom_sel_n_0	1.65	1.64	1.65	1.64
zoom_sel_n_1	1.65	1.64	1.65	1.64
zoom	1.65	1.64	1.64	1.64
TOG_n	1.65	1.63	1.64	1.63

Table 7b Pre-Irradiation and Post-Annealing Input Thresholds (V_{IH})

	4876		4899		4909	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.64	1.62	1.64	1.63	1.65	1.63
Resetn	1.65	1.64	1.66	1.64	1.66	1.65
oe_EAQ	1.65	1.64	1.65	1.64	1.65	1.64
enable_HSB	1.63	1.62	1.63	1.62	1.64	1.62
IO_Pattern_Length_1	1.66	1.65	1.66	1.65	1.66	1.65
IO_Pattern_Length_2	1.63	1.62	1.64	1.62	1.64	1.63
A_Pattern_Length_0	1.63	1.62	1.63	1.62	1.64	1.62
A_Pattern_Length_1	1.65	1.64	1.65	1.64	1.66	1.65
IO_Pattern_Length_0	1.64	1.63	1.65	1.64	1.65	1.64
ctest_done_sel_2	1.65	1.64	1.65	1.65	1.66	1.65
IO_Johnson	1.65	1.64	1.65	1.64	1.65	1.64
A_Johnson	1.64	1.63	1.65	1.63	1.64	1.63

	4918		4930	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.64	1.63	1.64	1.62
Resetn	1.65	1.64	1.66	1.65
oe_EAQ	1.66	1.65	1.66	1.65
enable_HSB	1.64	1.63	1.64	1.62
IO_Pattern_Length_1	1.66	1.65	1.65	1.64
IO_Pattern_Length_2	1.64	1.63	1.63	1.62
A_Pattern_Length_0	1.64	1.62	1.63	1.62
A_Pattern_Length_1	1.65	1.64	1.65	1.64
IO_Pattern_Length_0	1.65	1.64	1.64	1.64
ctest_done_sel_2	1.66	1.65	1.66	1.65

IO_Johnson	1.65	1.64	1.65	1.64
A_Johnson	1.64	1.63	1.64	1.63

D. Output-Drive Voltage (V_{OL}/V_{OH})

The output drive voltage V_{OL}/V_{OH} is measured at an output pin when it is at Low/High state and sinking/sourcing 1, 12, 20, 50, or 100 mA. In each case, the post-annealing value is within the spec limit, and it is within ±10% of pre-irradiation data.

Table 8a Pre-Irradiation and Post-Annealing V_{OL} for DUT 4876 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.010	0.009	0.096	0.093	0.160	0.154	0.404	0.390	0.861	0.829
Shiftout7	0.013	0.012	0.103	0.097	0.170	0.160	0.425	0.401	0.905	0.851
RAM_out_EAQ_1	0.011	0.010	0.101	0.096	0.167	0.159	0.422	0.402	0.897	0.854
Shiftout3	0.013	0.012	0.099	0.094	0.163	0.154	0.409	0.386	0.871	0.822
RAM_Monitor_EAQ	0.010	0.009	0.093	0.092	0.155	0.153	0.391	0.386	0.836	0.823
Shiftout8	0.012	0.012	0.102	0.102	0.168	0.163	0.422	0.404	0.899	0.878
PADN_LVPECL_1	0.010	0.010	0.098	0.100	0.163	0.166	0.413	0.421	0.880	0.896
PADN_LVPECL_0	0.010	0.010	0.101	0.102	0.169	0.169	0.427	0.428	0.906	0.909
PADP_LVPECL_0	0.011	0.011	0.102	0.100	0.167	0.166	0.423	0.417	0.898	0.883
PADP_LVPECL_1	0.010	0.010	0.096	0.095	0.160	0.158	0.405	0.399	0.863	0.848
Global_Monitor_EAQ	0.009	0.009	0.092	0.090	0.153	0.149	0.388	0.379	0.831	0.809
RAM_out_EAQ_0	0.009	0.009	0.100	0.094	0.166	0.157	0.421	0.397	0.895	0.845
Array_out_EAQ_1	0.010	0.010	0.096	0.092	0.159	0.152	0.401	0.377	0.856	0.819

Table 8b Pre-Irradiation and Post-Annealing V_{OL} (V) for DUT 4899 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.010	0.009	0.095	0.091	0.157	0.151	0.397	0.382	0.849	0.814
Shiftout7	0.013	0.012	0.104	0.098	0.171	0.162	0.430	0.405	0.911	0.857
RAM_out_EAQ_1	0.011	0.011	0.102	0.097	0.169	0.161	0.426	0.405	0.905	0.859
Shiftout3	0.013	0.012	0.101	0.095	0.165	0.156	0.413	0.391	0.877	0.828
RAM_Monitor_EAQ	0.009	0.010	0.093	0.092	0.155	0.153	0.393	0.386	0.840	0.823
Shiftout8	0.012	0.012	0.104	0.100	0.172	0.167	0.431	0.422	0.913	0.891
PADN_LVPECL_1	0.010	0.010	0.098	0.099	0.162	0.164	0.410	0.416	0.874	0.887
PADN_LVPECL_0	0.010	0.010	0.101	0.101	0.168	0.168	0.425	0.424	0.903	0.903
PADP_LVPECL_0	0.011	0.011	0.101	0.100	0.167	0.165	0.423	0.415	0.898	0.879
PADP_LVPECL_1	0.010	0.010	0.096	0.095	0.161	0.158	0.406	0.398	0.866	0.847
Global_Monitor_EAQ	0.008	0.008	0.092	0.090	0.153	0.149	0.390	0.379	0.835	0.809
RAM_out_EAQ_0	0.009	0.009	0.100	0.096	0.167	0.159	0.424	0.402	0.902	0.854
Array_out_EAQ_1	0.011	0.010	0.096	0.092	0.160	0.153	0.403	0.395	0.860	0.820

Table 8c Pre-Irradiation and Post-Annealing V_{OL} (V) for DUT 4909 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.010	0.009	0.096	0.092	0.159	0.153	0.403	0.387	0.861	0.825
Shiftout7	0.013	0.012	0.103	0.097	0.170	0.159	0.426	0.399	0.905	0.847
RAM_out_EAQ_1	0.010	0.010	0.099	0.095	0.165	0.158	0.417	0.398	0.887	0.844
Shiftout3	0.013	0.012	0.099	0.093	0.163	0.154	0.408	0.384	0.869	0.815
RAM_Monitor_EAQ	0.009	0.009	0.093	0.091	0.155	0.151	0.391	0.382	0.838	0.816
Shiftout8	0.012	0.012	0.103	0.101	0.170	0.167	0.428	0.420	0.908	0.872
PADN_LVPECL_1	0.010	0.010	0.096	0.097	0.159	0.161	0.404	0.409	0.863	0.873
PADN_LVPECL_0	0.010	0.010	0.100	0.100	0.166	0.165	0.421	0.419	0.895	0.892
PADP_LVPECL_0	0.010	0.010	0.100	0.098	0.165	0.162	0.418	0.409	0.890	0.867
PADP_LVPECL_1	0.009	0.010	0.095	0.093	0.158	0.155	0.400	0.391	0.853	0.831
Global_Monitor_EAQ	0.009	0.009	0.092	0.089	0.153	0.149	0.389	0.378	0.835	0.808
RAM_out_EAQ_0	0.009	0.009	0.098	0.093	0.164	0.154	0.416	0.391	0.887	0.833
Array_out_EAQ_1	0.010	0.010	0.096	0.090	0.158	0.150	0.400	0.382	0.855	0.809

Table 8d Pre-Irradiation and Post-Annealing V_{OL} (V) for DUT 4918 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.010	0.009	0.096	0.093	0.160	0.154	0.405	0.389	0.863	0.829
Shiftout7	0.013	0.012	0.104	0.098	0.171	0.161	0.429	0.404	0.912	0.859
RAM_out_EAQ_1	0.010	0.010	0.099	0.095	0.165	0.157	0.417	0.397	0.885	0.843
Shiftout3	0.013	0.012	0.100	0.094	0.164	0.155	0.413	0.389	0.879	0.827
RAM_Monitor_EAQ	0.009	0.009	0.092	0.091	0.153	0.151	0.388	0.382	0.830	0.814
Shiftout8	0.012	0.012	0.103	0.101	0.171	0.169	0.429	0.428	0.911	0.885
PADN_LVPECL_1	0.010	0.010	0.096	0.096	0.159	0.161	0.403	0.408	0.859	0.868
PADN_LVPECL_0	0.010	0.010	0.100	0.099	0.166	0.165	0.421	0.418	0.892	0.888
PADP_LVPECL_0	0.011	0.011	0.100	0.098	0.165	0.162	0.418	0.410	0.886	0.868
PADP_LVPECL_1	0.010	0.009	0.095	0.093	0.157	0.154	0.398	0.390	0.848	0.829
Global_Monitor_EAQ	0.008	0.008	0.091	0.089	0.152	0.148	0.386	0.376	0.826	0.802
RAM_out_EAQ_0	0.009	0.009	0.098	0.093	0.164	0.156	0.417	0.395	0.887	0.839
Array_out_EAQ_1	0.010	0.010	0.095	0.091	0.158	0.150	0.399	0.391	0.851	0.810

Table 8e Pre-Irradiation and Post-Annealing V_{OL} (V) for DUT 4930 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.010	0.009	0.096	0.092	0.159	0.153	0.402	0.387	0.858	0.825
Shiftout7	0.013	0.012	0.103	0.097	0.170	0.160	0.426	0.401	0.904	0.851
RAM_out_EAQ_1	0.010	0.010	0.099	0.095	0.165	0.157	0.415	0.397	0.883	0.843
Shiftout3	0.013	0.012	0.099	0.094	0.163	0.154	0.408	0.385	0.868	0.817
RAM_Monitor_EAQ	0.009	0.009	0.092	0.091	0.153	0.151	0.389	0.382	0.831	0.815
Shiftout8	0.012	0.012	0.103	0.102	0.170	0.166	0.427	0.430	0.907	0.882

PADN_LVPECL_1	0.010	0.009	0.096	0.097	0.159	0.161	0.404	0.408	0.861	0.870
PADN_LVPECL_0	0.010	0.010	0.100	0.099	0.166	0.165	0.419	0.417	0.892	0.887
PADP_LVPECL_0	0.011	0.010	0.100	0.098	0.165	0.162	0.417	0.409	0.885	0.867
PADP_LVPECL_1	0.010	0.010	0.095	0.093	0.158	0.154	0.399	0.391	0.852	0.831
Global_Monitor_EAQ	0.009	0.008	0.091	0.089	0.152	0.148	0.388	0.377	0.831	0.806
RAM_out_EAQ_0	0.009	0.009	0.098	0.093	0.163	0.154	0.413	0.392	0.879	0.833
Array_out_EAQ_1	0.010	0.010	0.096	0.092	0.157	0.155	0.398	0.380	0.848	0.827

Table 9a Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4876 at dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.70	1.67
Shiftout7	2.95	2.95	2.83	2.83	2.75	2.74	2.40	2.40	1.64	1.63
RAM_out_EAQ_1	2.95	2.95	2.84	2.83	2.75	2.75	2.40	2.40	1.66	1.64
Shiftout3	2.95	2.95	2.84	2.83	2.75	2.75	2.41	2.41	1.67	1.66
RAM_Monitor_EAQ	2.95	2.95	2.84	2.84	2.76	2.75	2.43	2.42	1.72	1.69
Shiftout8	2.95	2.95	2.84	2.83	2.75	2.75	2.39	2.38	1.63	1.61
PADN_LVPECL_1	2.95	2.95	2.84	2.83	2.75	2.75	2.41	2.39	1.67	1.63
PADN_LVPECL_0	2.95	2.95	2.83	2.83	2.74	2.74	2.39	2.38	1.63	1.60
PADP_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.74	2.40	2.38	1.64	1.61
PADP_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.40	1.69	1.66
Global_Monitor_EAQ	2.96	2.95	2.85	2.84	2.76	2.76	2.44	2.43	1.73	1.70
RAM_out_EAQ_0	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.40	1.66	1.66
Array_out_EAQ_1	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.70	1.67

Table 9b Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4899 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.95	2.84	2.84	2.76	2.76	2.43	2.42	1.70	1.68
Shiftout7	2.95	2.95	2.83	2.83	2.74	2.74	2.39	2.39	1.64	1.63
RAM_out_EAQ_1	2.95	2.95	2.84	2.83	2.75	2.75	2.40	2.40	1.65	1.64
Shiftout3	2.95	2.95	2.84	2.83	2.75	2.75	2.41	2.41	1.67	1.66
RAM_Monitor_EAQ	2.95	2.95	2.84	2.84	2.76	2.75	2.43	2.42	1.72	1.68
Shiftout8	2.95	2.95	2.83	2.83	2.74	2.74	2.38	2.37	1.61	1.57
PADN_LVPECL_1	2.95	2.95	2.84	2.84	2.75	2.75	2.41	2.40	1.68	1.64
PADN_LVPECL_0	2.95	2.95	2.83	2.83	2.75	2.74	2.39	2.38	1.63	1.61
PADP_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.74	2.40	2.38	1.64	1.61
PADP_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.69	1.66
Global_Monitor_EAQ	2.96	2.95	2.85	2.84	2.76	2.76	2.44	2.42	1.72	1.69
RAM_out_EAQ_0	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.40	1.65	1.65
Array_out_EAQ_1	2.96	2.95	2.84	2.84	2.76	2.75	2.42	2.42	1.69	1.67

Table 9c Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4909 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.69	1.67
Shiftout7	2.95	2.95	2.84	2.83	2.75	2.75	2.40	2.40	1.65	1.65
RAM_out_EAQ_1	2.95	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.68	1.67
Shiftout3	2.95	2.95	2.84	2.84	2.75	2.75	2.42	2.42	1.68	1.67
RAM_Monitor_EAQ	2.95	2.95	2.84	2.84	2.76	2.76	2.44	2.42	1.72	1.69
Shiftout8	2.95	2.95	2.83	2.83	2.74	2.73	2.39	2.36	1.62	1.60

PADN_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.40	1.68	1.64
PADN_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.74	2.40	2.39	1.63	1.61
PADP_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.74	2.40	2.39	1.64	1.61
PADP_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.69	1.66
Global_Monitor_EAQ	2.96	2.95	2.85	2.84	2.77	2.76	2.44	2.43	1.73	1.70
RAM_out_EAQ_0	2.96	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.67	1.68
Array_out_EAQ_1	2.96	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.70	1.69

Table 9d Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4918 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.70	1.69
Shiftout7	2.95	2.95	2.83	2.83	2.75	2.75	2.40	2.40	1.65	1.65
RAM_out_EAQ_1	2.95	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.67	1.67
Shiftout3	2.95	2.95	2.84	2.84	2.75	2.75	2.42	2.42	1.68	1.69
RAM_Monitor_EAQ	2.95	2.95	2.85	2.84	2.76	2.76	2.44	2.43	1.74	1.71
Shiftout8	2.95	2.95	2.83	2.83	2.74	2.74	2.39	2.38	1.62	1.55
PADN_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.70	1.67
PADN_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.75	2.40	2.39	1.65	1.63
PADP_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.75	2.40	2.39	1.66	1.64
PADP_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.43	2.42	1.71	1.69
Global_Monitor_EAQ	2.96	2.95	2.85	2.84	2.77	2.76	2.44	2.43	1.74	1.72
RAM_out_EAQ_0	2.96	2.96	2.84	2.84	2.75	2.76	2.41	2.41	1.67	1.68
Array_out_EAQ_1	2.96	2.95	2.84	2.84	2.76	2.76	2.43	2.43	1.71	1.67

Table 9e Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4930 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.69	1.68
Shiftout7	2.95	2.95	2.83	2.83	2.75	2.75	2.40	2.40	1.65	1.66
RAM_out_EAQ_1	2.95	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.67	1.67
Shiftout3	2.95	2.95	2.84	2.84	2.75	2.75	2.41	2.42	1.68	1.68
RAM_Monitor_EAQ	2.95	2.95	2.85	2.84	2.76	2.76	2.44	2.42	1.72	1.70
Shiftout8	2.95	2.95	2.83	2.83	2.74	2.74	2.39	2.38	1.61	1.59
PADN_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.40	1.68	1.65
PADN_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.74	2.39	2.39	1.63	1.61
PADP_LVPECL_0	2.95	2.95	2.84	2.83	2.75	2.75	2.40	2.39	1.64	1.62
PADP_LVPECL_1	2.95	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.69	1.67
Global_Monitor_EAQ	2.96	2.95	2.85	2.84	2.76	2.76	2.44	2.43	1.72	1.70
RAM_out_EAQ_0	2.96	2.96	2.84	2.84	2.75	2.76	2.41	2.42	1.67	1.68
Array_out_EAQ_1	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.69	1.68

E. Propagation Delay

Table 10 lists the pre-irradiation and post-annealing propagation delay and percentage change (degradations) for each DUT. Every DUT passes the ±10%-degradation criterion.

Table 10a Radiation-Induced Propagation Delay Degradations

	Propagation Delay (us)		
	4876	4899	4909

Measurement	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn
Delay0	1.340	1.328	-0.90%	1.357	1.342	-1.11%	1.370	1.353	-1.26%
Delay1	1.351	1.339	-0.87%	1.368	1.353	-1.12%	1.375	1.359	-1.21%
Delay2	1.393	1.381	-0.90%	1.410	1.395	-1.11%	1.421	1.403	-1.25%
Delay3	1.347	1.335	-0.87%	1.362	1.347	-1.10%	1.368	1.351	-1.24%
Delay4	1.363	1.351	-0.90%	1.378	1.363	-1.12%	1.387	1.370	-1.24%
Delay_Chain	5.630	5.560	-1.24%	5.685	5.610	-1.32%	5.700	5.620	-1.40%

	Propagation Delay (us)					
	4918			4930		
Measurement	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn
Delay0	1.347	1.332	-1.11%	1.350	1.334	-1.21%
Delay1	1.356	1.341	-1.11%	1.359	1.343	-1.18%
Delay2	1.398	1.383	-1.12%	1.403	1.386	-1.19%
Delay3	1.348	1.334	-1.10%	1.353	1.337	-1.16%
Delay4	1.367	1.352	-1.11%	1.370	1.354	-1.20%
Delay_Chain	5.640	5.570	-1.24%	5.660	5.585	-1.33%

G. Transition Time

Figures 7 to 16 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

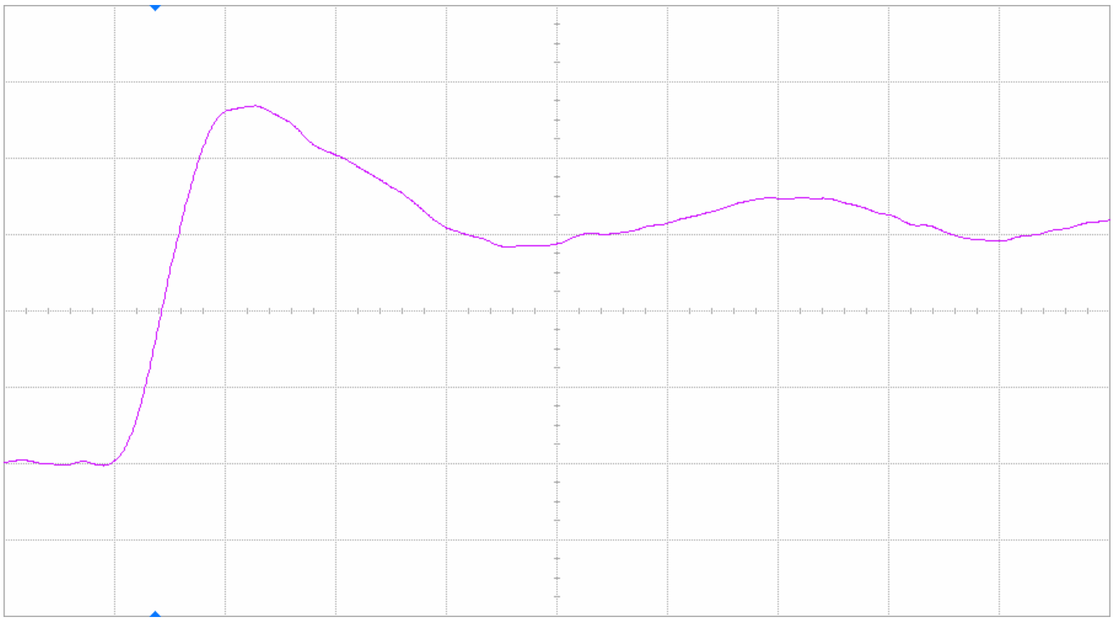

Figure 7(a) DUT 4876 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

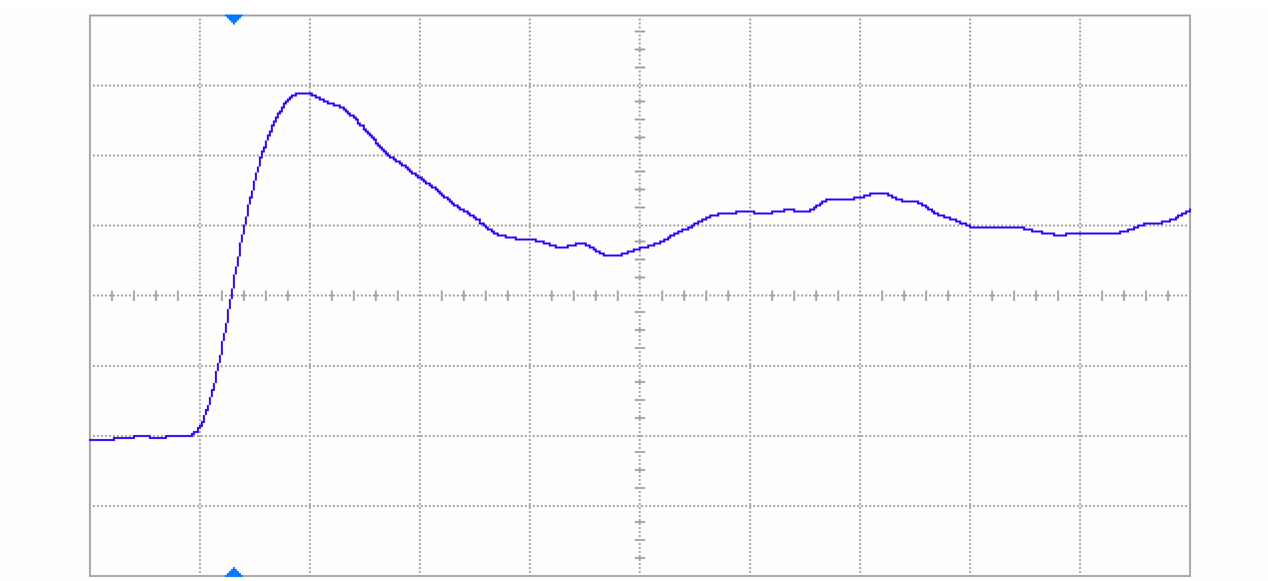

Figure 7(b) DUT 4876 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

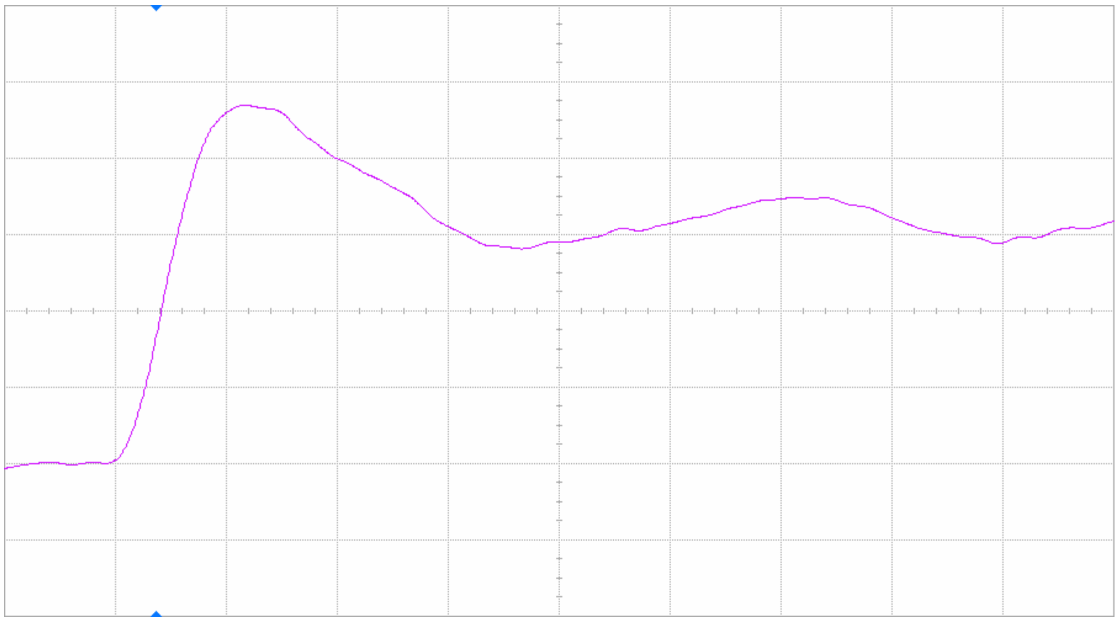

Figure 8(a) DUT 4899 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

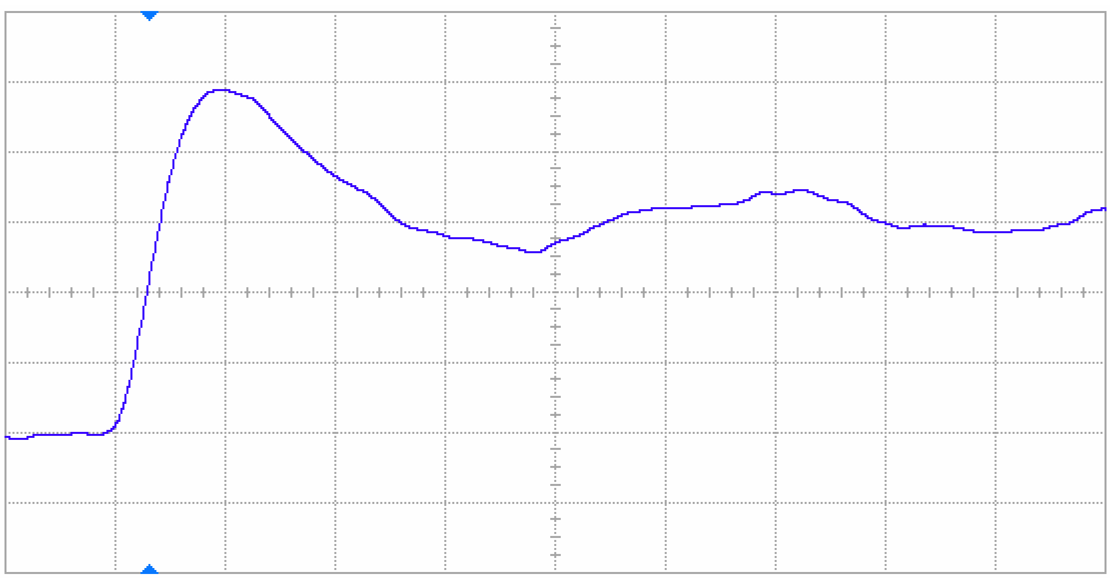

Figure 8(b) DUT 4899 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

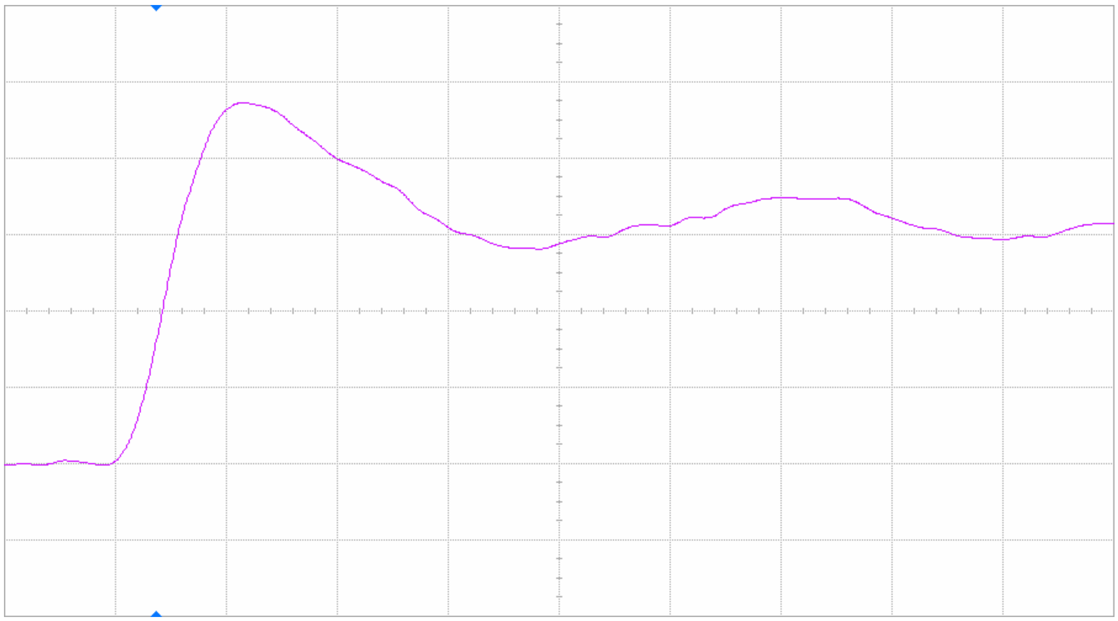

Figure 9(a) DUT 4909 pre-radiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

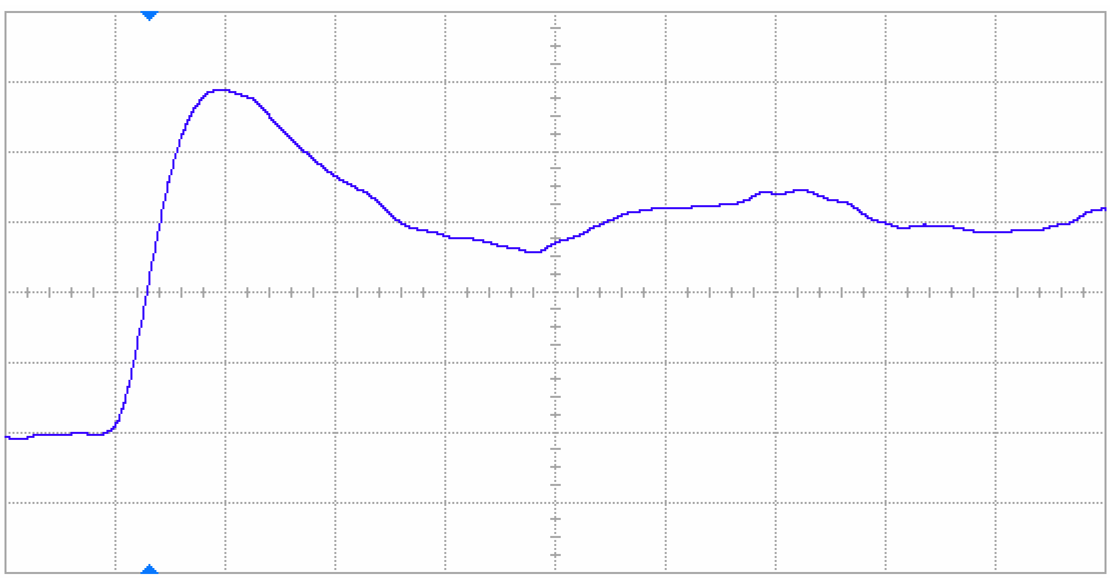

Figure 9(b) DUT 4909 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

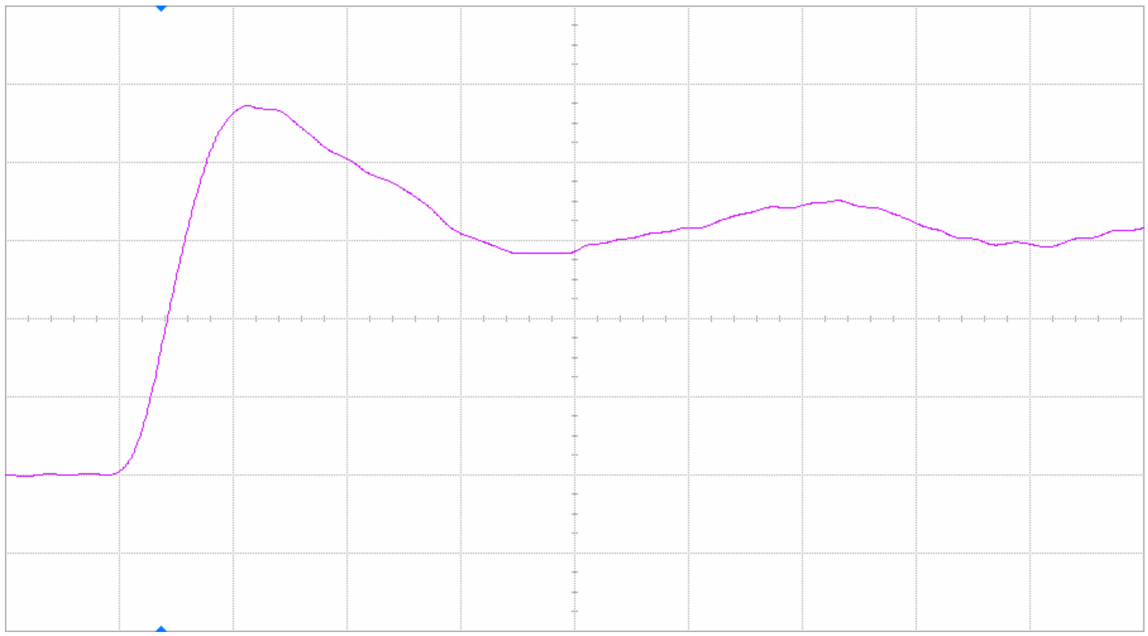

Figure 10(a) DUT 4918 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

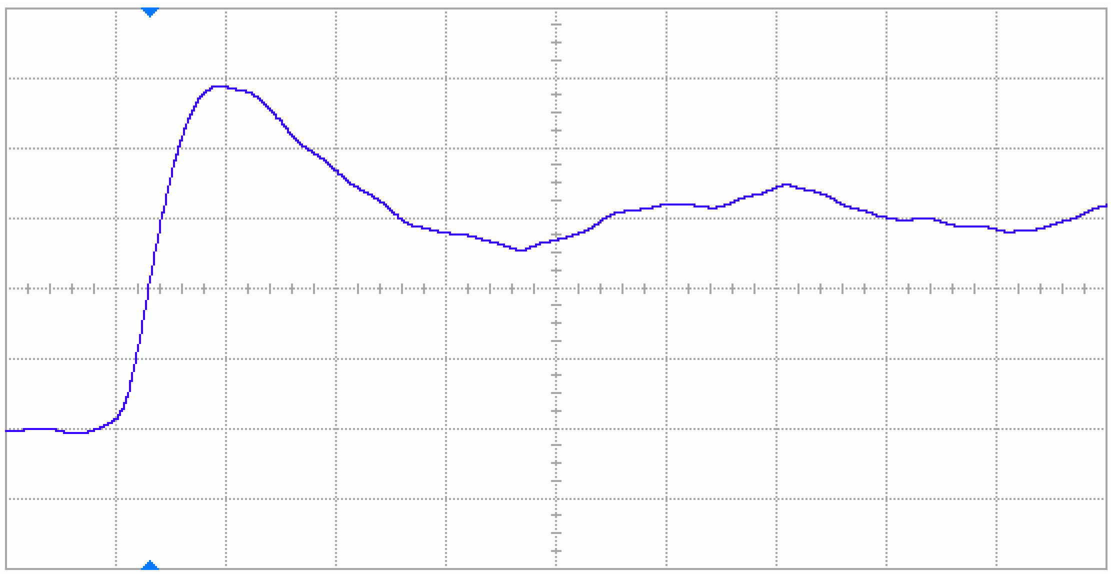

Figure 10(b) DUT 4918 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

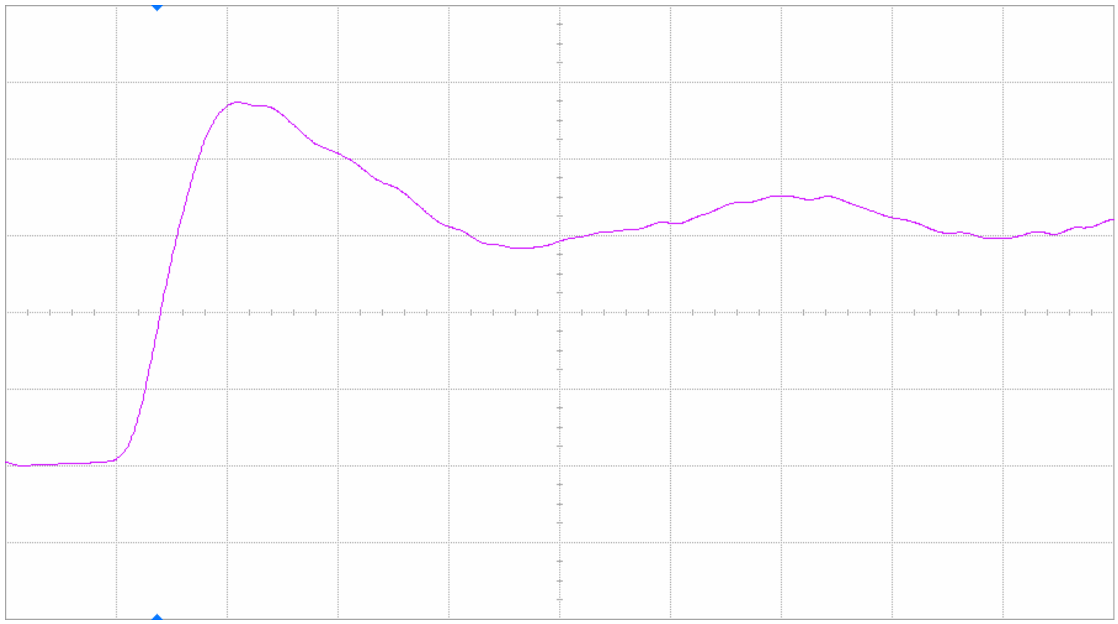

Figure 11(a) DUT 4930 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

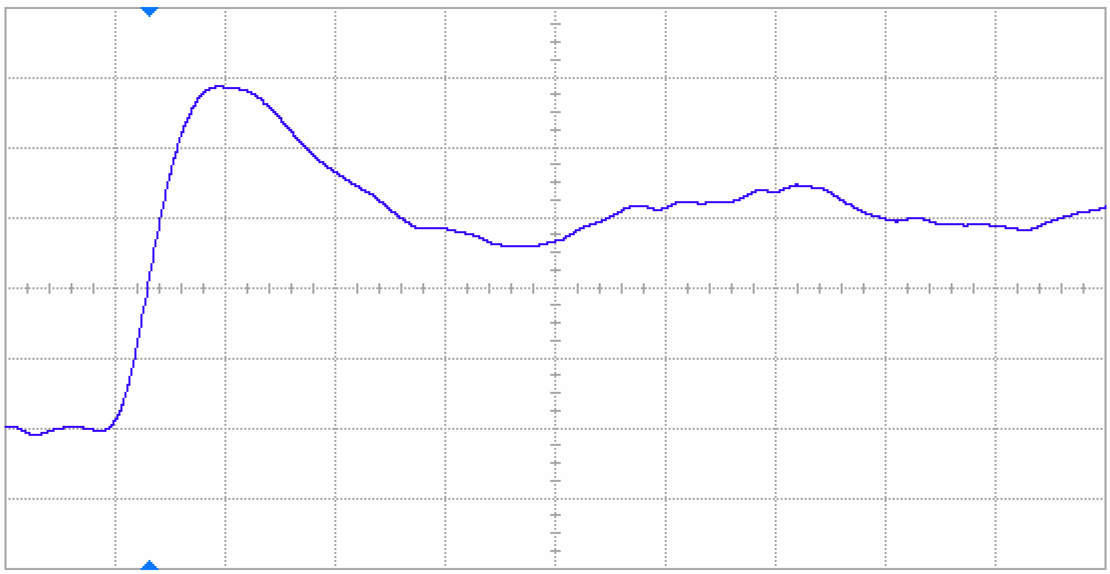

Figure 11(b) DUT 4930 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

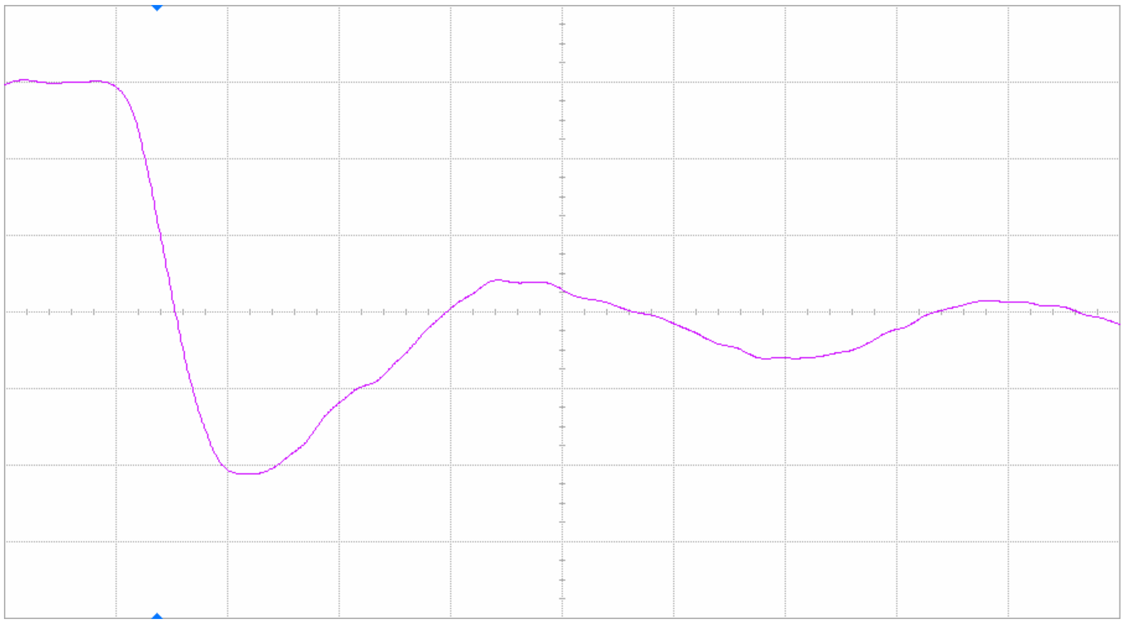

Figure 12(a) DUT 4876 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

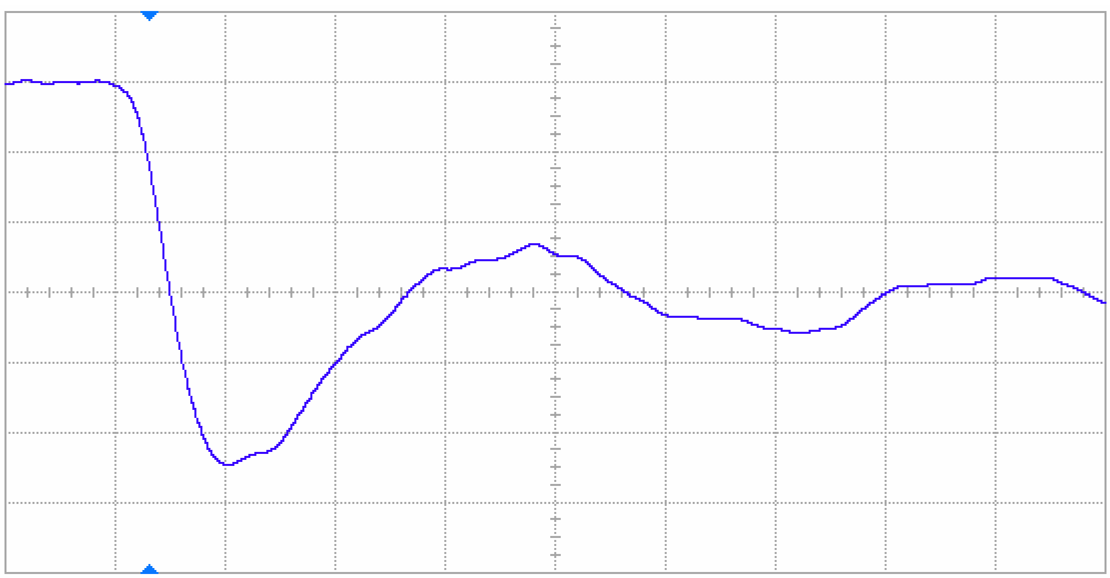

Figure 12(b) DUT 4876 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

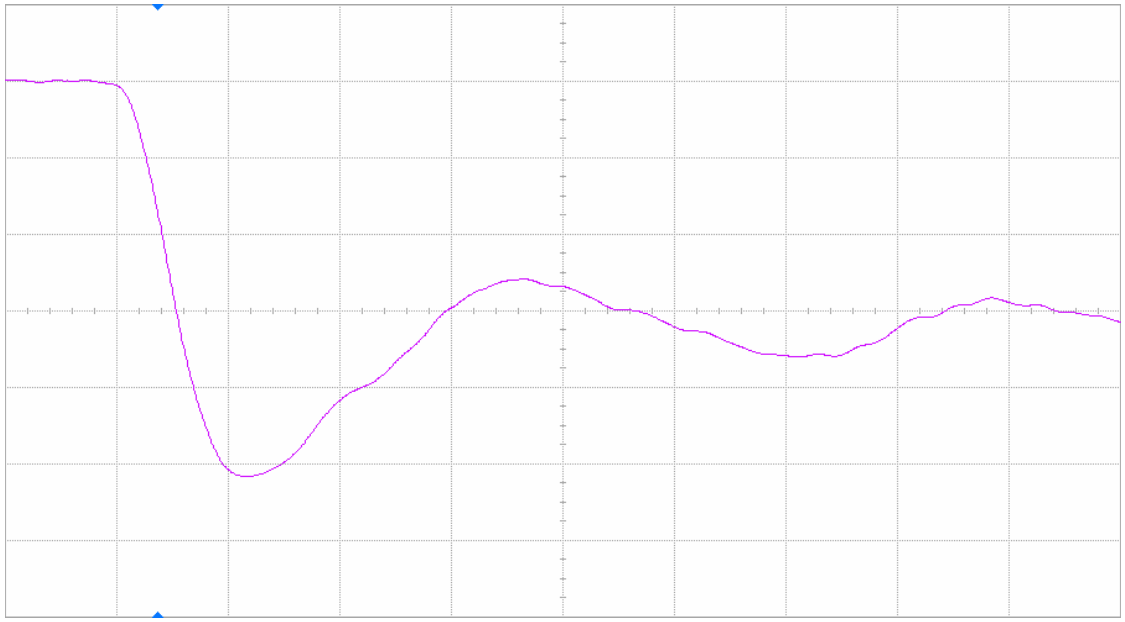

Figure 13(a) DUT 4899 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

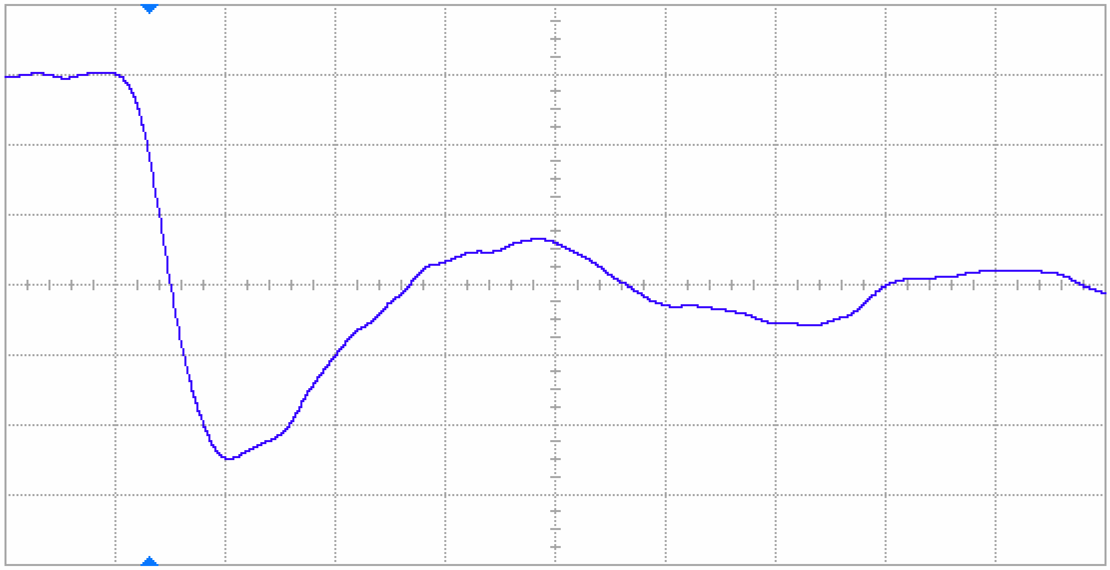

Figure 13(b) DUT 4899 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

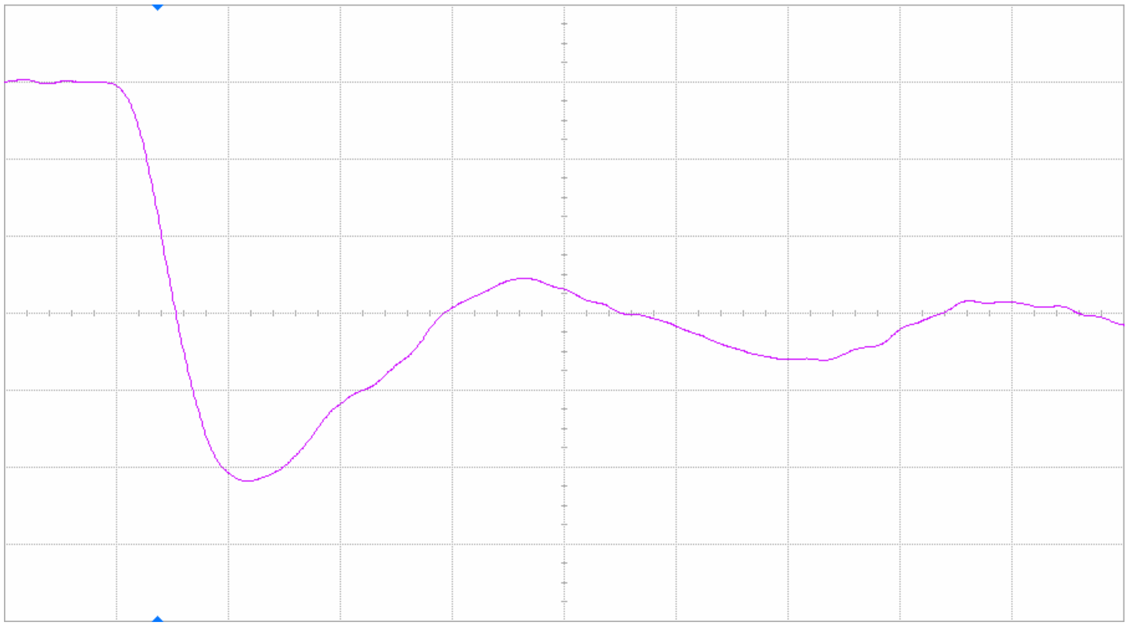

Figure 14(a) DUT 4909 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

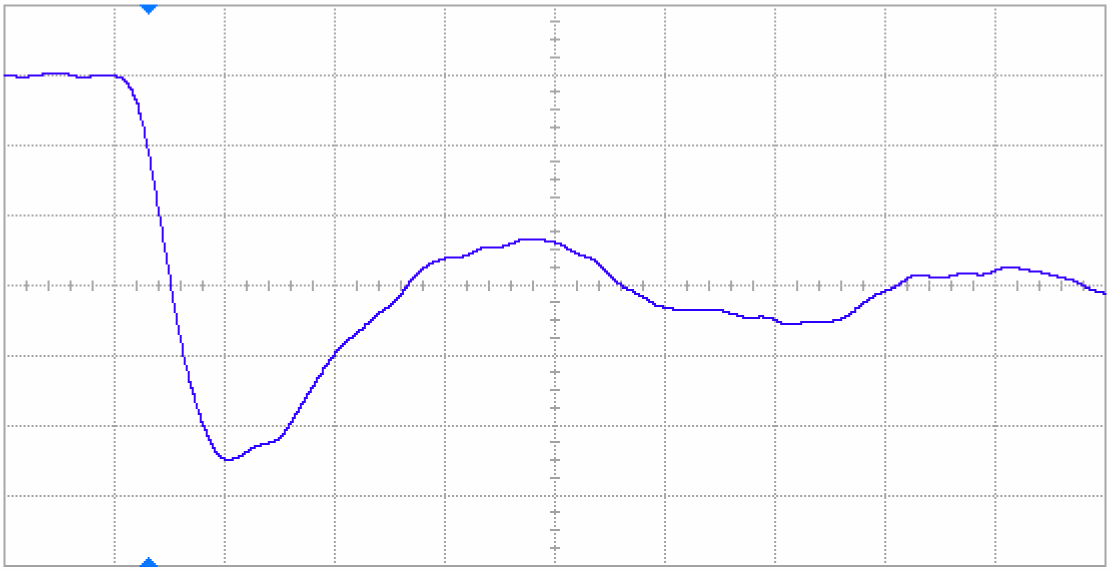

Figure 14(b) DUT 4909 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

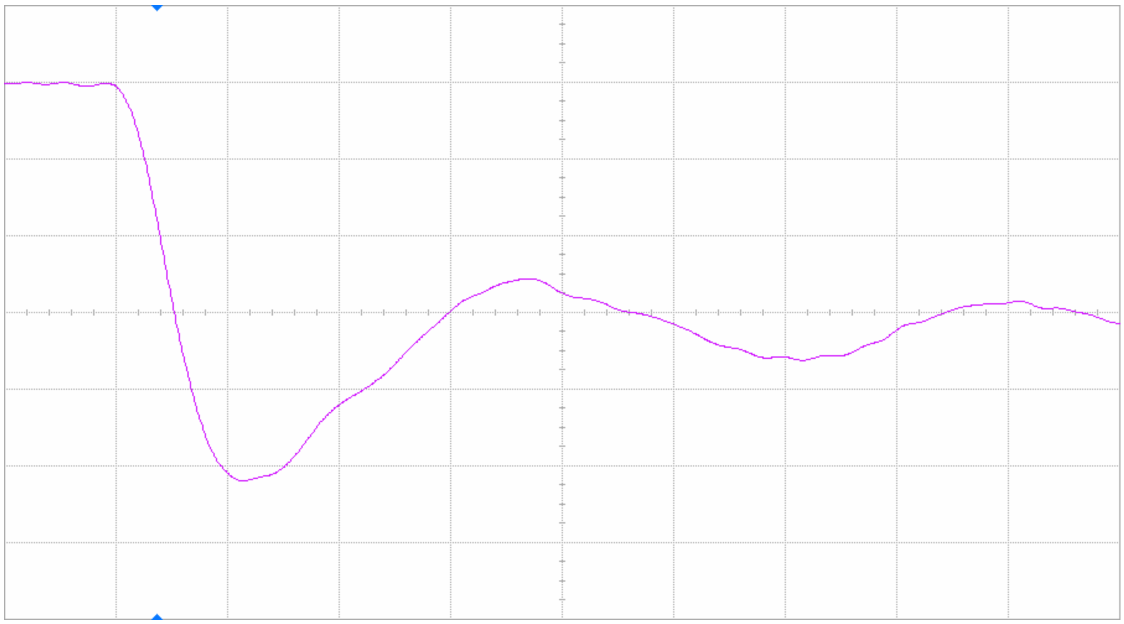

Figure 15(a) DUT 4918 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

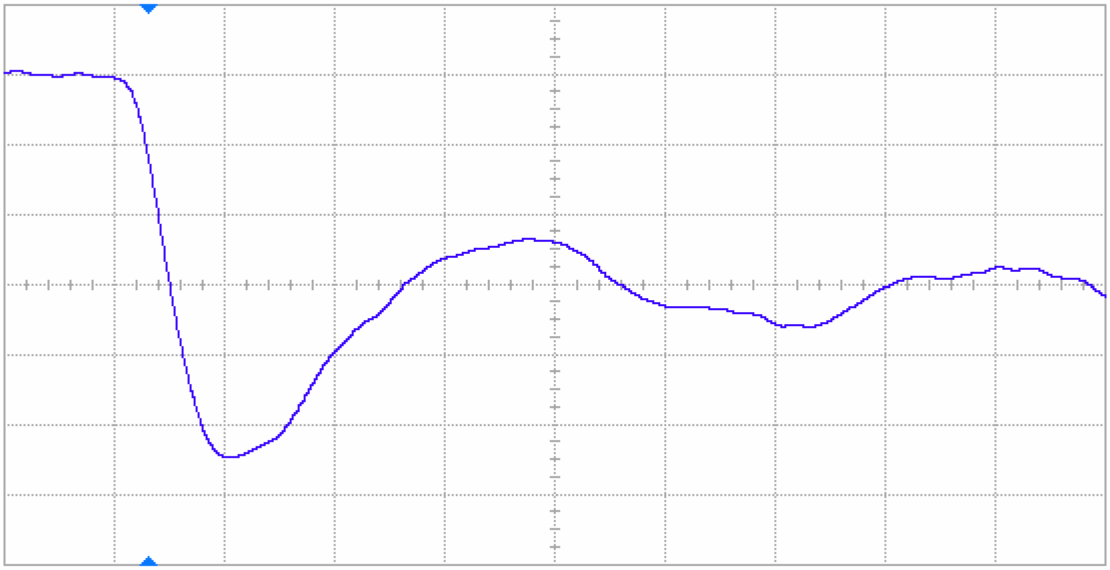

Figure 15(b) DUT 4918 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

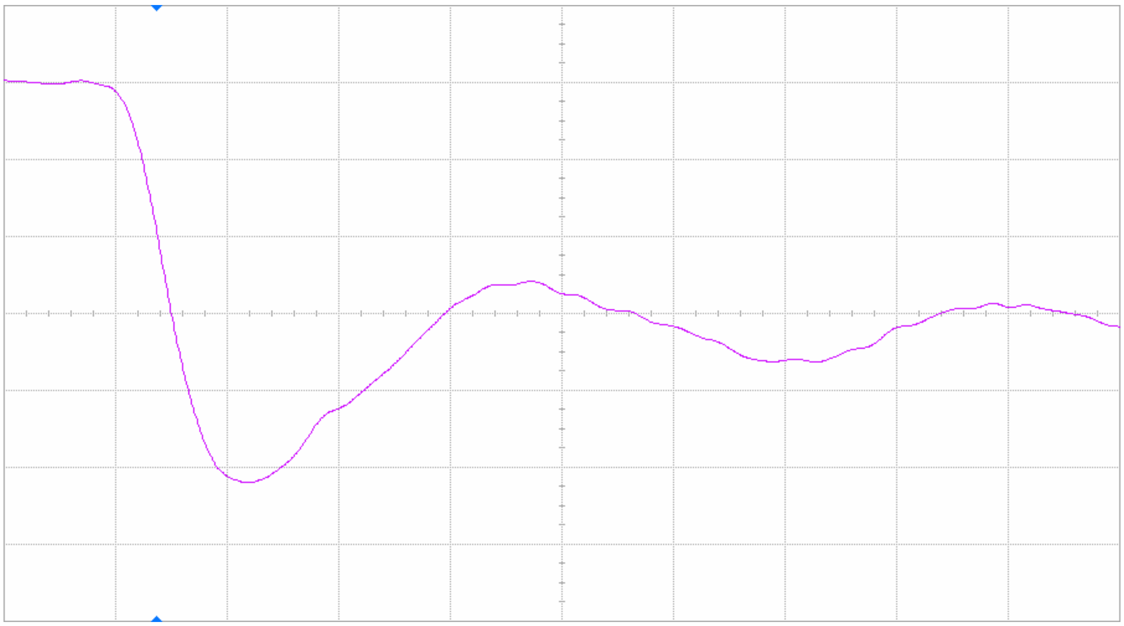

Figure 16(a) DUT 4930 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

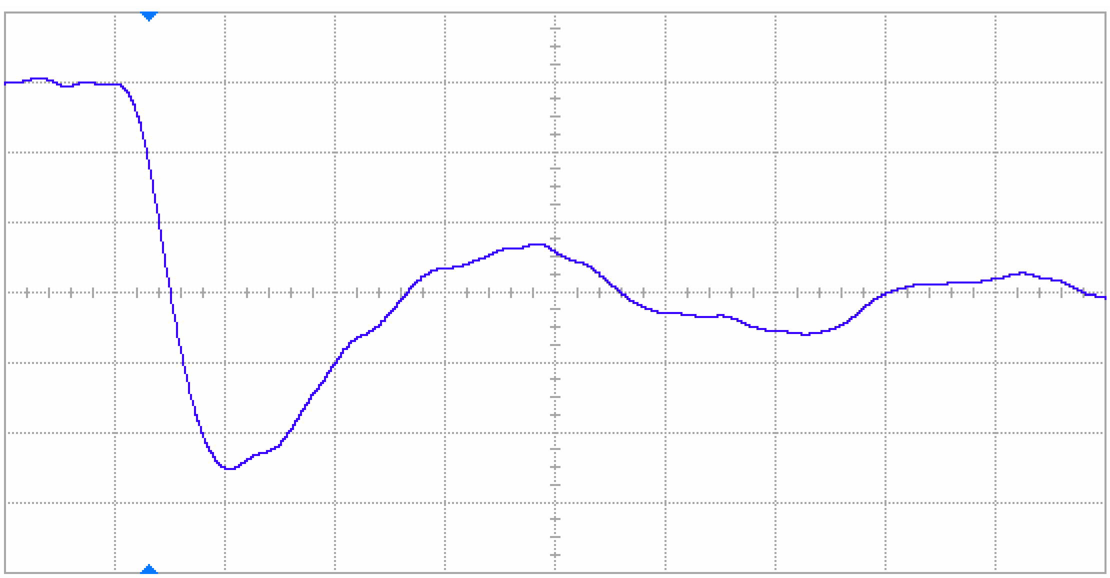

Figure 16(b) DUT 4930 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

APPENDIX A DUT BIAS

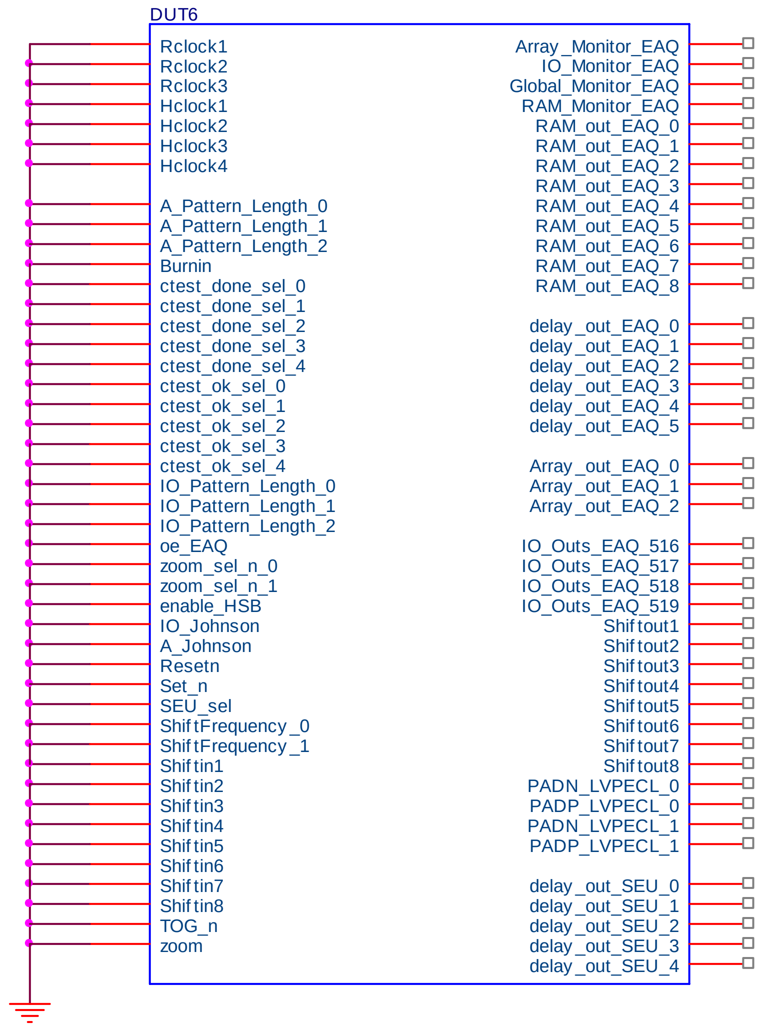

Figure A1 IO bias during irradiation

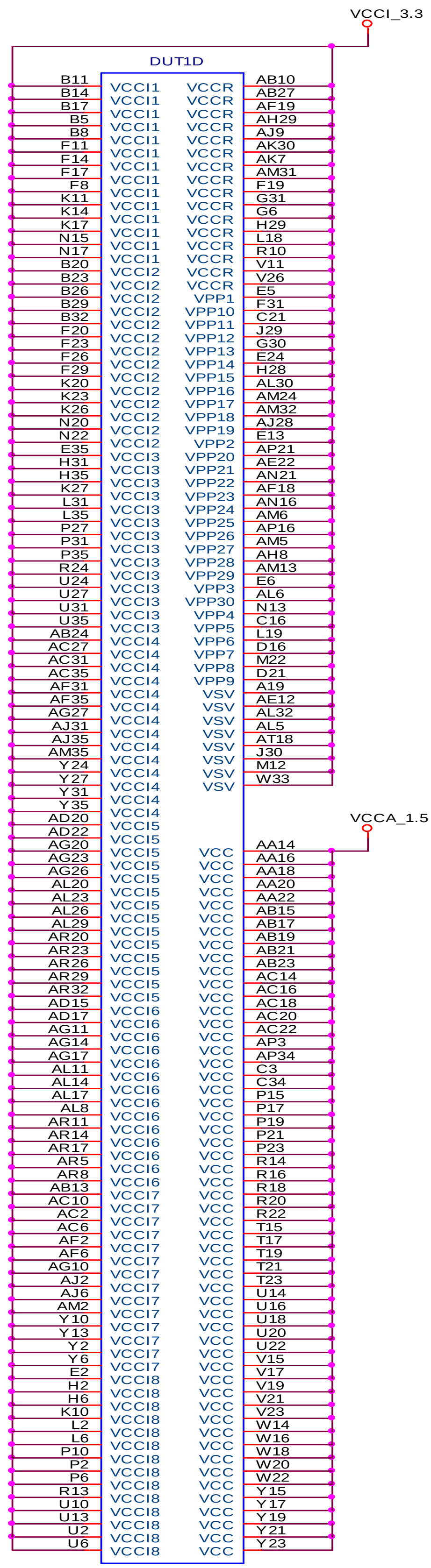

Figure A2 Power supply, ground and special pins bias during irradiation

APPENDIX B FUNCTIONALITY TEST

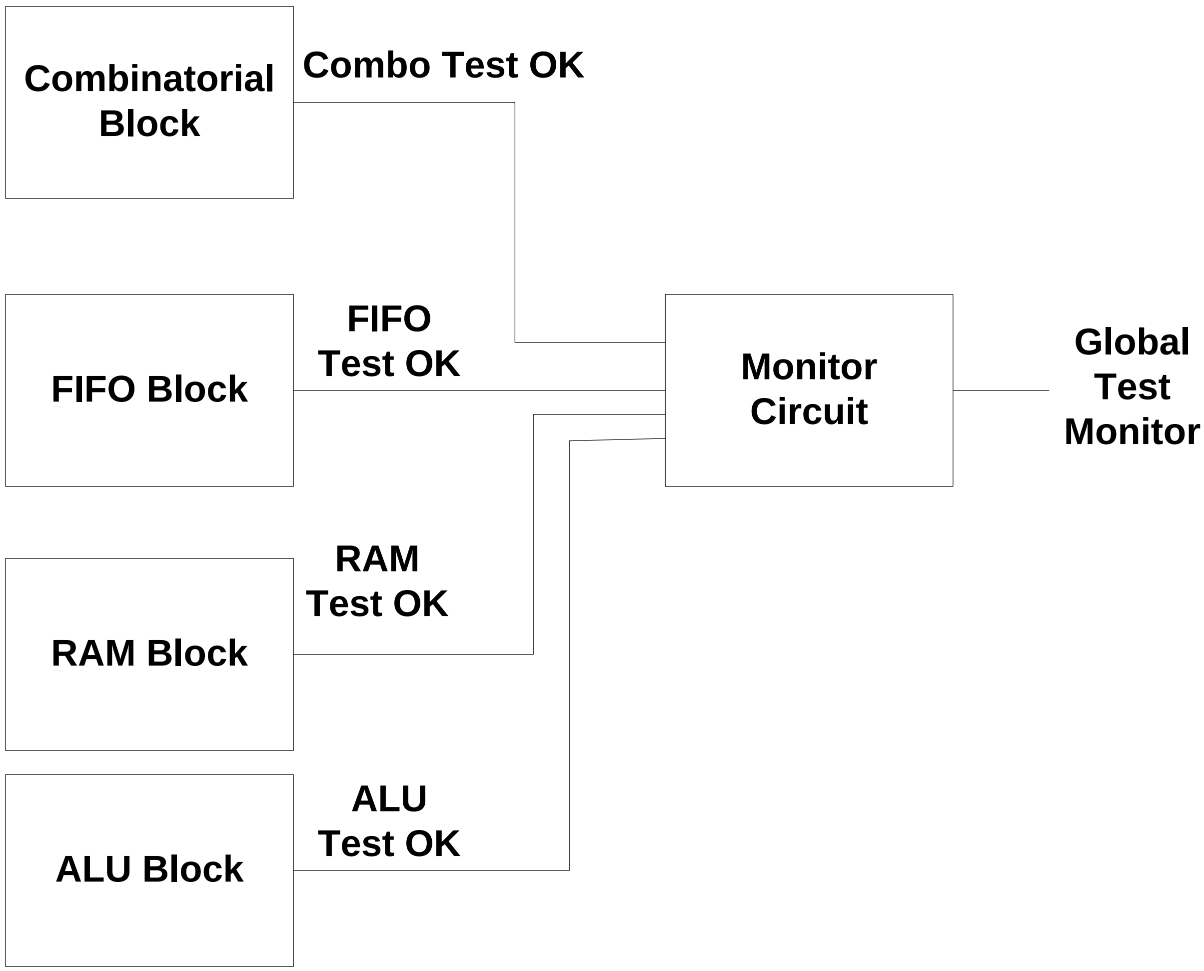

Figure B1 QBI Block – Top level design

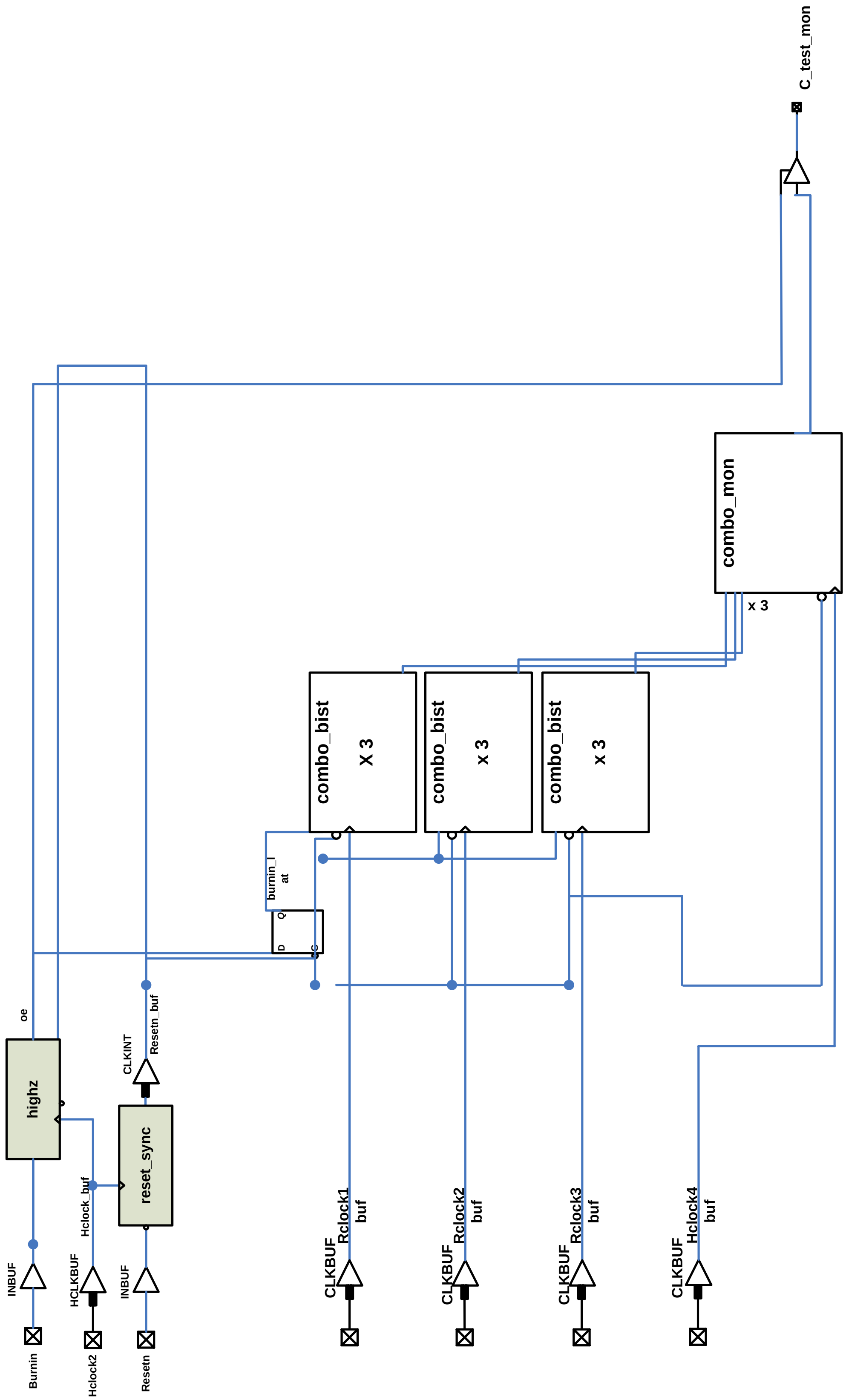

Figure B2 QBI Block – Combinatorial Test (Top Level)

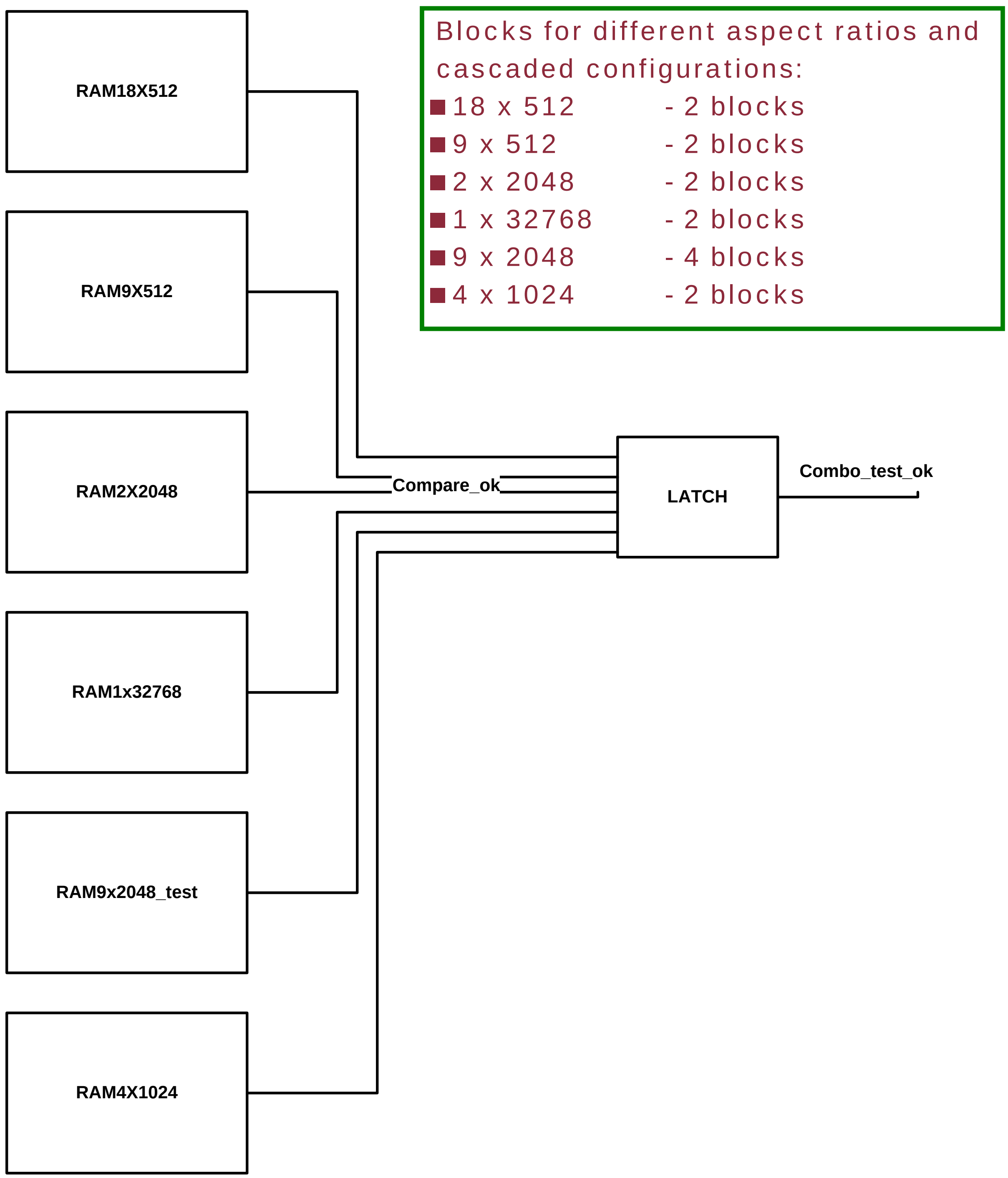

Figure B3 QBI Block – RAM Test (Top Level)

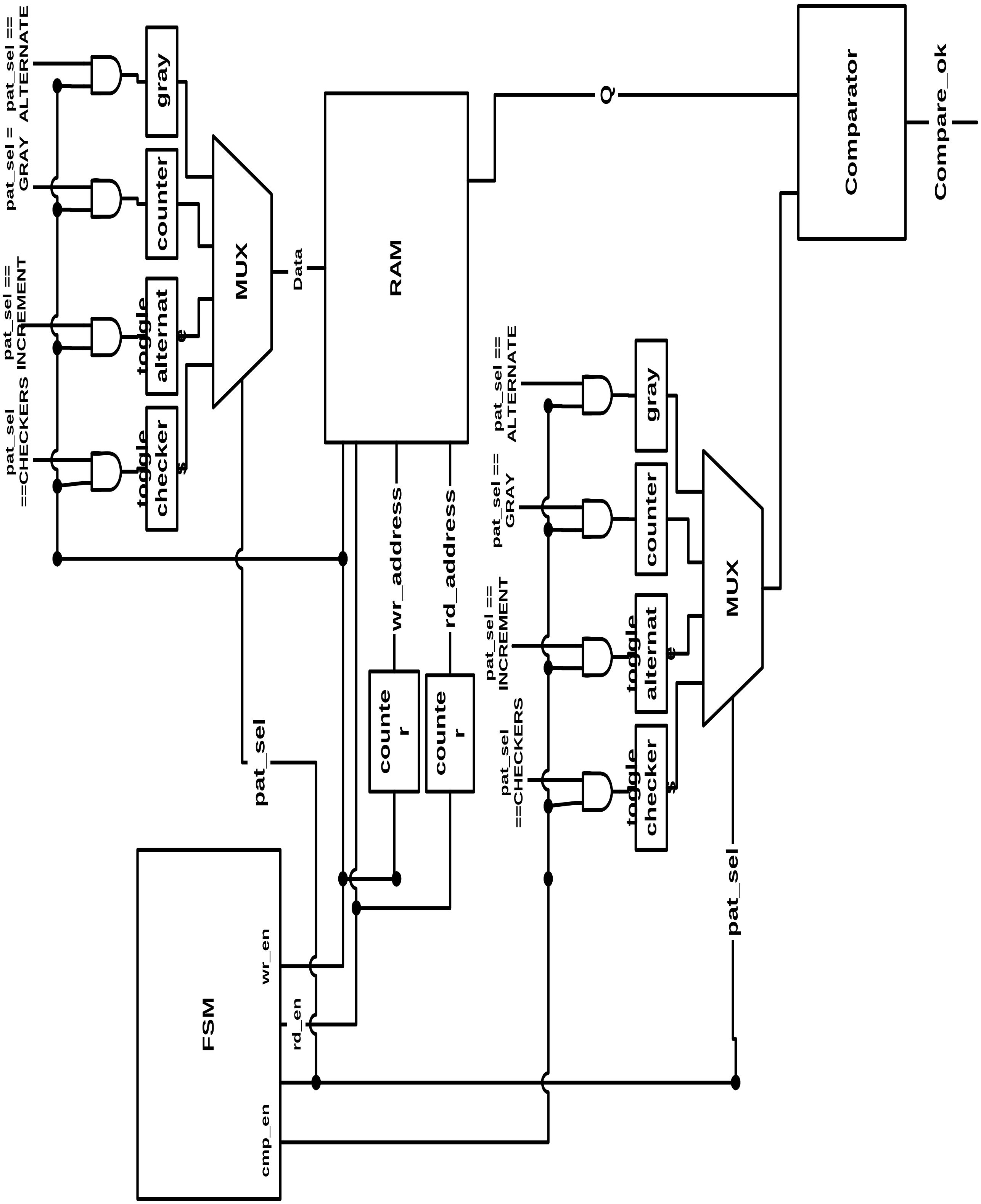

Figure B4   QBI Block – RAM Block

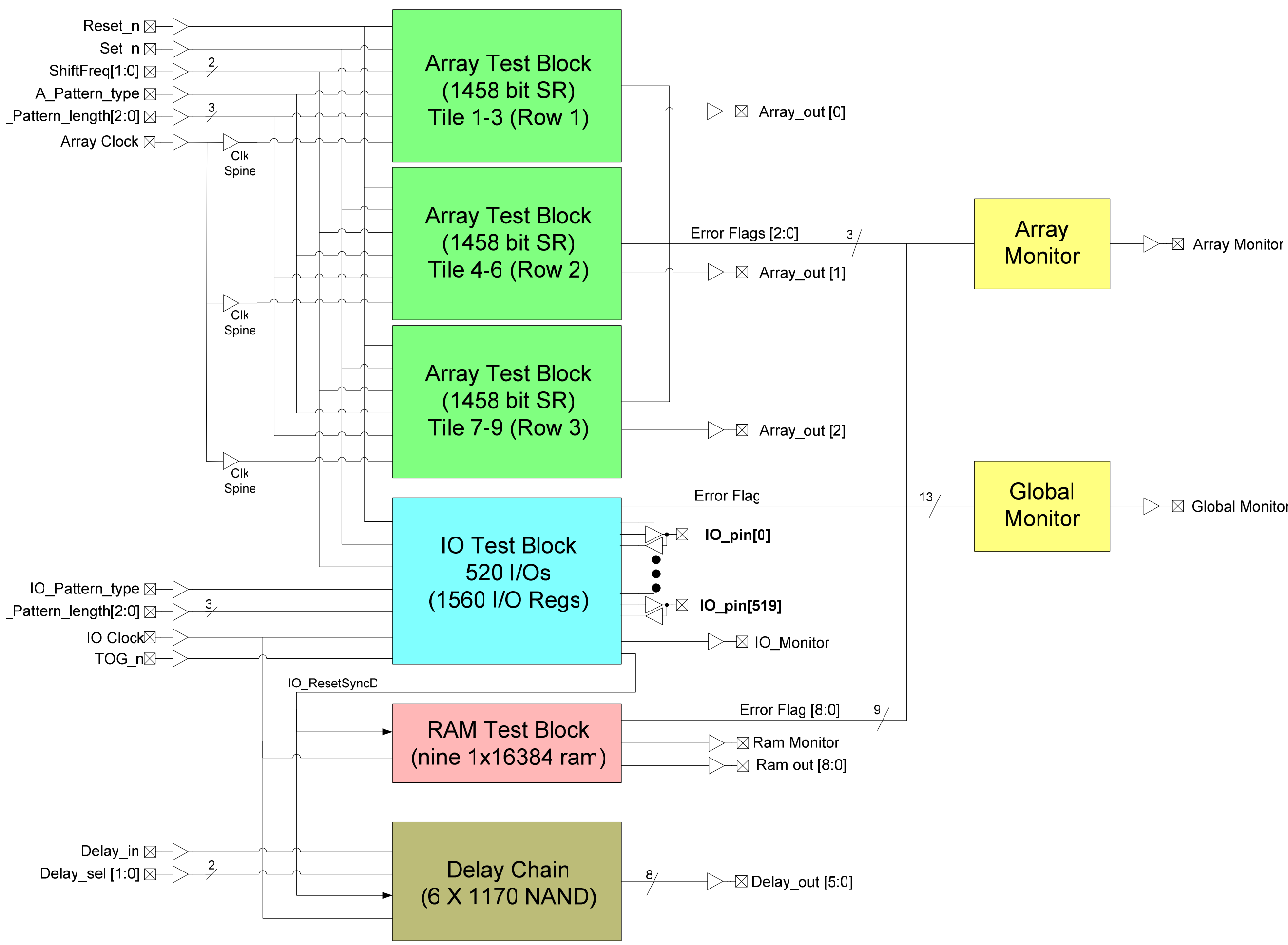

Figure B5 EAQ Block – Top Level

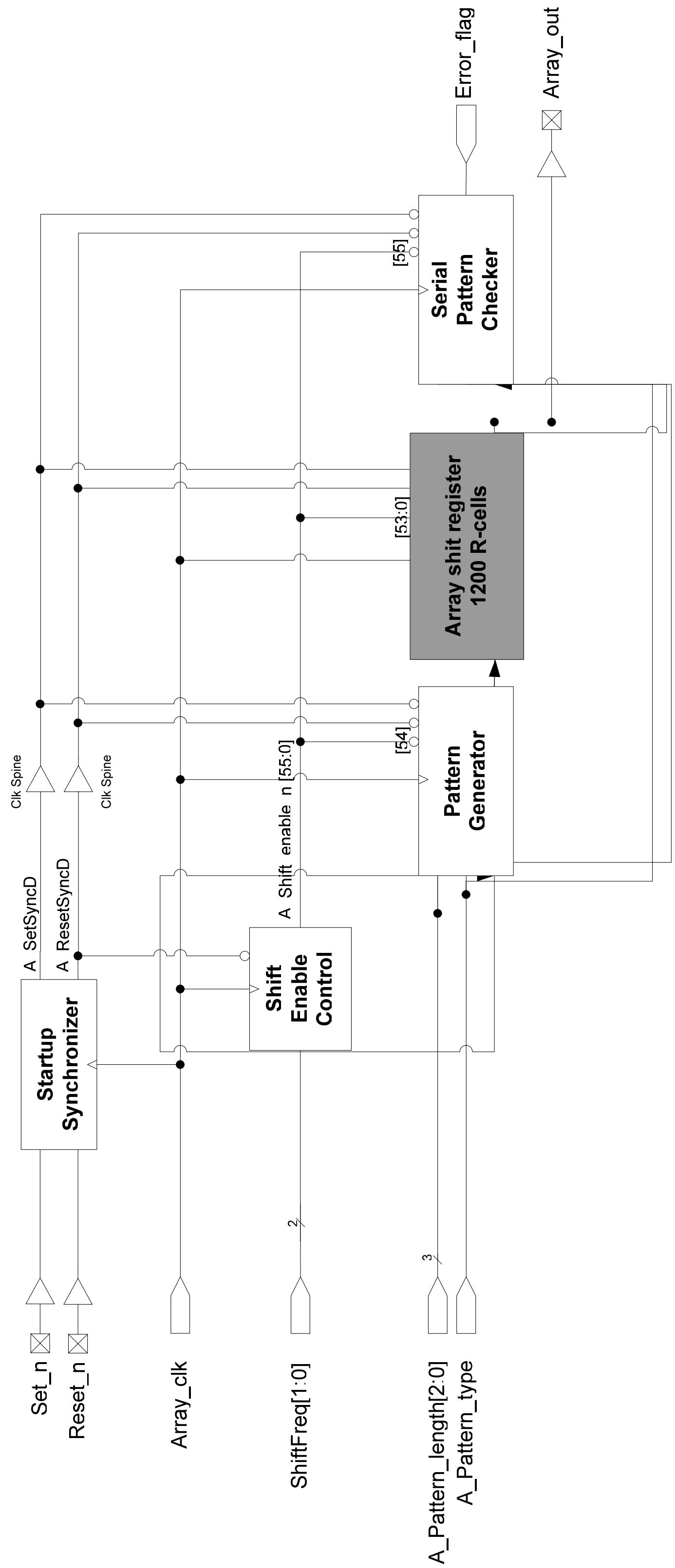

Figure B6 EAQ Block – Array Test (Shift Register)

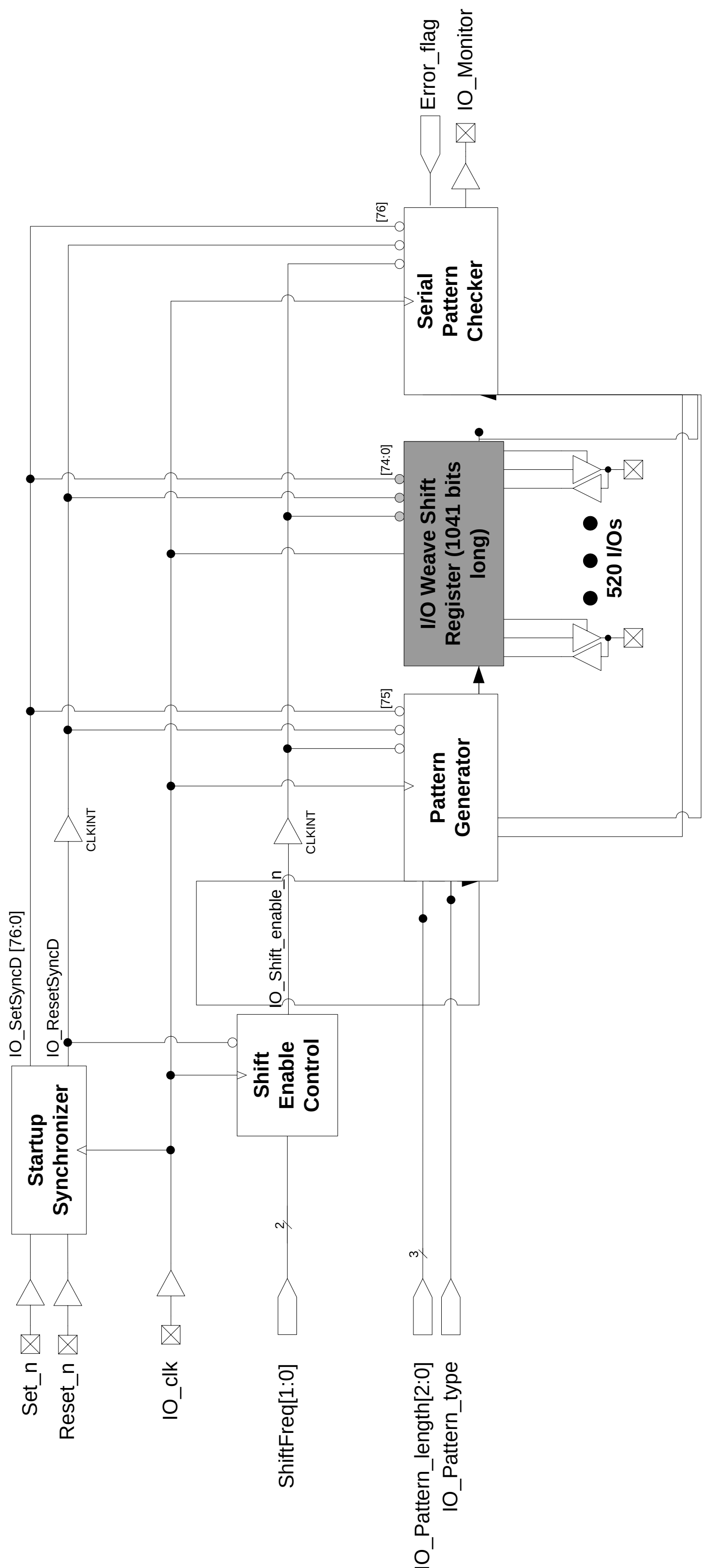

Figure B7 EAQ Block – I/O Test (Top Level)

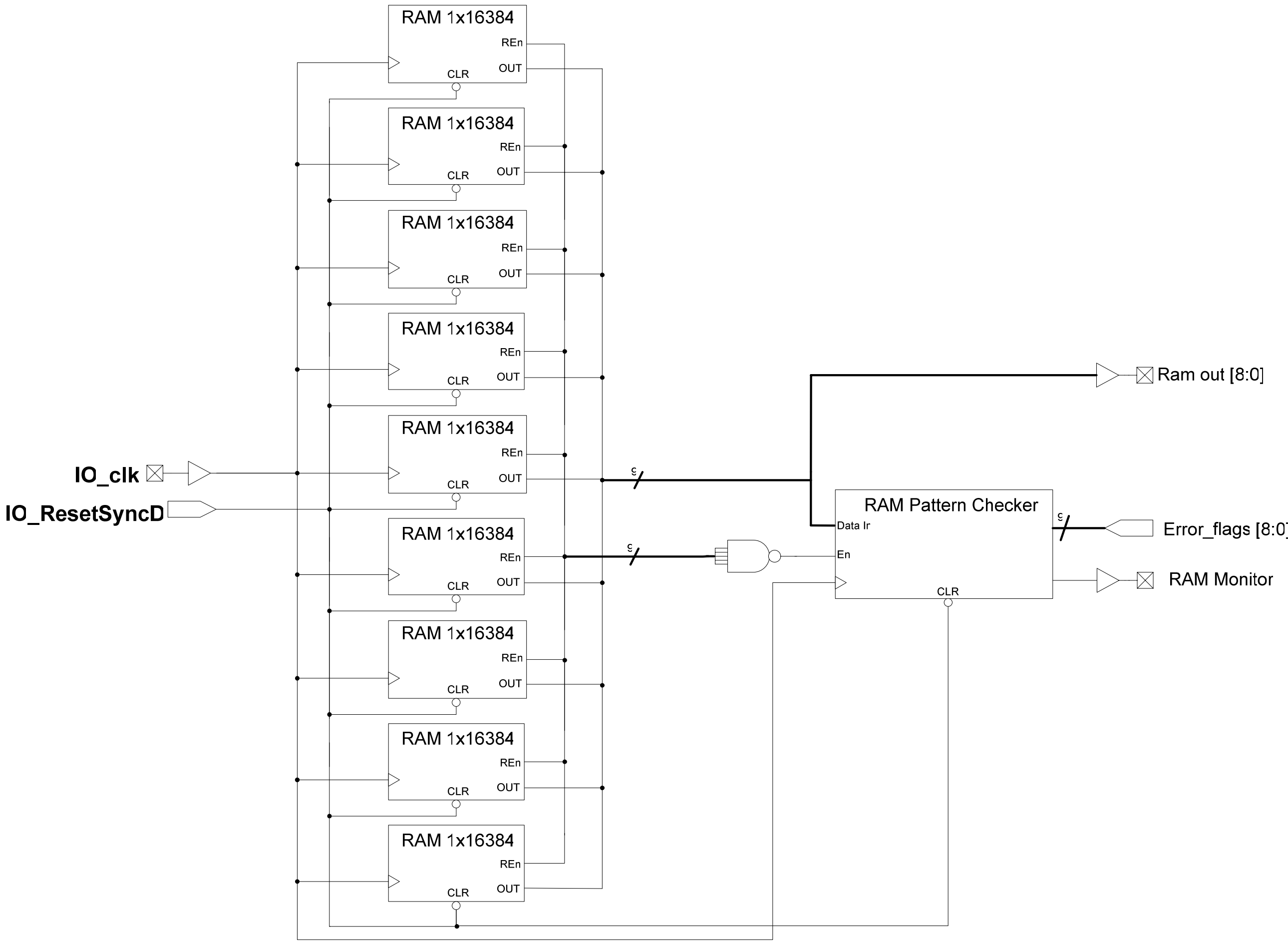

Figure B8 EAQ Block – SRAM Test (Top Level)