TOTAL IONIZING DOSE TEST REPORT

No. 08T-RTAX4000S-CG1272-D30121
February 12, 2009
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I. SUMMARY TABLE

Table 1 summarizes the TID tolerance for each tested parameter. The overall tolerance is limited by the standby power-supply current (I_{CC}). The room temperature annealing allowed by 1019.6 to anneal down I_{CC} is performed for approximately 50 days. Every DUT passes the major specifications listed in the table for 300 krad(SiO_2) of irradiation, except for I_{CCI}, which passes 200 krad(SiO_2).

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO_2)
2. Standby Power Supply Current (I_{CCA}/I_{CCI})	Passed 200 krad(SiO_2)
3. Input Switching Threshold (V_{IHL}/V_{ILH})	Passed 300 krad(SiO_2)
4. Output Threshold (V_{OL}/V_{OH})	Passed 300 krad(SiO_2)
5. Propagation Delay	Passed 300 krad(SiO_2) for ±10% degradation criterion
6. Transition Time	Passed 300 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This section describes the device under test (DUT), irradiation facility and parameters, test method, test design, and electrical parameter measurements. This TID testing, in various slightly modified forms, has been used to build an extensive TID database for many generations of antifuse-based FPGAs. The link to access this TID database is attached in below:

http://www.actel.com/products/milaero/hireldata.aspx#tid

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ and the clocks (Rclock1-4 and Hclock1-4). Inputs Burnin and oe_EAQ are set high to 3.3V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or V_{CCI} through a 4.7kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Device	RTAX4000S
Package	CG1272
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	Master_RTAX4000S_CG1272_Design
Die Lot Number	D30121
Quantity Tested	6
Serial Number	200 krad: 4773, 4787, 4789 300 krad: 4750, 4755, 4766
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL

B. Test Method

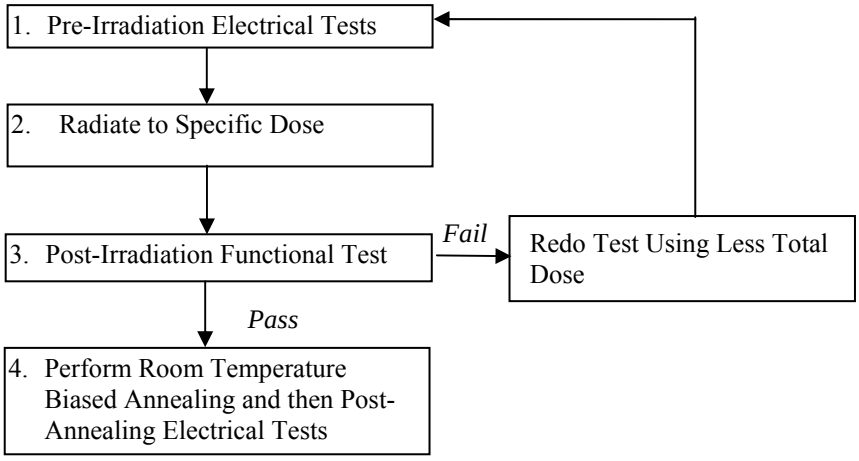

Figure 1 Parametric test flow chart

The test method is based on the military standard TM1019.6. Figure 1 shows the test flow. During irradiation, the DUT is statically biased with V_{CCI}/V_{CCA} = 3.3V/1.5V and all the inputs grounded. The accelerated annealing test in TM1019.6, section 3.12 had been done on samples of the RTAXS family, and the results indicate that post-irradiation annealing recovers the electrical characteristics rather than adversely affecting the electrical performance. This is consistent with the general belief that the dominant TID effects in deep submicron CMOS devices are due to oxide-trapped-hole induced leakage currents. These leakages decrease with the annealing temperature. Consequently, for this lot testing, the accelerated annealing test is omitted.

TM1019.6, Section 3.11 "Extended room temperature anneal test" has been applied for approximately 50 days of annealing. The data measured after this annealing is termed "Post Annealing" in section III, Test Results.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (Master_RTAX4000S_Design) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1MHz and 50MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 – Minimum and Maximum Power Specifications for RTAX-S/SL

SUPPLY VOLTAGE	MINIMUM	RECOMMENDED	MAXIMUM
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V V_{CCDA} I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic threshold (V_{IL}/V_{IH}) is measured on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7,

Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (V_{OL}/V_{OH}) is measured on single-ended outputs Global_Monitor_EAQ, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_1, Array_out_EAQ_1, Array_out_EAQ_2, PADN_LVPECL_1, PADN_LVPECL_0, PADP_LVPECL_1, PADP_LVPECL_0, Shiftout3, Shiftout7, and Shiftout8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{IL}/V_{IH})	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (V_{OL}/V_{OH})	Single-ended outputs (Global_Monitor_EAQ, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_1, Array_out_EAQ_1, Array_out_EAQ_2, PADN_LVPECL_1, PADN_LVPECL_0, PADP_LVPECL_1, PADP_LVPECL_0, Shiftout3, Shiftout7, Shiftout8)
5. Propagation Delay	String of NAND4-inverters. Measured from HClock1 input to delay_out_SEU0, delay_out_SEU1, delay_out_SEU2, delay_out_SEU3, and delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. TEST RESULTS

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Standby Power Supply Current (I_{CCA} and I_{CCI})

The logic-array power supply (V_{CCA}) is 1.5V, and the IO power supply (V_{CCI}) is 3.3V. Their standby currents, I_{CCA} and I_{CCI}, are monitored in-flux. Figure 2-7 show the in-flux I_{CCA} and I_{CCI} versus total dose for the DUTs.

Referring to TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} should be defined as the addition of highest I_{CCI}, I_{CCDA} and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS specifications document posted on the Actel website; the link is

http://www.actel.com/documents/RTAXS_DS.pdf

Therefore, the PIPL for I_{CCA} is 500 mA, and the PIPL for I_{CCI} is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing I_{CCA} and I_{CCI} data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad(SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
4750	300	11	51	12	10	410	84
4755	300	11	54	12	10	416	98
4766	300	10	42	9	10	422	94
4773	200	9	8	10	10	176	34
4787	200	13	12	12	10	163	32
4789	200	9	8	9	10	181	34

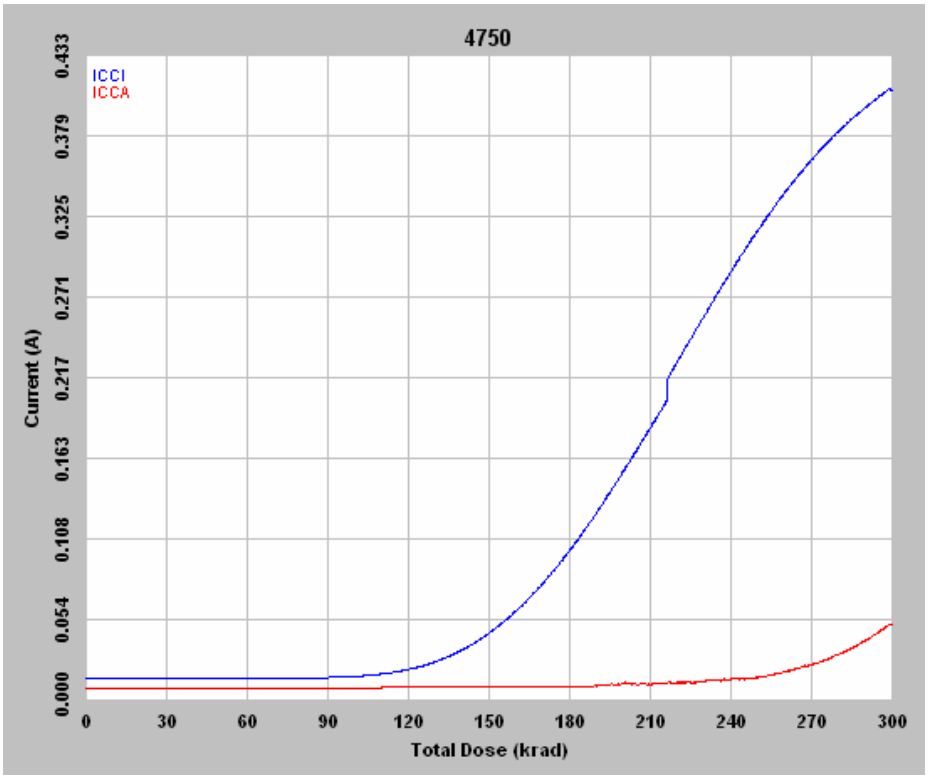

Figure 2 DUT 4750 in-flux I_{CCA} and I_{CCI}

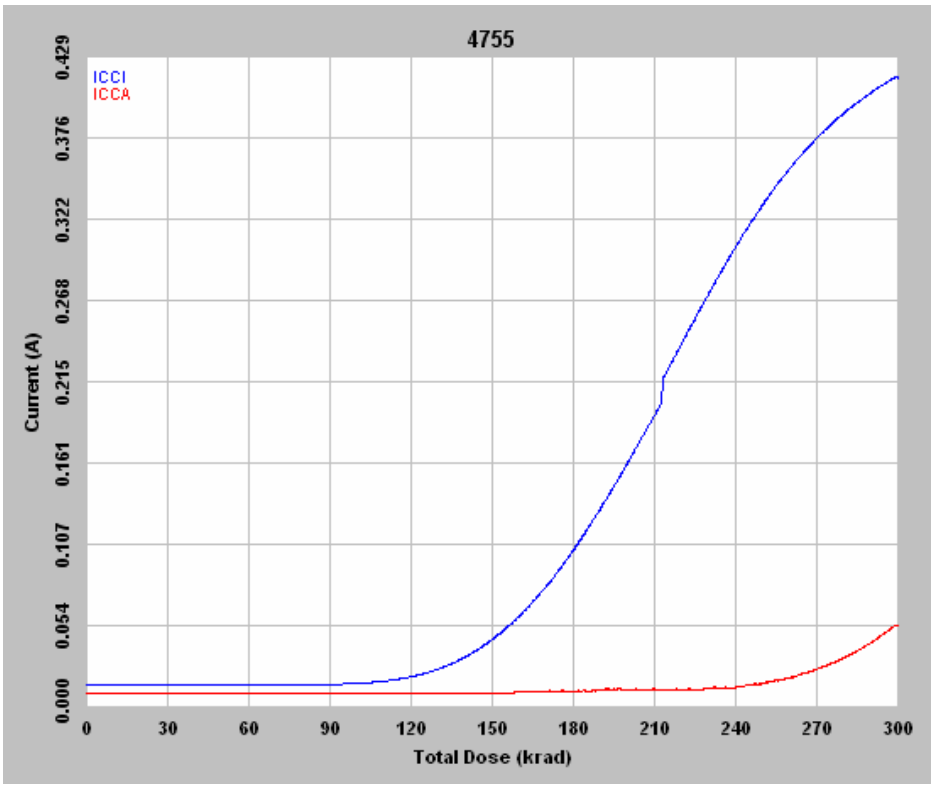

Figure 3 DUT 4755 in-flux I_{CCA} and I_{CCI}

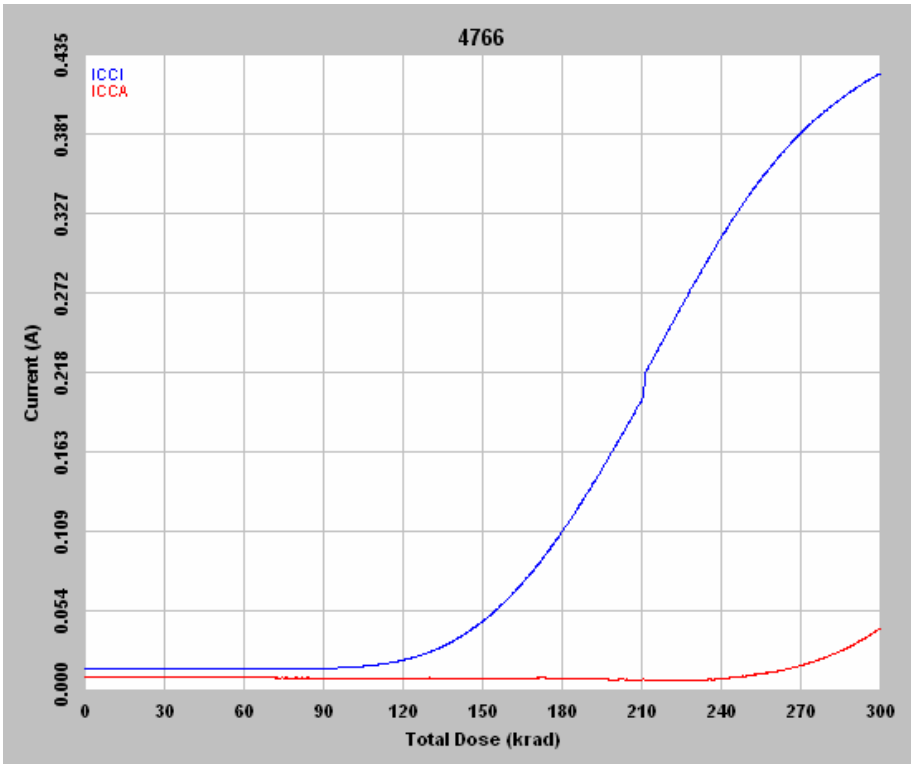

Figure 4 DUT 4766 in-flux I_{CCA} and I_{CCI}

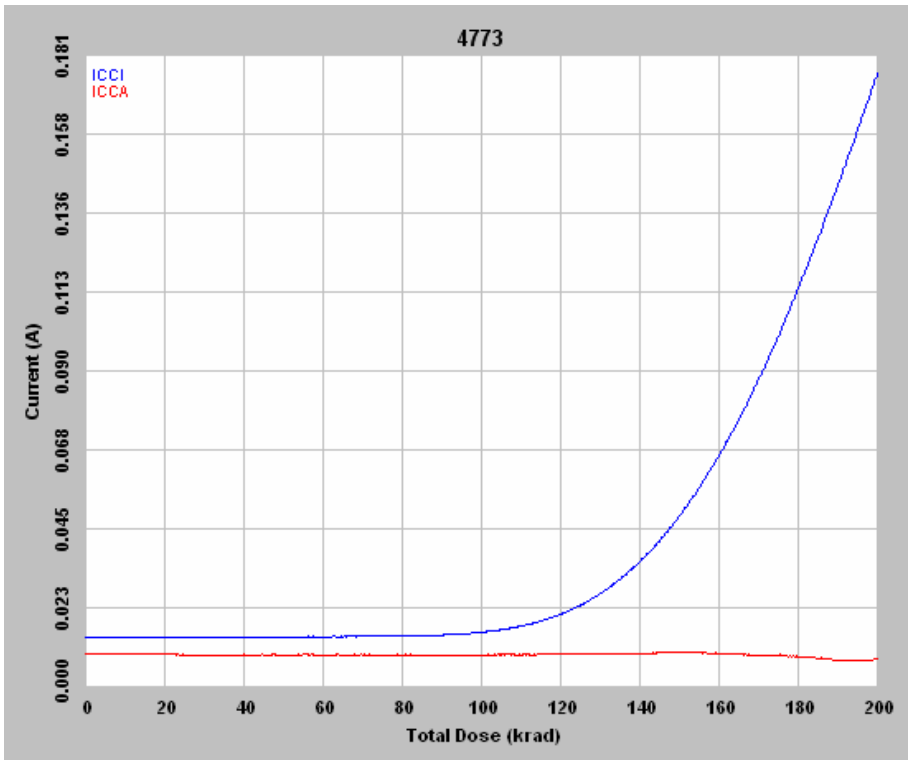

Figure 5 DUT 4773 in-flux I_{CCA} and I_{CCI}

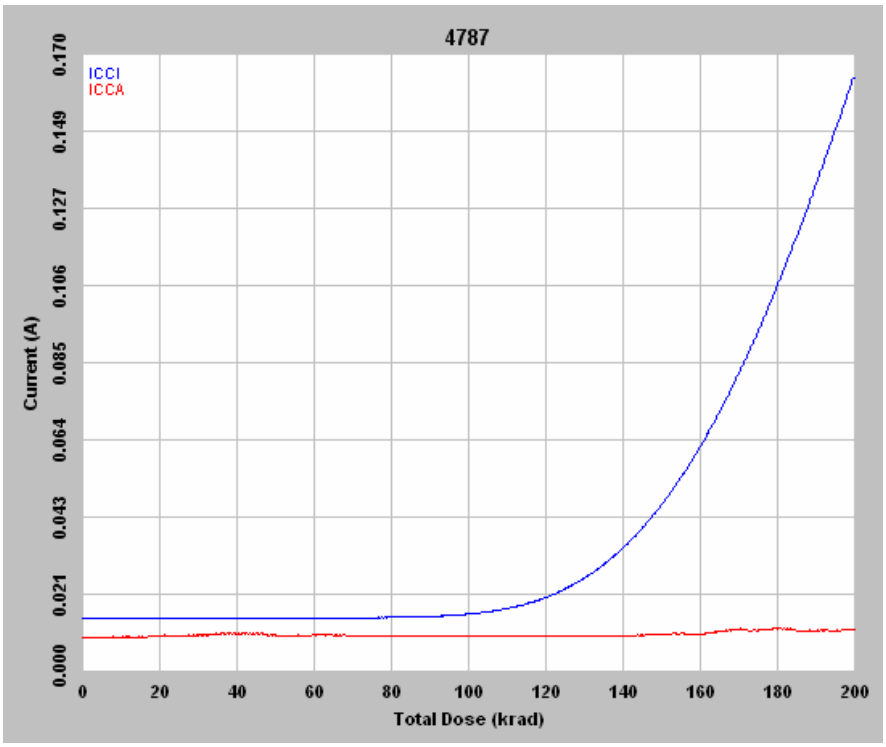

Figure 6 DUT 4787 in-flux I_{CCA} and I_{CCI}

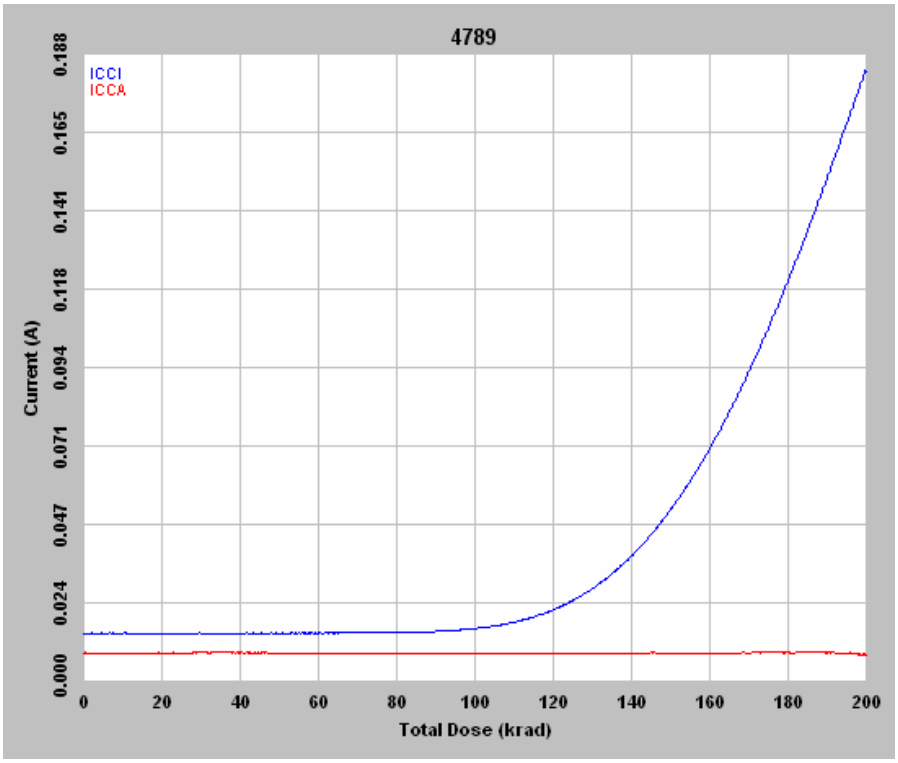

Figure 7 DUT 4789 in-flux I_{CCA} and I_{CCI}

C. *Single-Ended 3.3V-LVTTL V_{IHL}/V_{ILH}*

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design−often just input and output buffers−starts to switch: V_{IH} is the input trip point when the input is going high to low; V_{IL} is the input trip point when the input is going low to high.

Tables 6a and 6b list the pre-irradiation and post-annealing single-ended V_{IL}. In each case, the difference between the pre-irradiation and post-annealing data is negligibly small. Tables 7a and 7b show the pre-irradiation and post-annealing single-ended V_{IH}. Again, the difference between the pre-irradiation and post-annealing data is negligibly small.

Table 6a Pre-Irradiation and Post-Annealing Input Thresholds (V_{IL})

	4750		4755		4766	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.42	1.37	1.38	1.37	1.37	1.35
Shiftin7	1.43	1.37	1.38	1.37	1.36	1.35
Shiftin5	1.44	1.39	1.39	1.39	1.38	1.37
Shiftin4	1.44	1.38	1.39	1.39	1.38	1.37
Shiftin3	1.44	1.39	1.39	1.39	1.39	1.37
Shiftin2	1.45	1.39	1.39	1.39	1.38	1.37
Shiftin1	1.40	1.38	1.40	1.39	1.39	1.38
SEU_sel	1.41	1.37	1.38	1.37	1.37	1.36
zoom_sel_n_0	1.40	1.36	1.40	1.37	1.41	1.36
zoom_sel_n_1	1.41	1.37	1.40	1.37	1.42	1.37
zoom	1.40	1.37	1.39	1.37	1.40	1.37
TOG_n	1.40	1.36	1.39	1.36	1.40	1.37

	4773		4787		4789	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.37	1.36	1.42	1.38	1.37	1.36
Shiftin7	1.38	1.37	1.42	1.38	1.37	1.36
Shiftin5	1.39	1.38	1.44	1.39	1.39	1.38
Shiftin4	1.39	1.38	1.43	1.39	1.38	1.38
Shiftin3	1.39	1.38	1.44	1.39	1.39	1.38
Shiftin2	1.38	1.38	1.44	1.39	1.39	1.38
Shiftin1	1.39	1.38	1.41	1.39	1.39	1.38
SEU_sel	1.39	1.36	1.40	1.37	1.37	1.37
zoom_sel_n_0	1.43	1.37	1.39	1.38	1.38	1.36
zoom_sel_n_1	1.43	1.37	1.39	1.38	1.39	1.36
zoom	1.42	1.37	1.39	1.38	1.38	1.37
TOG_n	1.42	1.37	1.39	1.38	1.38	1.36

Table 6b Pre-Irradiation and Post-Annealing Input Thresholds (V_{IL})

	4750		4755		4766	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.39	1.36	1.38	1.37	1.38	1.36
Resetn	1.40	1.38	1.39	1.38	1.39	1.37
oe_EAQ	1.38	1.35	1.38	1.35	1.39	1.35
enable_HSB	1.45	1.37	1.40	1.38	1.38	1.36
IO_Pattern_Length_1	1.39	1.36	1.40	1.37	1.41	1.36
IO_Pattern_Length_2	1.39	1.37	1.41	1.37	1.41	1.36
A_Pattern_Length_0	1.40	1.37	1.38	1.37	1.38	1.36
A_Pattern_Length_1	1.40	1.36	1.38	1.36	1.38	1.36
IO_Pattern_Length_0	1.39	1.37	1.40	1.37	1.41	1.37
ctest_done_sel_2	1.39	1.37	1.38	1.37	1.37	1.36
IO_Johnson	1.40	1.38	1.40	1.39	1.39	1.38
A_Johnson	1.41	1.37	1.38	1.37	1.38	1.36

	4773		4787		4789	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.38	1.36	1.39	1.38	1.37	1.36
Resetn	1.39	1.38	1.41	1.39	1.39	1.38
oe_EAQ	1.40	1.35	1.38	1.36	1.37	1.34
enable_HSB	1.42	1.37	1.42	1.38	1.39	1.37
IO_Pattern_Length_1	1.41	1.37	1.39	1.38	1.39	1.36
IO_Pattern_Length_2	1.42	1.37	1.39	1.38	1.40	1.36
A_Pattern_Length_0	1.38	1.37	1.40	1.38	1.38	1.37
A_Pattern_Length_1	1.38	1.37	1.40	1.38	1.38	1.37
IO_Pattern_Length_0	1.41	1.37	1.39	1.38	1.39	1.36
ctest_done_sel_2	1.38	1.37	1.40	1.38	1.38	1.37
IO_Johnson	1.41	1.38	1.40	1.39	1.38	1.38
A_Johnson	1.38	1.37	1.41	1.38	1.37	1.37

Table 7a Pre-Irradiation and Post-Annealing Input Thresholds (V_{IH})

	4750		4755		4766	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.72	1.65	1.66	1.65	1.68	1.63
Shiftin7	1.71	1.64	1.66	1.64	1.67	1.62
Shiftin5	1.73	1.66	1.67	1.66	1.69	1.64
Shiftin4	1.74	1.66	1.67	1.67	1.70	1.65
Shiftin3	1.73	1.66	1.67	1.66	1.70	1.65
Shiftin2	1.75	1.67	1.68	1.67	1.70	1.65
Shiftin1	1.68	1.66	1.68	1.67	1.67	1.66
SEU_sel	1.69	1.65	1.79	1.65	1.77	1.64
zoom_sel_n_0	1.69	1.64	1.77	1.64	1.77	1.64
zoom_sel_n_1	1.69	1.64	1.77	1.64	1.77	1.64
zoom	1.69	1.64	1.76	1.65	1.76	1.65
TOG_n	1.68	1.63	1.75	1.64	1.75	1.64

	4773		4787		4789	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Shiftin8	1.70	1.64	1.71	1.66	1.65	1.64
Shiftin7	1.70	1.64	1.70	1.66	1.65	1.64
Shiftin5	1.71	1.65	1.72	1.67	1.67	1.66
Shiftin4	1.71	1.66	1.72	1.67	1.67	1.66
Shiftin3	1.71	1.65	1.72	1.67	1.66	1.65
Shiftin2	1.71	1.66	1.73	1.68	1.67	1.66
Shiftin1	1.67	1.66	1.69	1.67	1.67	1.66
SEU_sel	1.75	1.64	1.68	1.65	1.67	1.64
zoom_sel_n_0	1.76	1.65	1.67	1.66	1.77	1.65
zoom_sel_n_1	1.76	1.65	1.68	1.66	1.77	1.64
zoom	1.74	1.65	1.68	1.66	1.77	1.65
TOG_n	1.74	1.65	1.68	1.66	1.76	1.65

Table 7b Pre-Irradiation and Post-Annealing Input Thresholds (V_{IH})

	4750		4755		4766	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.67	1.64	1.68	1.64	1.68	1.63
Resetn	1.69	1.66	1.67	1.66	1.68	1.65
oe_EAQ	1.66	1.62	1.70	1.62	1.68	1.62
enable_HSB	1.72	1.63	1.82	1.64	1.79	1.63
IO_Pattern_Length_1	1.67	1.64	1.72	1.64	1.71	1.64
IO_Pattern_Length_2	1.67	1.64	1.72	1.64	1.71	1.64
A_Pattern_Length_0	1.67	1.64	1.68	1.64	1.67	1.64
A_Pattern_Length_1	1.67	1.64	1.68	1.64	1.67	1.63
IO_Pattern_Length_0	1.67	1.64	1.72	1.64	1.71	1.64
ctest_done_sel_2	1.67	1.64	1.66	1.64	1.66	1.63
IO_Johnson	1.69	1.66	1.72	1.66	1.71	1.65
A_Johnson	1.69	1.64	1.70	1.64	1.69	1.64

	4773		4787		4789	
Pin Name	Pre-irrad	Post-an	Pre-irrad	Post-an	Pre-irrad	Post-an
Set_n	1.68	1.65	1.67	1.66	1.68	1.64
Resetn	1.68	1.65	1.69	1.67	1.67	1.65
oe_EAQ	1.69	1.63	1.66	1.64	1.69	1.62
enable_HSB	1.82	1.64	1.70	1.65	1.68	1.65
IO_Pattern_Length_1	1.71	1.65	1.68	1.66	1.71	1.64
IO_Pattern_Length_2	1.71	1.65	1.69	1.66	1.71	1.64
A_Pattern_Length_0	1.69	1.67	1.68	1.67	1.66	1.66
A_Pattern_Length_1	1.69	1.67	1.68	1.67	1.66	1.67
IO_Pattern_Length_	1.71	1.65	1.68	1.66	1.71	1.64

0						
ctest_done_sel_2	1.66	1.64	1.68	1.65	1.65	1.64
IO_Johnson	1.71	1.67	1.69	1.68	1.71	1.66
A_Johnson	1.73	1.67	1.69	1.67	1.66	1.67

D. Output-Drive Voltage (V_{OL}/V_{OH})

The output drive voltage V_{OL}/V_{OH} is measured at an output pin when it is at Low/High state and sinking/sourcing 1, 12, 20, 50, or 100 mA. In each case, the post-annealing value is within the specifications limit, and it is within ±10% of pre-irradiation data.

Table 8a Pre-Irradiation and Post-Annealing V_{OL} for DUT 4750 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.008	0.008	0.088	0.084	0.147	0.140	0.376	0.356	0.806	0.762
Shiftout7	0.009	0.009	0.097	0.093	0.162	0.155	0.413	0.394	0.884	0.840
RAM_out_EAQ_1	0.009	0.009	0.095	0.086	0.159	0.143	0.402	0.363	0.856	0.774
Shiftout3	0.009	0.009	0.096	0.091	0.161	0.151	0.409	0.382	0.876	0.816
RAM_Monitor_EAQ	0.009	0.008	0.107	0.093	0.178	0.155	0.454	0.394	0.967	0.839
Shiftout8	0.009	0.009	0.098	0.093	0.164	0.155	0.416	0.392	0.889	0.835
PADN_LVPECL_1	0.009	0.009	0.084	0.081	0.140	0.135	0.355	0.341	0.764	0.734
PADN_LVPECL_0	0.009	0.010	0.085	0.086	0.141	0.143	0.356	0.361	0.766	0.773
PADP_LVPECL_0	0.012	0.010	0.105	0.080	0.173	0.132	0.428	0.330	0.899	0.709
PADP_LVPECL_1	0.010	0.010	0.088	0.081	0.146	0.135	0.368	0.339	0.789	0.725
Global_Monitor_EAQ	0.008	0.007	0.084	0.078	0.141	0.129	0.359	0.330	0.775	0.711
RAM_out_EAQ_0	0.008	0.007	0.084	0.080	0.140	0.133	0.357	0.340	0.769	0.728
Array_out_EAQ_1	0.007	0.008	0.091	0.087	0.152	0.145	0.389	0.370	0.833	0.789

Table 8b Pre-Irradiation and Post-Annealing V_{OL} for DUT 4755 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.008	0.008	0.090	0.086	0.150	0.143	0.381	0.364	0.819	0.778
Shiftout7	0.009	0.009	0.098	0.095	0.164	0.157	0.418	0.400	0.897	0.853
RAM_out_EAQ_1	0.010	0.009	0.106	0.090	0.177	0.149	0.450	0.380	0.967	0.812
Shiftout3	0.009	0.009	0.096	0.092	0.161	0.153	0.410	0.389	0.879	0.832
RAM_Monitor_EAQ	0.009	0.008	0.104	0.094	0.173	0.157	0.442	0.399	0.939	0.851
Shiftout8	0.010	0.009	0.100	0.095	0.166	0.157	0.422	0.399	0.904	0.851
PADN_LVPECL_1	0.010	0.009	0.106	0.082	0.176	0.136	0.443	0.346	0.952	0.748
PADN_LVPECL_0	0.009	0.010	0.087	0.089	0.145	0.148	0.367	0.374	0.789	0.802
PADP_LVPECL_0	0.011	0.010	0.088	0.082	0.145	0.134	0.366	0.338	0.787	0.725
PADP_LVPECL_1	0.010	0.010	0.087	0.083	0.144	0.137	0.365	0.345	0.784	0.740
Global_Monitor_EAQ	0.008	0.007	0.084	0.079	0.140	0.131	0.359	0.335	0.777	0.724
RAM_out_EAQ_0	0.008	0.008	0.086	0.084	0.143	0.140	0.365	0.356	0.785	0.766
Array_out_EAQ_1	0.008	0.008	0.093	0.088	0.155	0.147	0.395	0.375	0.847	0.802

Table 8c Pre-Irradiation and Post-Annealing V_{OL} for DUT 4766 at Dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.008	0.008	0.091	0.086	0.151	0.143	0.385	0.364	0.827	0.780
Shiftout7	0.009	0.009	0.099	0.095	0.165	0.159	0.422	0.402	0.902	0.856
RAM_out_EAQ_1	0.010	0.009	0.097	0.088	0.162	0.146	0.410	0.372	0.878	0.793
Shiftout3	0.009	0.009	0.097	0.092	0.162	0.154	0.412	0.390	0.880	0.831
RAM_Monitor_EAQ	0.008	0.008	0.103	0.095	0.172	0.159	0.438	0.405	0.934	0.863
Shiftout8	0.010	0.009	0.100	0.095	0.167	0.158	0.424	0.400	0.906	0.851
PADN_LVPECL_1	0.011	0.009	0.114	0.082	0.192	0.136	0.463	0.346	0.993	0.746
PADN_LVPECL_0	0.009	0.009	0.088	0.085	0.145	0.141	0.367	0.355	0.787	0.763
PADP_LVPECL_0	0.011	0.011	0.094	0.082	0.155	0.135	0.391	0.338	0.836	0.725
PADP_LVPECL_1	0.010	0.010	0.088	0.083	0.146	0.137	0.368	0.344	0.790	0.737
Global_Monitor_EAQ	0.008	0.007	0.083	0.079	0.140	0.131	0.356	0.334	0.770	0.719
RAM_out_EAQ_0	0.008	0.008	0.087	0.082	0.145	0.137	0.370	0.349	0.798	0.752
Array_out_EAQ_1	0.008	0.008	0.093	0.088	0.156	0.148	0.398	0.378	0.855	0.807

Table 8d Pre-Irradiation and Post-Annealing V_{OL} for DUT 4773 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.008	0.008	0.091	0.086	0.152	0.144	0.387	0.367	0.833	0.788
Shiftout7	0.009	0.009	0.100	0.096	0.168	0.161	0.427	0.409	0.912	0.871
RAM_out_EAQ_1	0.010	0.009	0.107	0.089	0.178	0.148	0.452	0.377	0.965	0.805
Shiftout3	0.009	0.008	0.100	0.094	0.166	0.156	0.423	0.396	0.906	0.846
RAM_Monitor_EAQ	0.009	0.008	0.101	0.097	0.170	0.162	0.433	0.412	0.923	0.878
Shiftout8	0.009	0.009	0.101	0.096	0.169	0.160	0.429	0.406	0.918	0.866
PADN_LVPECL_1	0.010	0.009	0.093	0.082	0.154	0.137	0.392	0.347	0.841	0.749
PADN_LVPECL_0	0.009	0.010	0.088	0.087	0.147	0.144	0.371	0.365	0.799	0.783
PADP_LVPECL_0	0.011	0.010	0.094	0.083	0.154	0.136	0.390	0.343	0.836	0.736
PADP_LVPECL_1	0.010	0.010	0.088	0.083	0.146	0.138	0.369	0.347	0.795	0.746
Global_Monitor_EAQ	0.008	0.007	0.085	0.080	0.141	0.133	0.360	0.338	0.780	0.730
RAM_out_EAQ_0	0.008	0.007	0.087	0.083	0.146	0.138	0.372	0.351	0.802	0.755
Array_out_EAQ_1	0.008	0.007	0.094	0.090	0.157	0.150	0.401	0.384	0.862	0.821

Table 8e Pre-Irradiation and Post-Annealing V_{OL} for DUT 4787 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.008	0.008	0.089	0.085	0.149	0.142	0.379	0.362	0.813	0.775
Shiftout7	0.009	0.009	0.098	0.096	0.163	0.159	0.414	0.404	0.883	0.860
RAM_out_EAQ_1	0.009	0.009	0.097	0.087	0.162	0.145	0.410	0.367	0.873	0.784
Shiftout3	0.009	0.008	0.097	0.092	0.161	0.153	0.409	0.388	0.873	0.827
RAM_Monitor_EAQ	0.008	0.008	0.100	0.094	0.168	0.158	0.428	0.402	0.911	0.855
Shiftout8	0.009	0.009	0.099	0.094	0.164	0.156	0.417	0.396	0.888	0.843
PADN_LVPECL_1	0.009	0.009	0.088	0.082	0.146	0.136	0.369	0.345	0.793	0.743

PADN_LVPECL_0	0.010	0.009	0.090	0.086	0.149	0.142	0.378	0.360	0.810	0.773
PADP_LVPECL_0	0.011	0.010	0.088	0.082	0.145	0.134	0.365	0.338	0.782	0.725
PADP_LVPECL_1	0.010	0.010	0.088	0.083	0.146	0.137	0.369	0.346	0.790	0.742
Global_Monitor_EAQ	0.008	0.007	0.085	0.078	0.142	0.130	0.362	0.332	0.779	0.715
RAM_out_EAQ_0	0.008	0.007	0.085	0.082	0.142	0.137	0.363	0.349	0.780	0.749
Array_out_EAQ_1	0.008	0.008	0.092	0.088	0.153	0.147	0.392	0.375	0.841	0.802

Table 8f Pre-Irradiation and Post-Annealing V_{OL} for DUT 4789 at Dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	0.008	0.008	0.090	0.087	0.151	0.144	0.385	0.368	0.828	0.790
Shiftout7	0.009	0.009	0.101	0.099	0.168	0.165	0.428	0.420	0.914	0.894
RAM_out_EAQ_1	0.009	0.009	0.096	0.088	0.160	0.147	0.405	0.373	0.867	0.798
Shiftout3	0.009	0.008	0.098	0.093	0.163	0.155	0.415	0.393	0.889	0.840
RAM_Monitor_EAQ	0.008	0.008	0.102	0.096	0.171	0.160	0.436	0.409	0.929	0.869
Shiftout8	0.010	0.009	0.101	0.096	0.168	0.160	0.425	0.405	0.909	0.865
PADN_LVPECL_1	0.011	0.009	0.105	0.083	0.174	0.137	0.427	0.348	0.909	0.750
PADN_LVPECL_0	0.010	0.010	0.090	0.099	0.149	0.165	0.379	0.407	0.812	0.872
PADP_LVPECL_0	0.011	0.010	0.091	0.082	0.150	0.135	0.378	0.339	0.810	0.728
PADP_LVPECL_1	0.010	0.010	0.089	0.084	0.146	0.138	0.369	0.349	0.794	0.747
Global_Monitor_EAQ	0.008	0.007	0.084	0.079	0.140	0.132	0.357	0.338	0.774	0.729
RAM_out_EAQ_0	0.008	0.007	0.087	0.082	0.145	0.137	0.369	0.350	0.795	0.753
Array_out_EAQ_1	0.008	0.008	0.093	0.089	0.156	0.150	0.399	0.382	0.857	0.818

Table 9a Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4750 at dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.96	2.85	2.85	2.77	2.77	2.46	2.46	1.78	1.77
Shiftout7	2.96	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.67	1.66
RAM_out_EAQ_1	2.96	2.96	2.84	2.85	2.76	2.77	2.43	2.44	1.71	1.74
Shiftout3	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.67	1.68
RAM_Monitor_EAQ	2.96	2.95	2.83	2.84	2.74	2.75	2.37	2.41	1.60	1.68
Shiftout8	2.96	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.66	1.66
PADN_LVPECL_1	2.96	2.96	2.86	2.86	2.78	2.78	2.48	2.48	1.82	1.83
PADN_LVPECL_0	2.96	2.96	2.86	2.85	2.78	2.78	2.48	2.47	1.82	1.79
PADP_LVPECL_0	2.95	2.95	2.84	2.85	2.76	2.78	2.44	2.48	1.76	1.83
PADP_LVPECL_1	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.47	1.80	1.81
Global_Monitor_EAQ	2.96	2.95	2.85	2.85	2.78	2.78	2.46	2.47	1.77	1.78
RAM_out_EAQ_0	2.96	2.96	2.85	2.85	2.78	2.77	2.47	2.46	1.79	1.78
Array_out_EAQ_1	2.96	2.96	2.85	2.85	2.77	2.77	2.44	2.44	1.74	1.74

Table 9b Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4755 at dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.96	2.85	2.85	2.77	2.77	2.45	2.45	1.77	1.76
Shiftout7	2.96	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.68	1.67
RAM_out_EAQ_1	2.96	2.96	2.83	2.85	2.74	2.77	2.38	2.44	1.64	1.73
Shiftout3	2.95	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.68	1.67
RAM_Monitor_EAQ	2.96	2.95	2.84	2.84	2.75	2.75	2.39	2.40	1.62	1.66
Shiftout8	2.96	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.67	1.67

PADN_LVPECL_1	2.95	2.96	2.84	2.86	2.76	2.78	2.43	2.48	1.72	1.81
PADN_LVPECL_0	2.95	2.96	2.85	2.85	2.78	2.77	2.47	2.45	1.80	1.76
PADP_LVPECL_0	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.48	1.80	1.81
PADP_LVPECL_1	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.47	1.80	1.79
Global_Monitor_EAQ	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.47	1.78	1.78
RAM_out_EAQ_0	2.95	2.96	2.85	2.85	2.78	2.78	2.46	2.46	1.78	1.78
Array_out_EAQ_1	2.96	2.96	2.85	2.85	2.77	2.76	2.44	2.44	1.73	1.73

Table 9c Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4766 at dose of 300krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.96	2.85	2.85	2.77	2.77	2.45	2.45	1.75	1.74
Shiftout7	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.40	1.65	1.65
RAM_out_EAQ_1	2.96	2.96	2.84	2.85	2.76	2.76	2.42	2.44	1.69	1.71
Shiftout3	2.96	2.95	2.84	2.84	2.75	2.75	2.41	2.41	1.65	1.64
RAM_Monitor_EAQ	2.96	2.95	2.84	2.84	2.75	2.75	2.39	2.40	1.62	1.64
Shiftout8	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.40	1.64	1.64
PADN_LVPECL_1	2.95	2.96	2.84	2.86	2.76	2.78	2.43	2.48	1.72	1.82
PADN_LVPECL_0	2.95	2.96	2.85	2.85	2.78	2.78	2.47	2.47	1.80	1.81
PADP_LVPECL_0	2.95	2.95	2.85	2.85	2.77	2.78	2.45	2.48	1.76	1.82
PADP_LVPECL_1	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.47	1.80	1.80
Global_Monitor_EAQ	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.47	1.77	1.77
RAM_out_EAQ_0	2.96	2.96	2.85	2.85	2.77	2.77	2.46	2.45	1.75	1.74
Array_out_EAQ_1	2.96	2.96	2.85	2.85	2.76	2.76	2.43	2.43	1.71	1.71

Table 9d Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4773 at dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.96	2.85	2.85	2.77	2.77	2.45	2.46	1.76	1.77
Shiftout7	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.40	1.64	1.64
RAM_out_EAQ_1	2.96	2.96	2.83	2.85	2.74	2.77	2.39	2.44	1.63	1.73
Shiftout3	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.41	1.63	1.65
RAM_Monitor_EAQ	2.96	2.96	2.84	2.84	2.75	2.75	2.40	2.40	1.64	1.65
Shiftout8	2.96	2.95	2.84	2.84	2.75	2.75	2.39	2.40	1.62	1.64
PADN_LVPECL_1	2.95	2.96	2.85	2.86	2.77	2.78	2.45	2.49	1.76	1.84
PADN_LVPECL_0	2.95	2.96	2.85	2.85	2.78	2.78	2.47	2.47	1.81	1.81
PADP_LVPECL_0	2.96	2.95	2.85	2.86	2.77	2.78	2.45	2.48	1.77	1.83
PADP_LVPECL_1	2.96	2.95	2.85	2.85	2.78	2.78	2.47	2.48	1.81	1.82
Global_Monitor_EAQ	2.96	2.96	2.85	2.85	2.78	2.78	2.47	2.47	1.77	1.78
RAM_out_EAQ_0	2.96	2.96	2.85	2.85	2.77	2.77	2.46	2.46	1.76	1.77
Array_out_EAQ_1	2.96	2.96	2.85	2.85	2.76	2.77	2.44	2.44	1.73	1.73

Table 9e Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4787 at dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.96	2.85	2.85	2.78	2.77	2.46	2.47	1.81	1.81
Shiftout7	2.96	2.95	2.84	2.84	2.76	2.75	2.42	2.41	1.69	1.68
RAM_out_EAQ_1	2.96	2.96	2.85	2.85	2.76	2.77	2.43	2.46	1.74	1.79
Shiftout3	2.96	2.95	2.84	2.84	2.76	2.76	2.42	2.42	1.70	1.71
RAM_Monitor_EAQ	2.96	2.96	2.84	2.84	2.75	2.76	2.41	2.42	1.69	1.70

Shiftout8	2.96	2.95	2.84	2.84	2.75	2.76	2.41	2.42	1.69	1.69
PADN_LVPECL_1	2.96	2.96	2.85	2.86	2.78	2.78	2.47	2.49	1.82	1.86
PADN_LVPECL_0	2.96	2.96	2.85	2.86	2.78	2.78	2.47	2.48	1.81	1.84
PADP_LVPECL_0	2.96	2.96	2.86	2.86	2.78	2.78	2.48	2.49	1.84	1.86
PADP_LVPECL_1	2.96	2.95	2.85	2.85	2.78	2.78	2.48	2.48	1.83	1.84
Global_Monitor_EAQ	2.96	2.96	2.85	2.86	2.78	2.78	2.46	2.48	1.78	1.81
RAM_out_EAQ_0	2.96	2.96	2.86	2.85	2.78	2.78	2.47	2.47	1.81	1.80
Array_out_EAQ_1	2.96	2.96	2.85	2.85	2.77	2.77	2.45	2.45	1.78	1.78

Table 9f Pre-Irradiation and Post-Annealing V_{OH} (V) for DUT 4789 at dose of 200krad

	1mA		12mA		20mA		50mA		100mA	
Pin Name	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
Array_out_EAQ_2	2.96	2.96	2.85	2.85	2.77	2.77	2.45	2.45	1.75	1.75
Shiftout7	2.96	2.95	2.84	2.83	2.75	2.75	2.40	2.39	1.64	1.62
RAM_out_EAQ_1	2.96	2.96	2.84	2.85	2.76	2.77	2.42	2.44	1.69	1.71
Shiftout3	2.95	2.95	2.84	2.84	2.75	2.76	2.41	2.41	1.65	1.65
RAM_Monitor_EAQ	2.96	2.96	2.84	2.84	2.75	2.75	2.38	2.39	1.60	1.62
Shiftout8	2.96	2.95	2.84	2.84	2.75	2.75	2.40	2.40	1.63	1.64
PADN_LVPECL_1	2.95	2.96	2.84	2.86	2.76	2.78	2.43	2.48	1.72	1.81
PADN_LVPECL_0	2.95	2.96	2.85	2.84	2.77	2.77	2.46	2.44	1.77	1.74
PADP_LVPECL_0	2.96	2.96	2.85	2.86	2.77	2.78	2.46	2.48	1.77	1.82
PADP_LVPECL_1	2.96	2.95	2.85	2.85	2.77	2.78	2.47	2.47	1.79	1.79
Global_Monitor_EAQ	2.96	2.96	2.85	2.85	2.78	2.78	2.47	2.47	1.77	1.77
RAM_out_EAQ_0	2.96	2.96	2.85	2.85	2.77	2.77	2.46	2.46	1.75	1.75
Array_out_EAQ_1	2.96	2.96	2.85	2.85	2.77	2.77	2.44	2.44	1.72	1.72

E. Propagation Delay

Table 10 lists the pre-irradiation and post-annealing propagation delay and percentage change (degradations) for each DUT. Every DUT passes the ±10%-degradation criterion.

Table 10a Radiation-Induced Propagation Delay Degradations

	Propagation Delay (us)								
	4750			4755			4766		
Measurement	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn
Delay0	1.368	1.351	-1.28%	1.398	1.384	-0.94%	1.425	1.408	-1.20%
Delay1	1.373	1.356	-1.27%	1.400	1.387	-0.96%	1.434	1.417	-1.19%
Delay2	1.413	1.395	-1.31%	1.439	1.425	-0.99%	1.478	1.459	-1.24%
Delay3	1.367	1.349	-1.30%	1.390	1.377	-0.96%	1.433	1.416	-1.19%
Delay4	1.385	1.367	-1.30%	1.411	1.398	-0.95%	1.447	1.429	-1.21%
Delay_Chain	5.710	5.610	-1.75%	5.825	5.745	-1.37%	5.895	5.805	-1.53%

	Propagation Delay (us)								
	4773			4787			4789		
Measurement	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn	Pre-rad	Post-an	Degrdn
Delay0	1.414	1.398	-1.12%	1.364	1.350	-1.08%	1.412	1.398	-0.98%
Delay1	1.424	1.408	-1.12%	1.368	1.353	-1.08%	1.419	1.405	-0.99%
Delay2	1.463	1.447	-1.09%	1.410	1.395	-1.06%	1.461	1.446	-1.01%

Delay3	1.421	1.406	-1.09%	1.363	1.348	-1.10%	1.416	1.401	-1.02%
Delay4	1.434	1.418	-1.12%	1.381	1.365	-1.11%	1.431	1.416	-1.02%
Delay_Chain	5.855	5.770	-1.45%	5.705	5.625	-1.40%	5.835	5.755	-1.37%

G. Transition Time

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

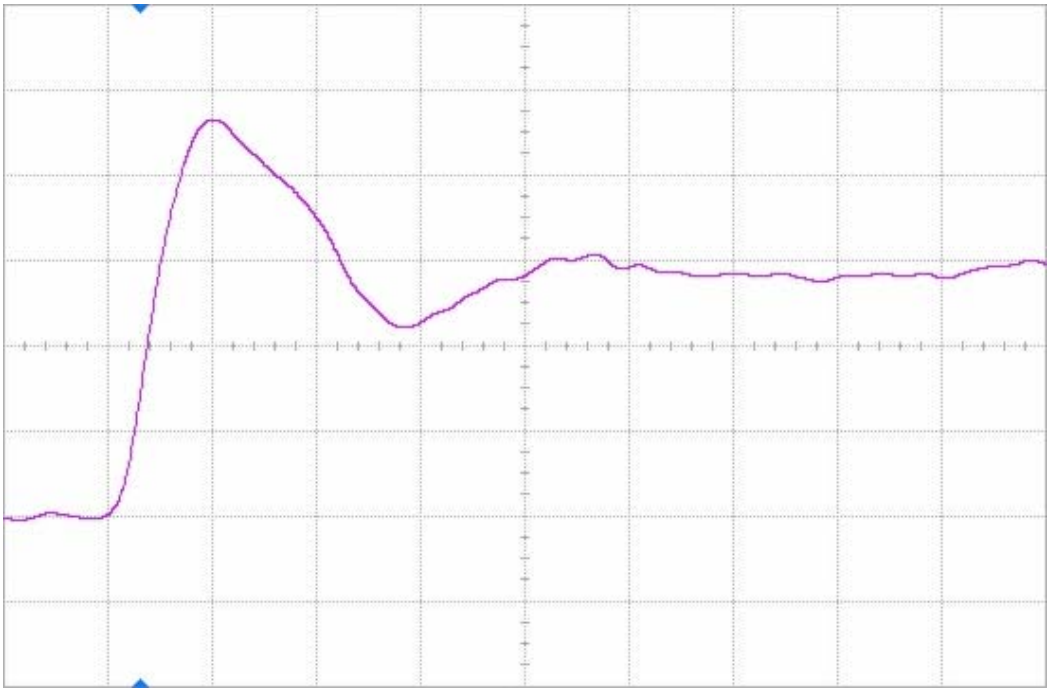

Figure 8(a) DUT 4750 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

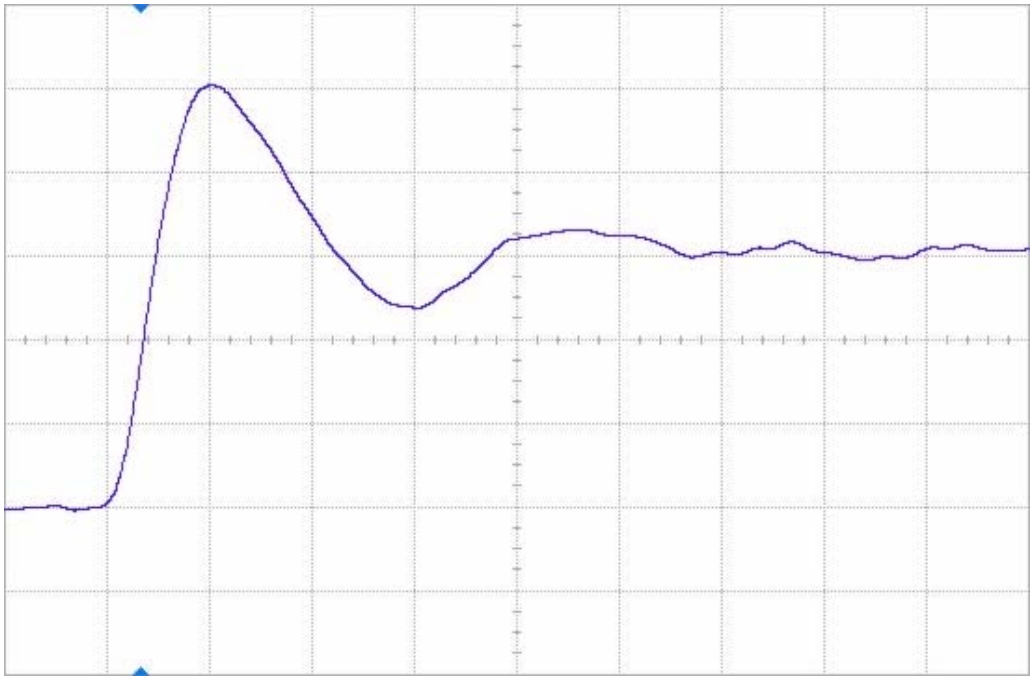

Figure 8(b) DUT 4750 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

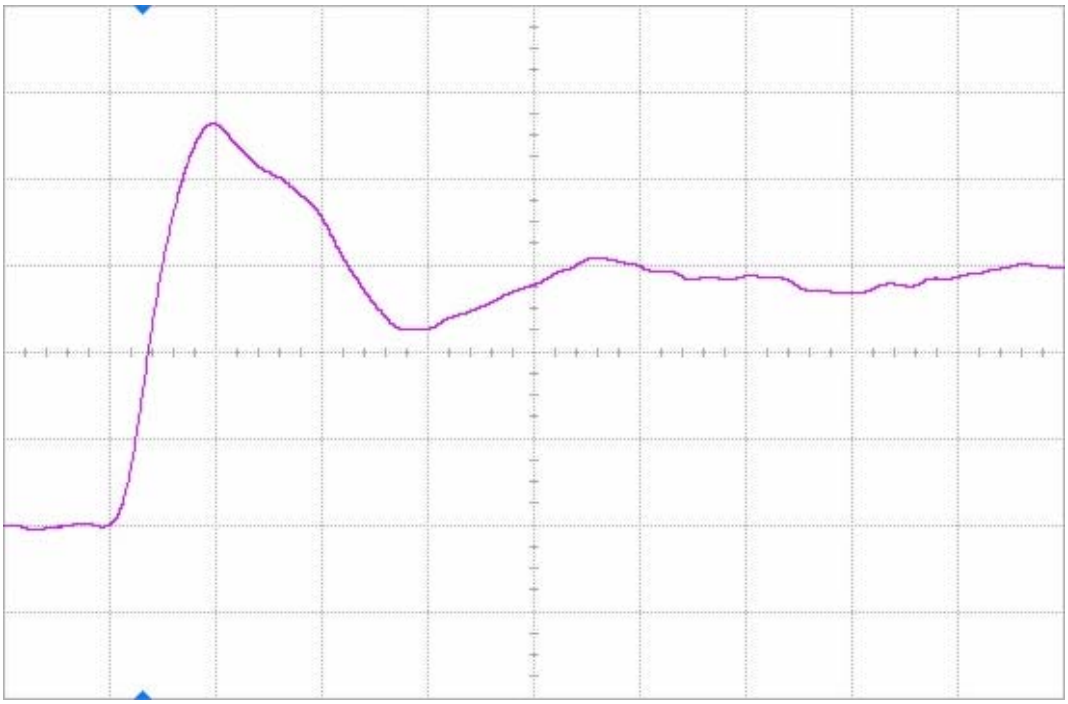

Figure 9(a) DUT 4755 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

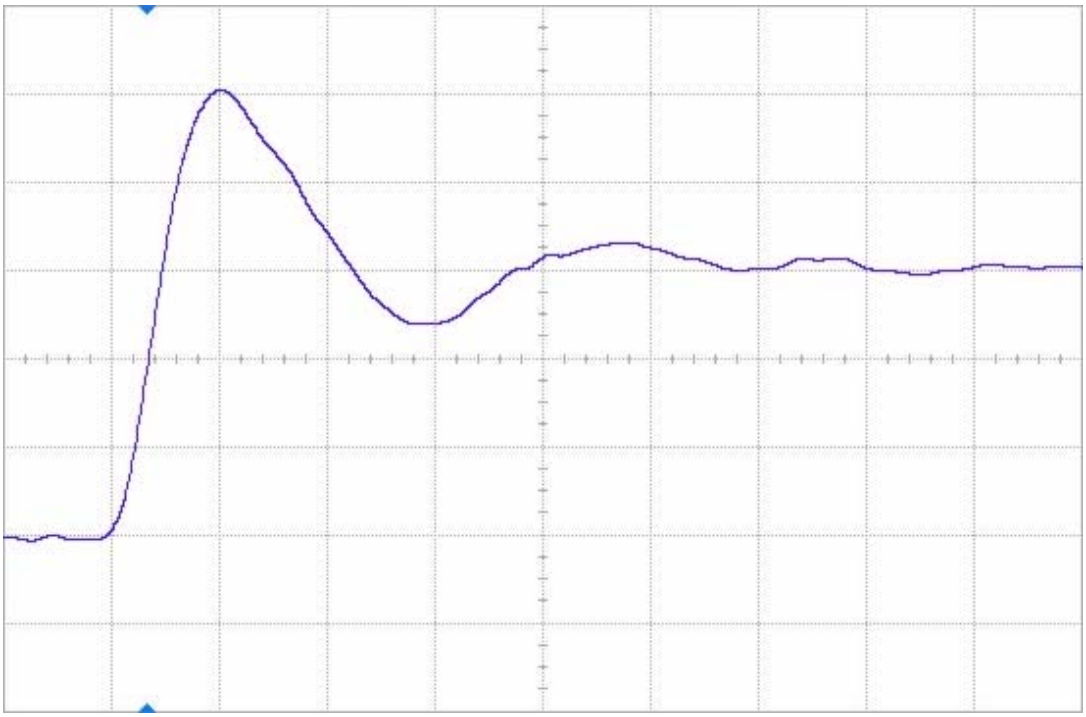

Figure 9(b) DUT 4755 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

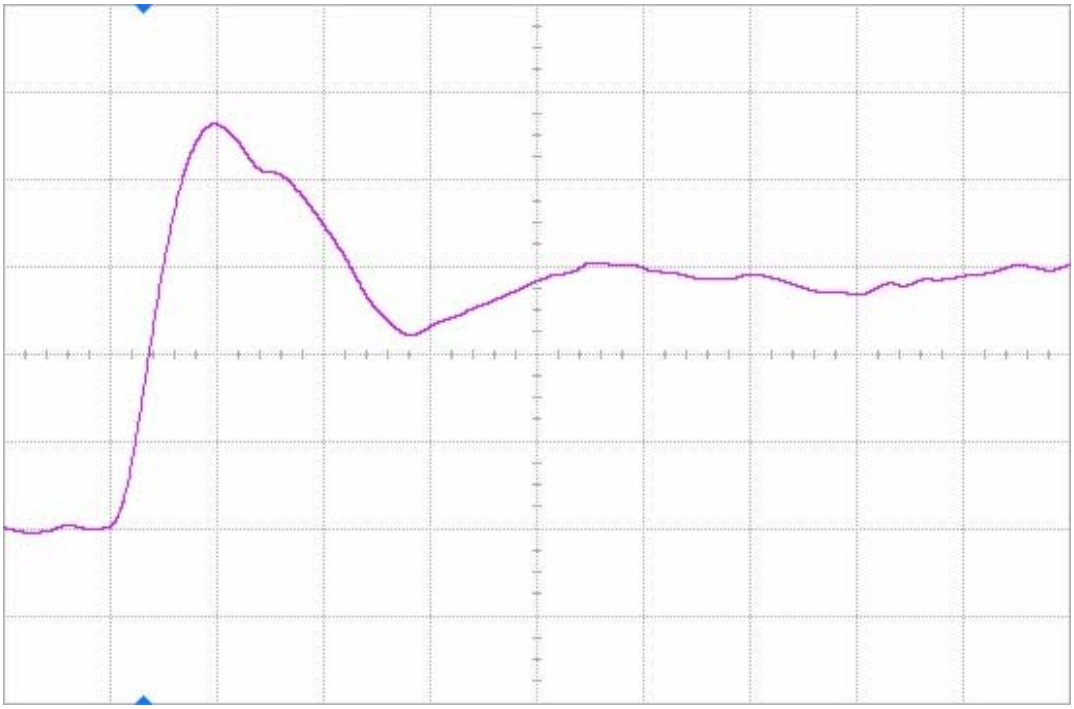

Figure 10(a) DUT 4766 pre-radiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

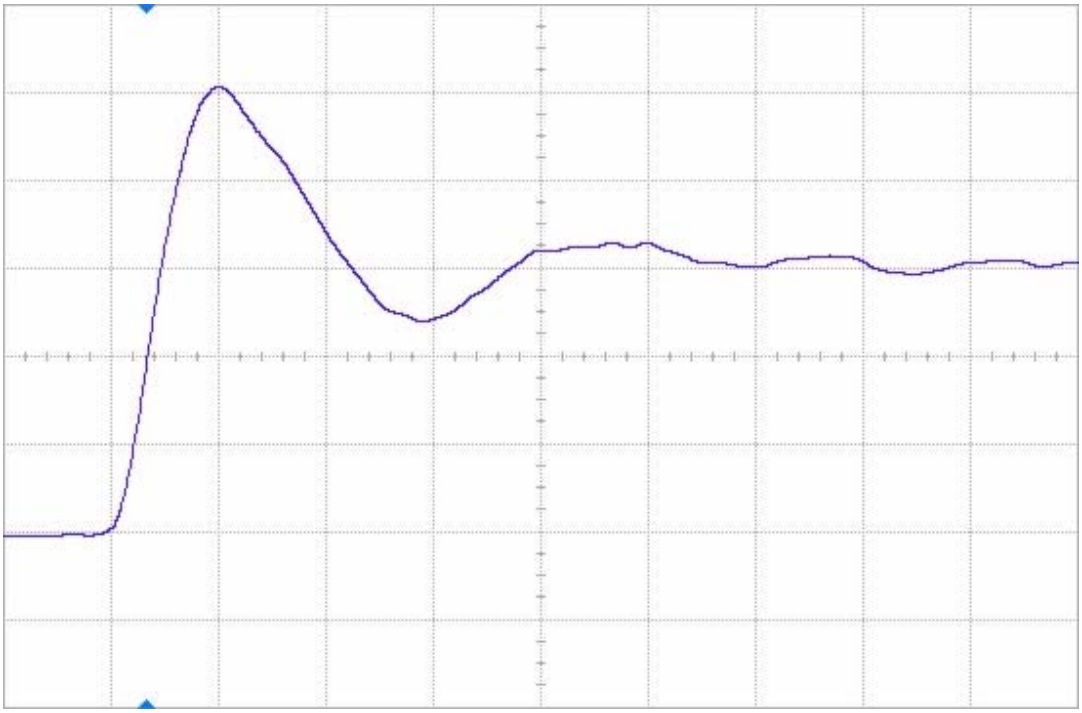

Figure 10(b) DUT 4766 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

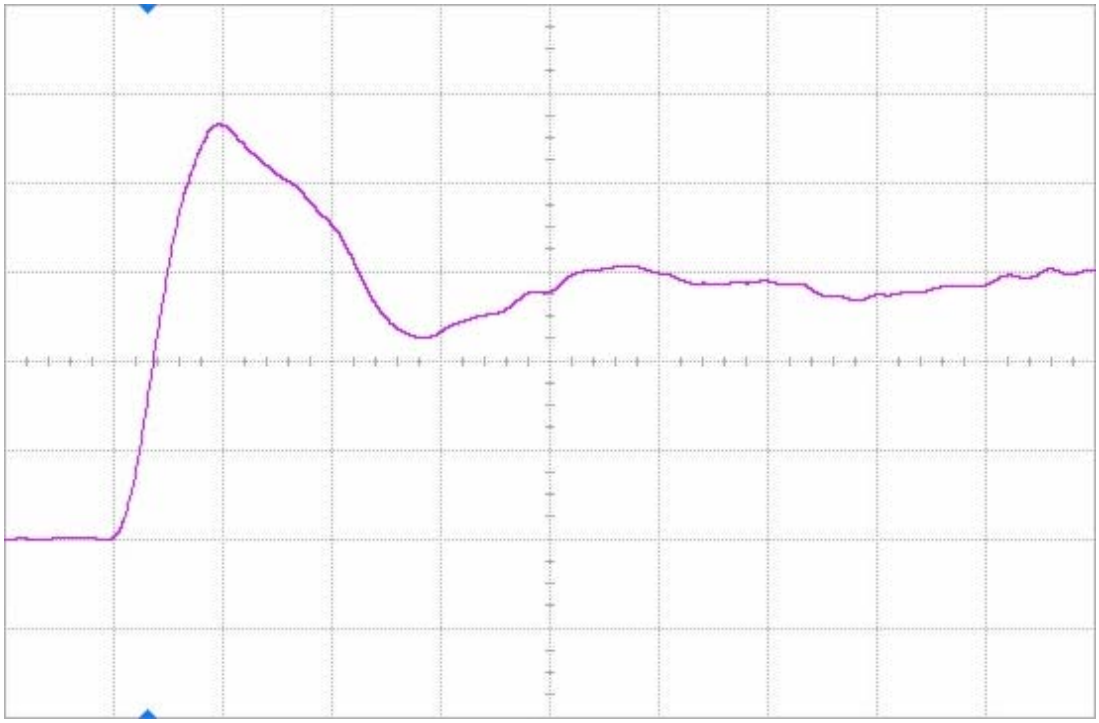

Figure 11(a) DUT 4773 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

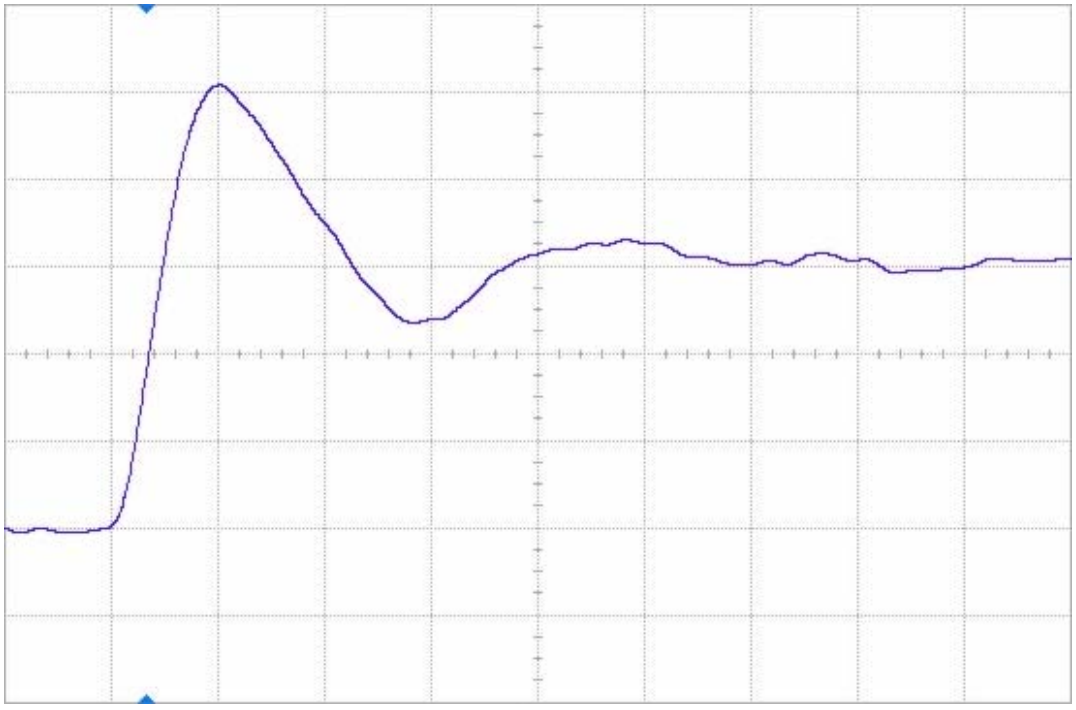

Figure 11(b) DUT 4773 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

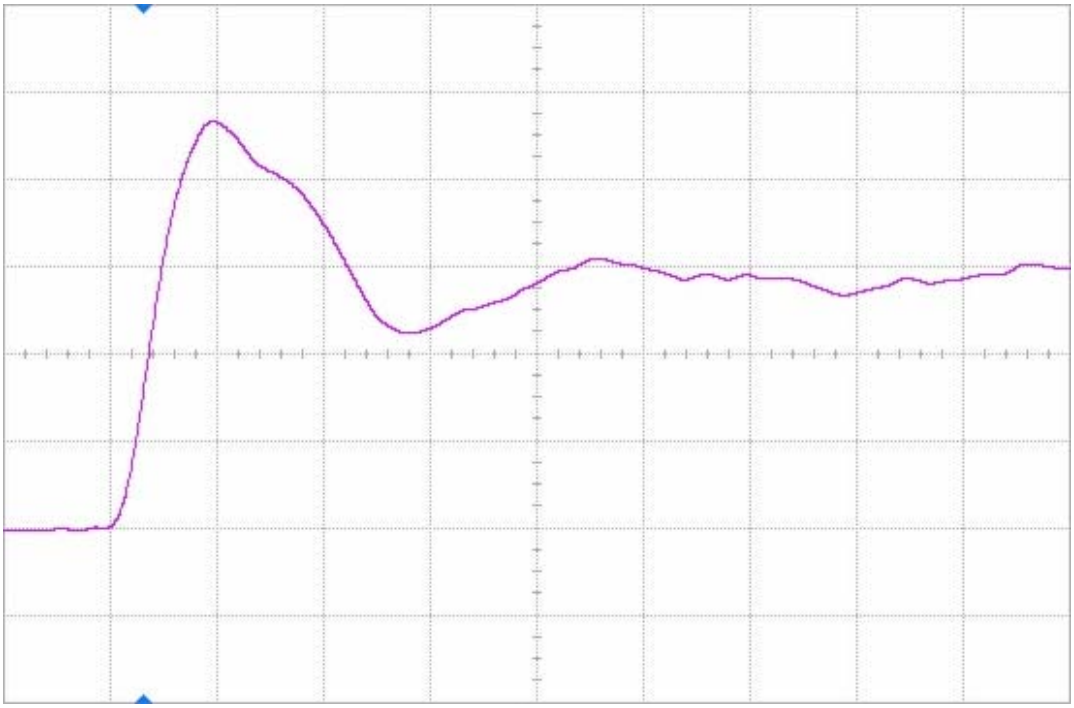

Figure 12(a) DUT 4787 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

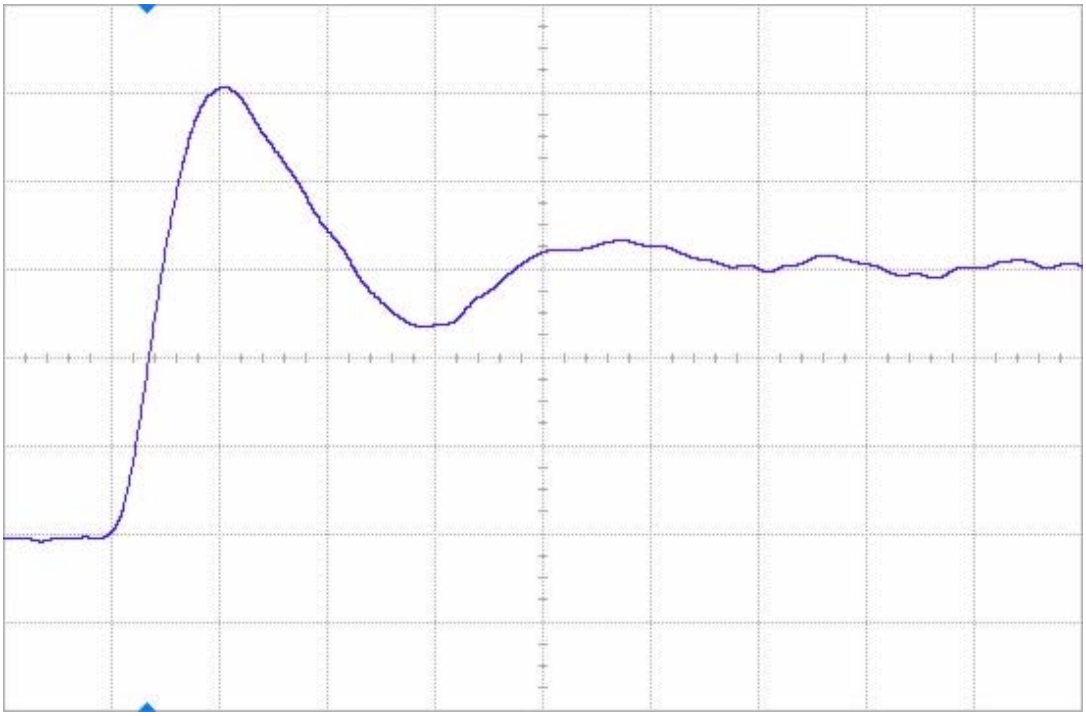

Figure 12(b) DUT 4787 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

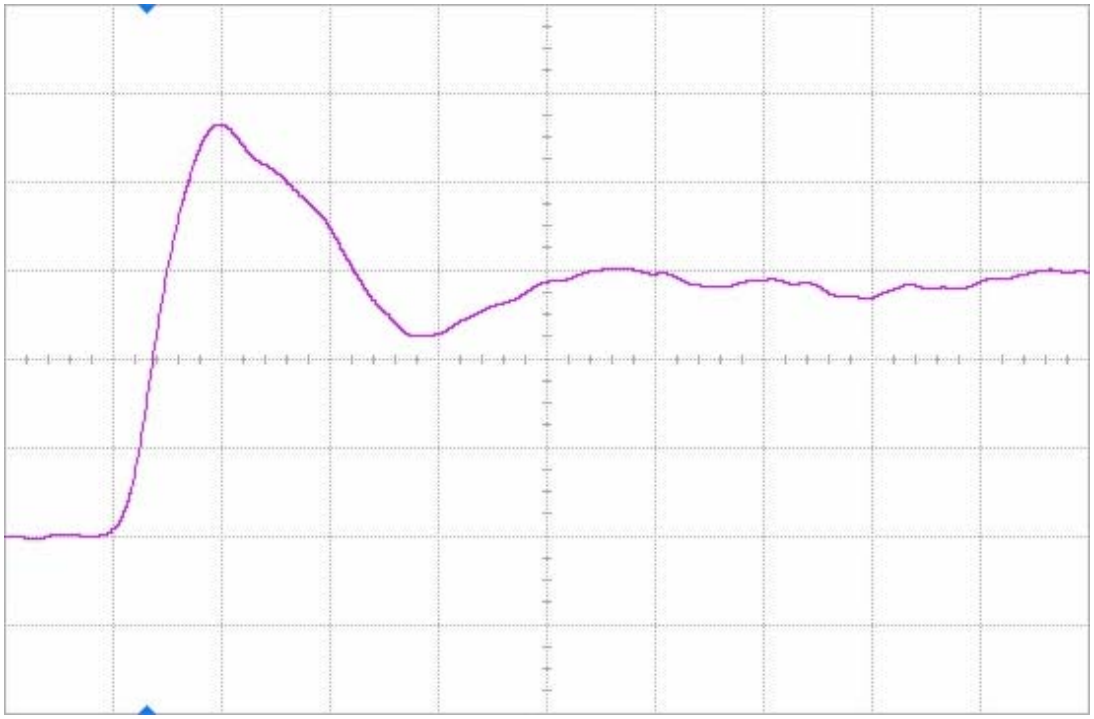

Figure 13(a) DUT 4789 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

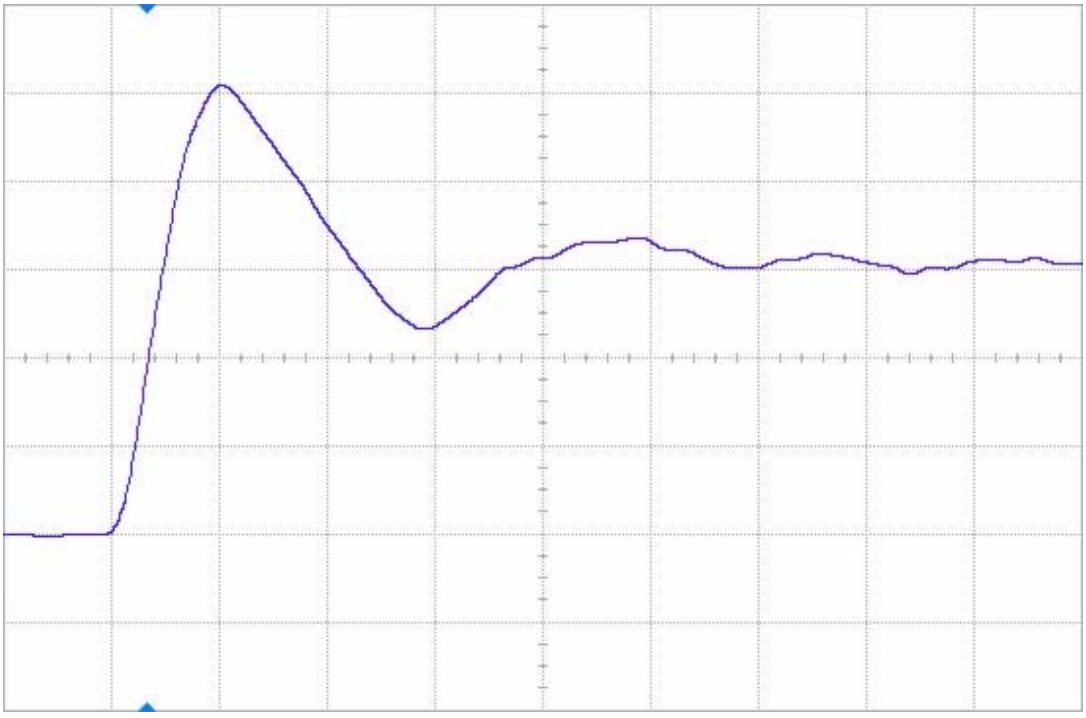

Figure 13(b) DUT 4789 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

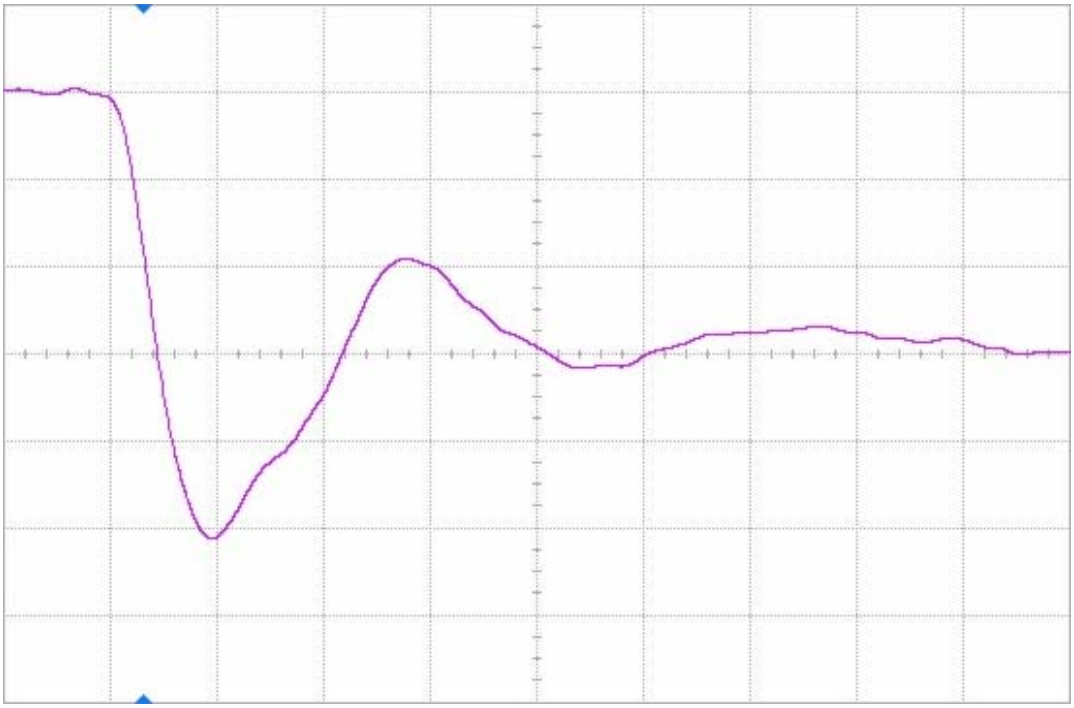

Figure 14(a) DUT 4750 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

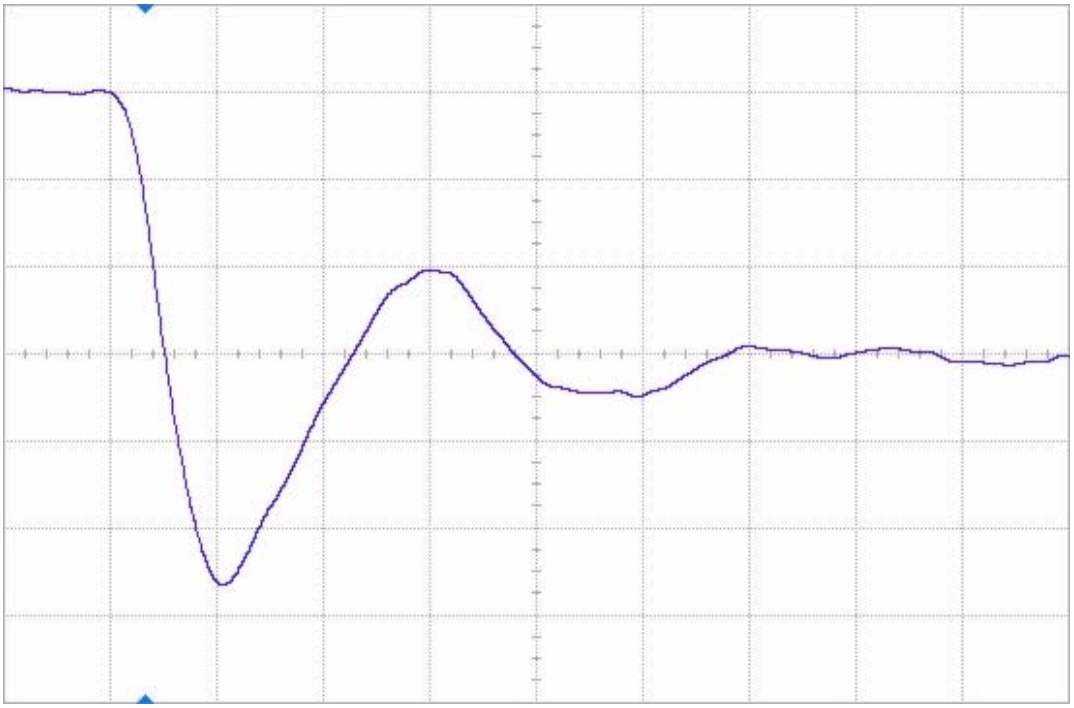

Figure 14(b) DUT 4750 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

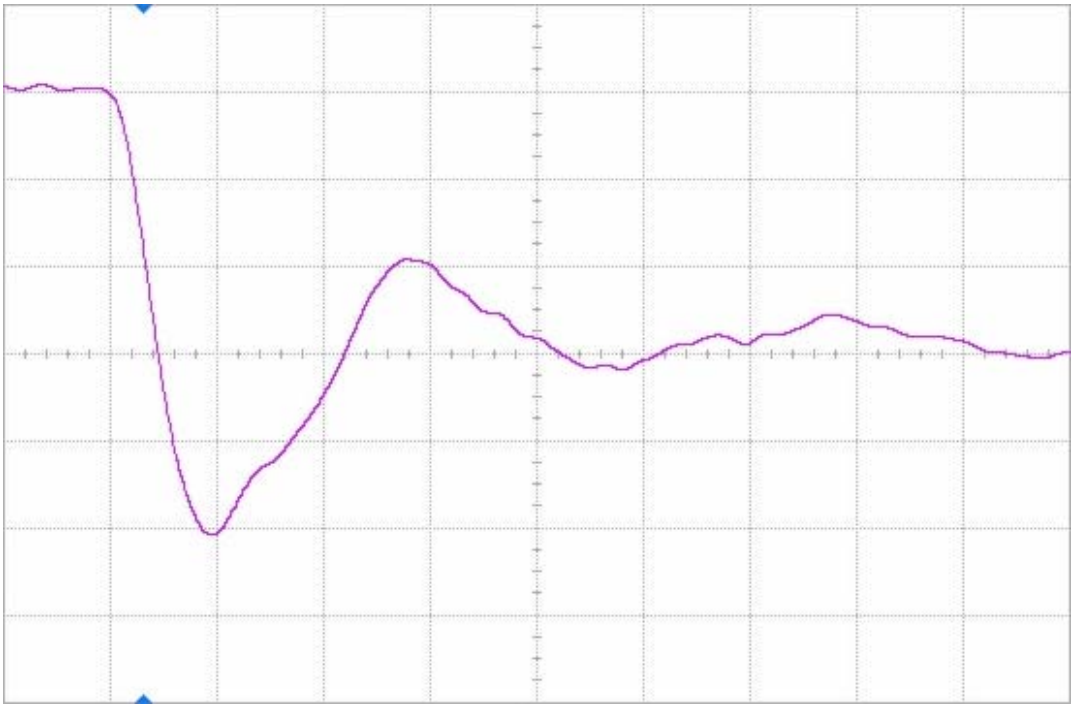

Figure 15(a) DUT 4755 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

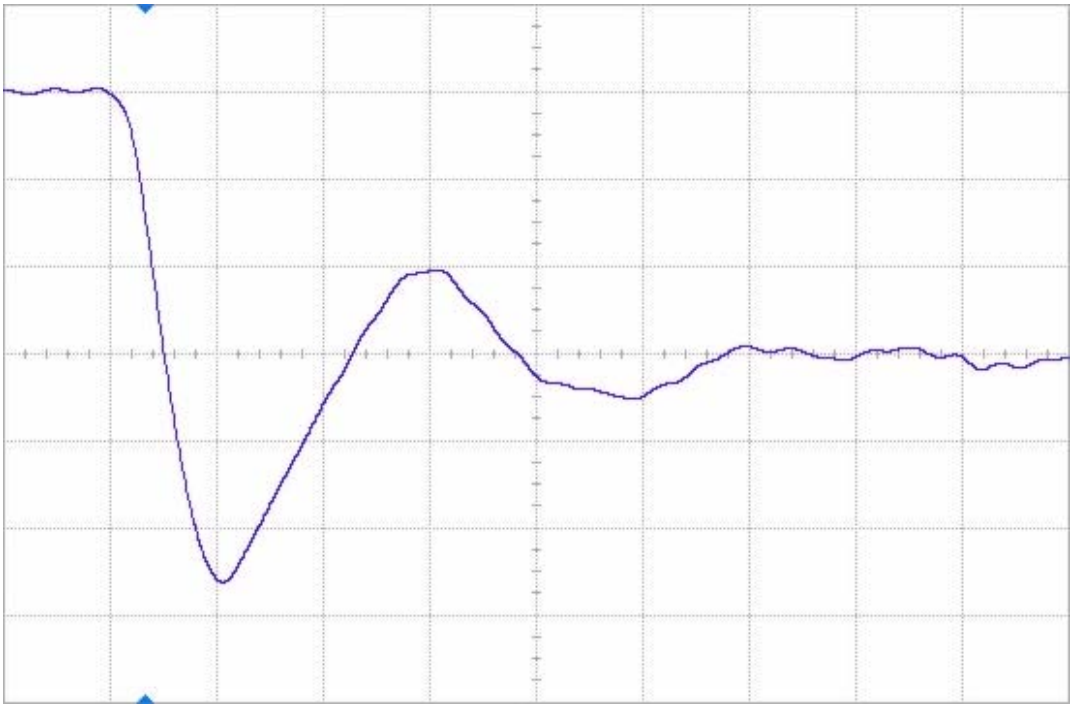

Figure 15(b) DUT 4755 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

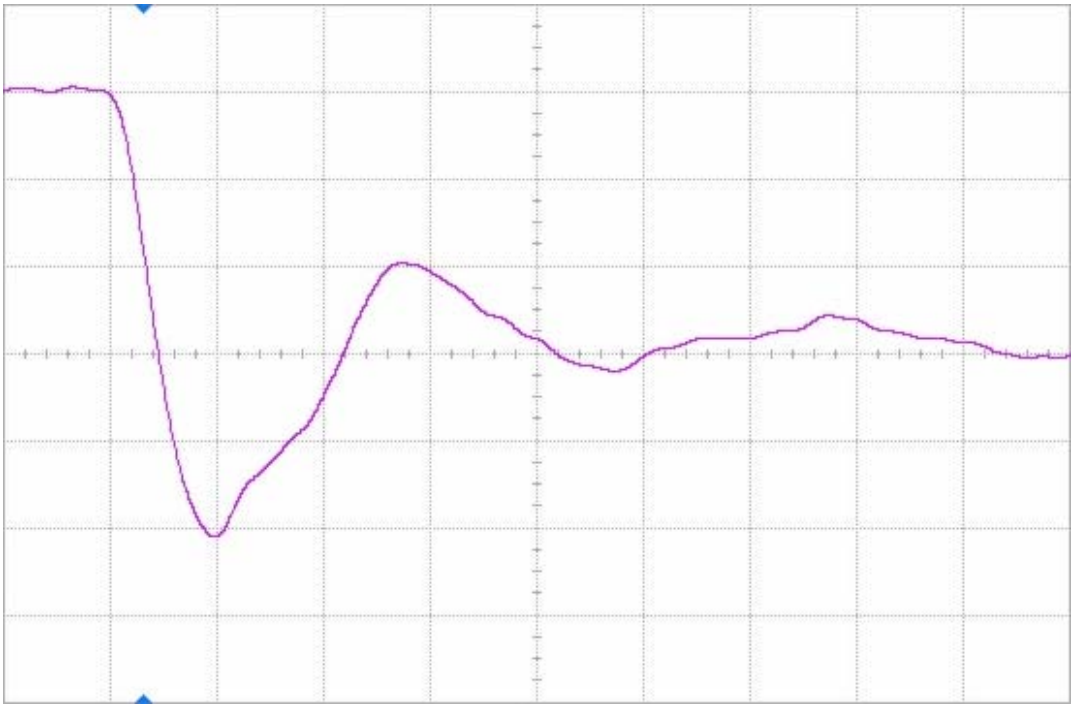

Figure 16(a) DUT 4766 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

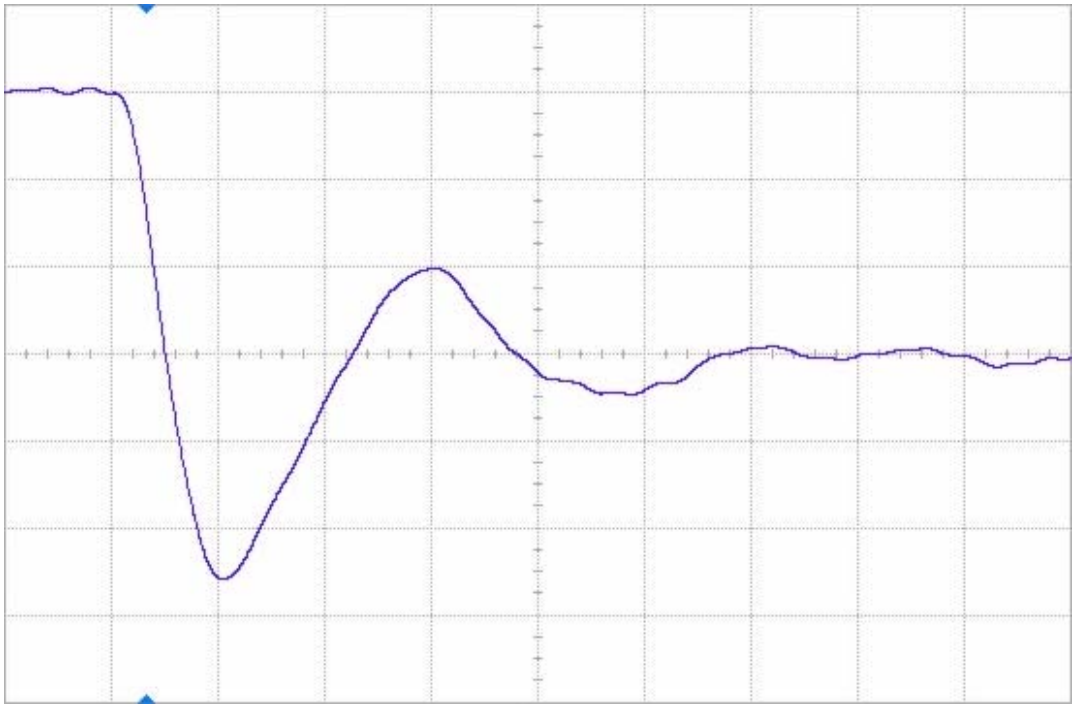

Figure 16(b) DUT 4766 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

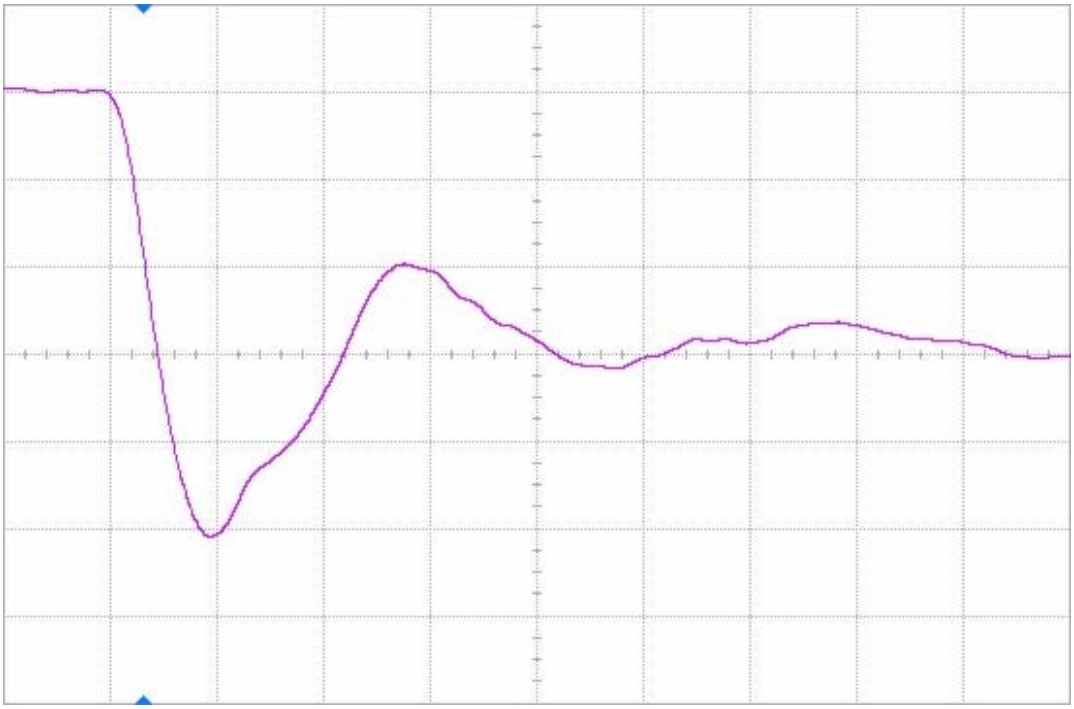

Figure 17(a) DUT 4773 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

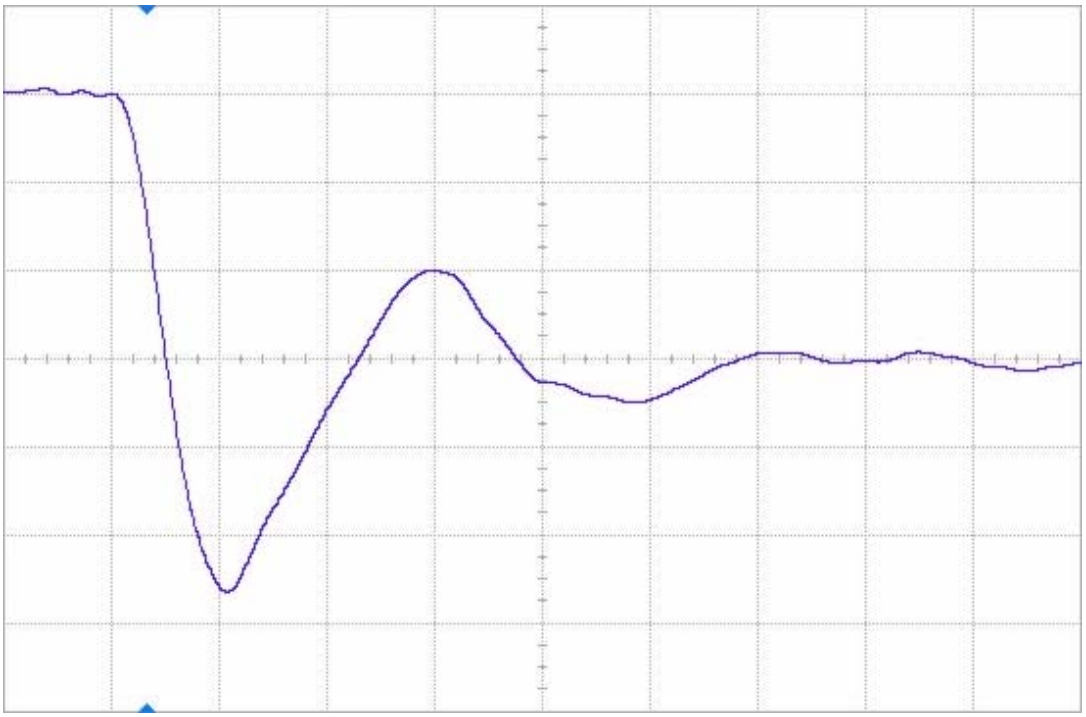

Figure 17(b) DUT 4773 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

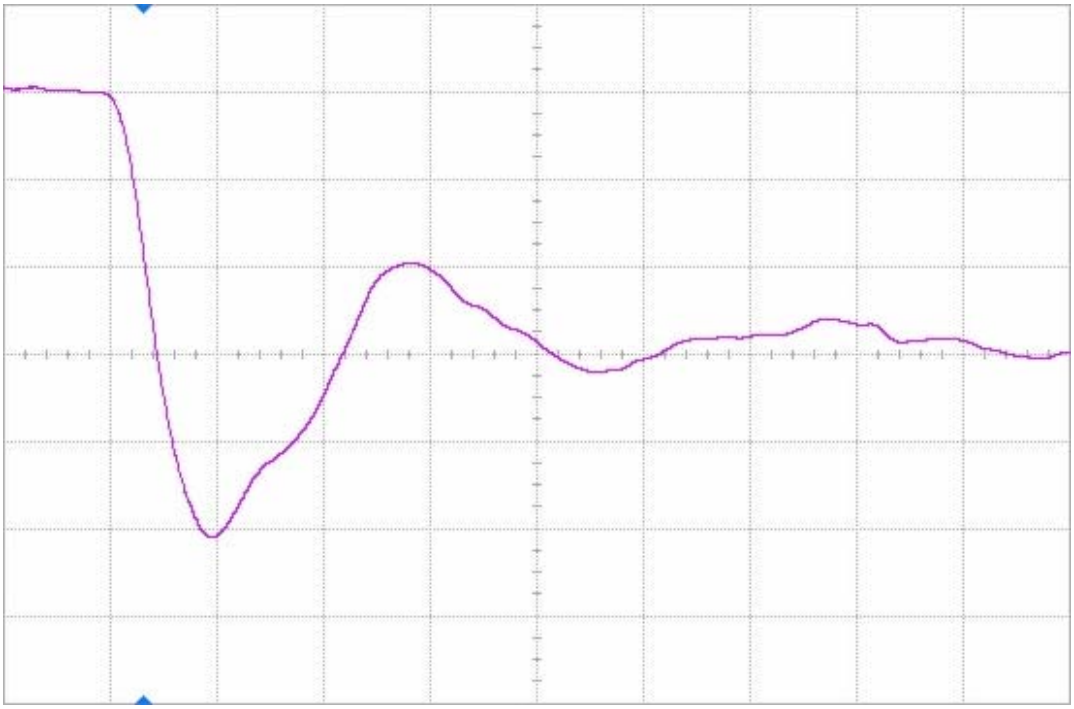

Figure 18(a) DUT 4787 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

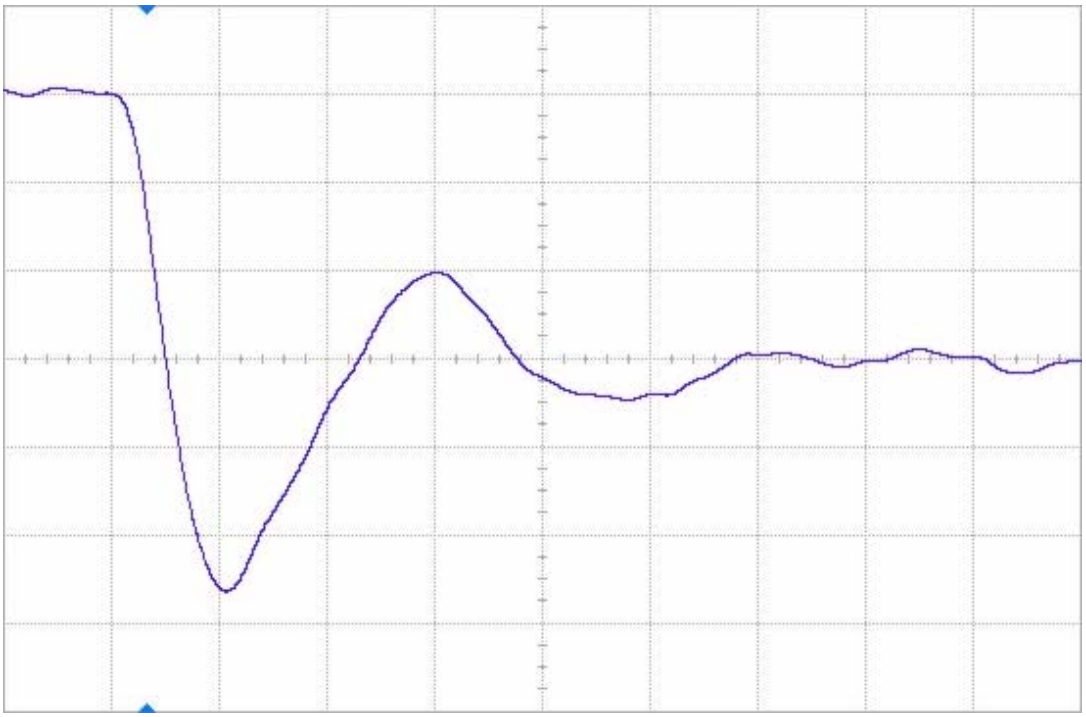

Figure 18(b) DUT 4787 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

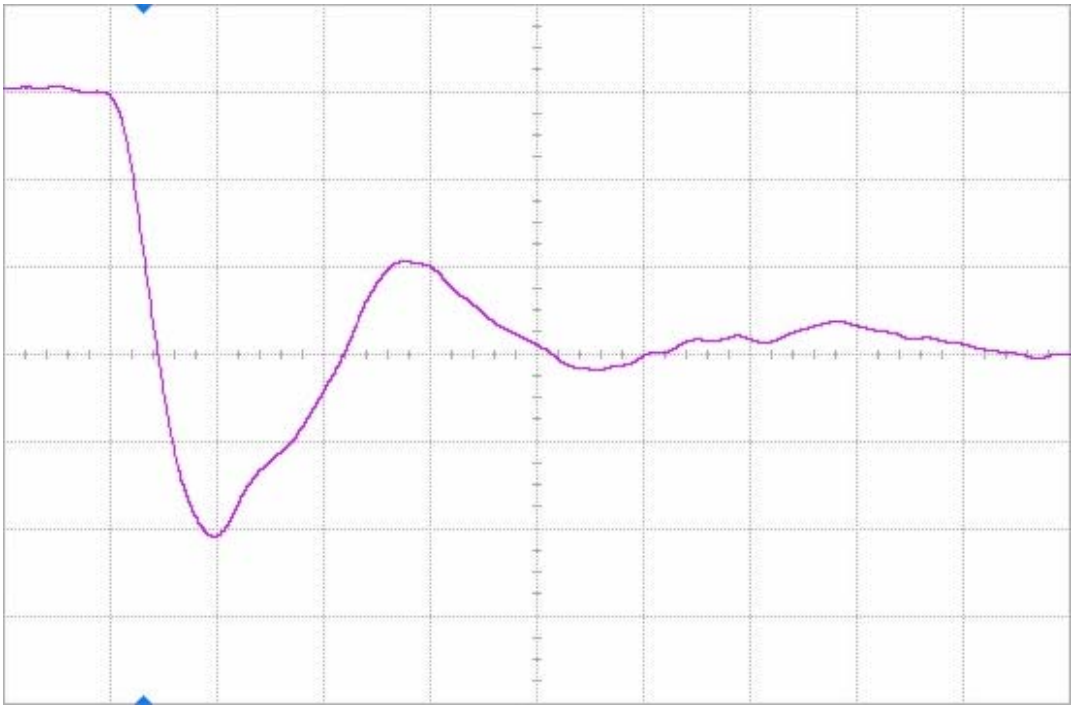

Figure 19(a) DUT 4789 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

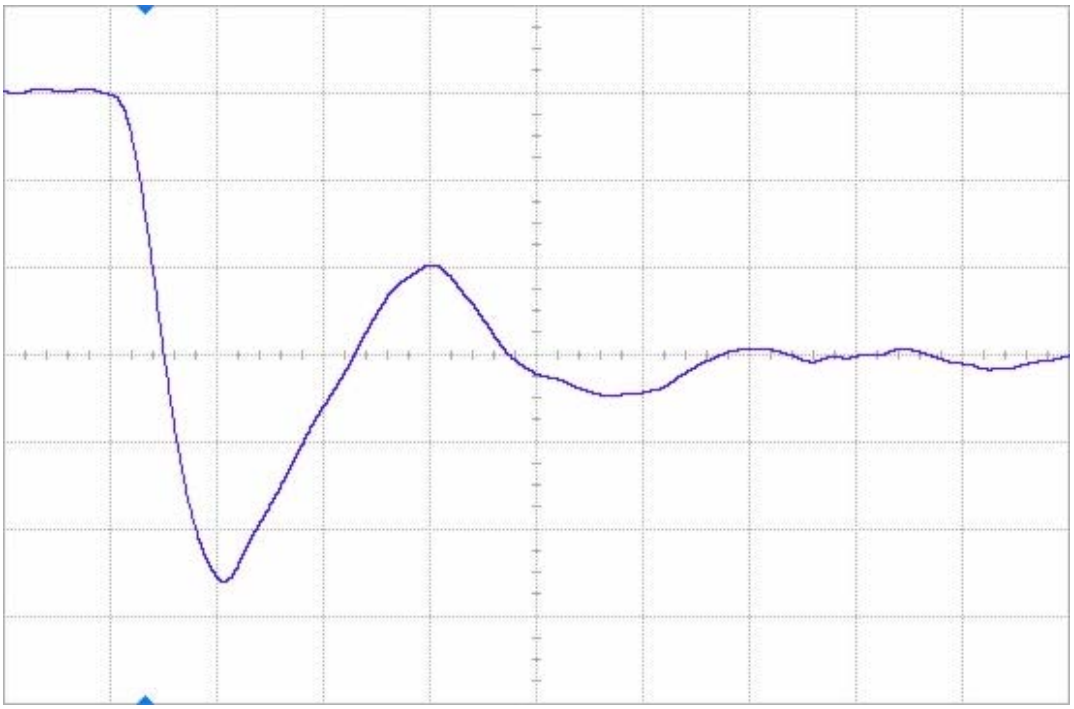

Figure 19(b) DUT 4789 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

APPENDIX A DUT BIAS

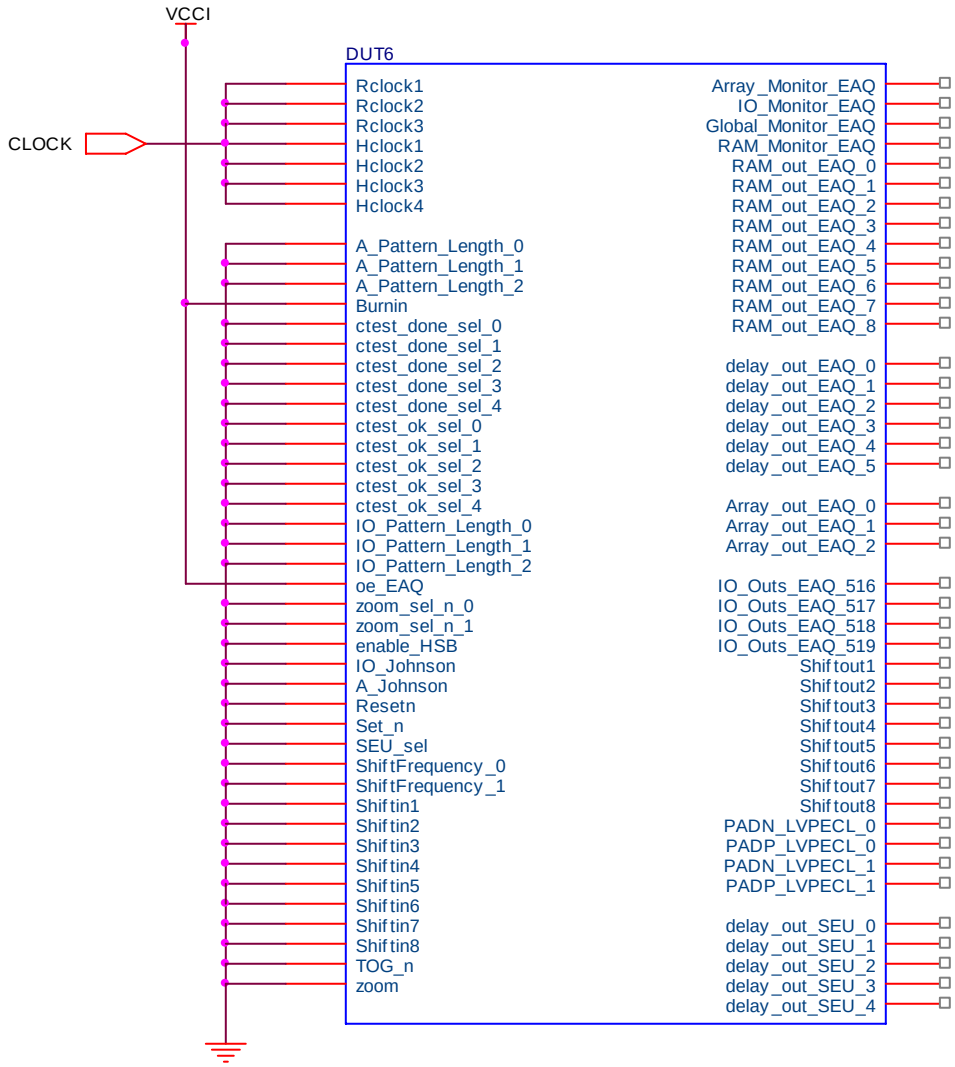

Figure A1 IO bias during irradiation

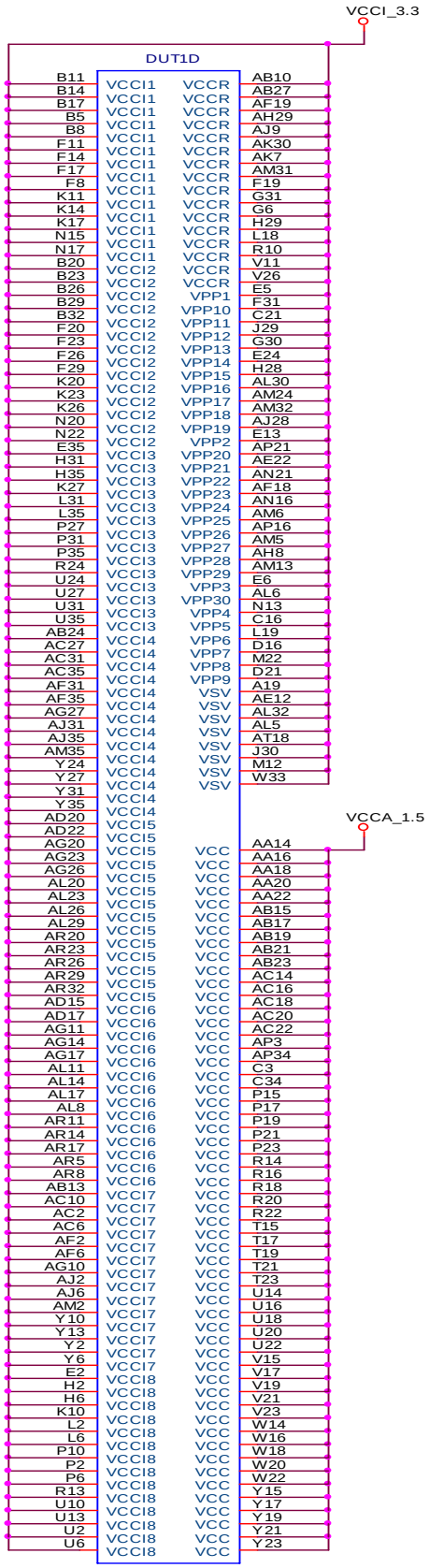

Figure A2 Power supply, ground and special pins bias during irradiation

APPENDIX B FUNCTIONALITY TEST

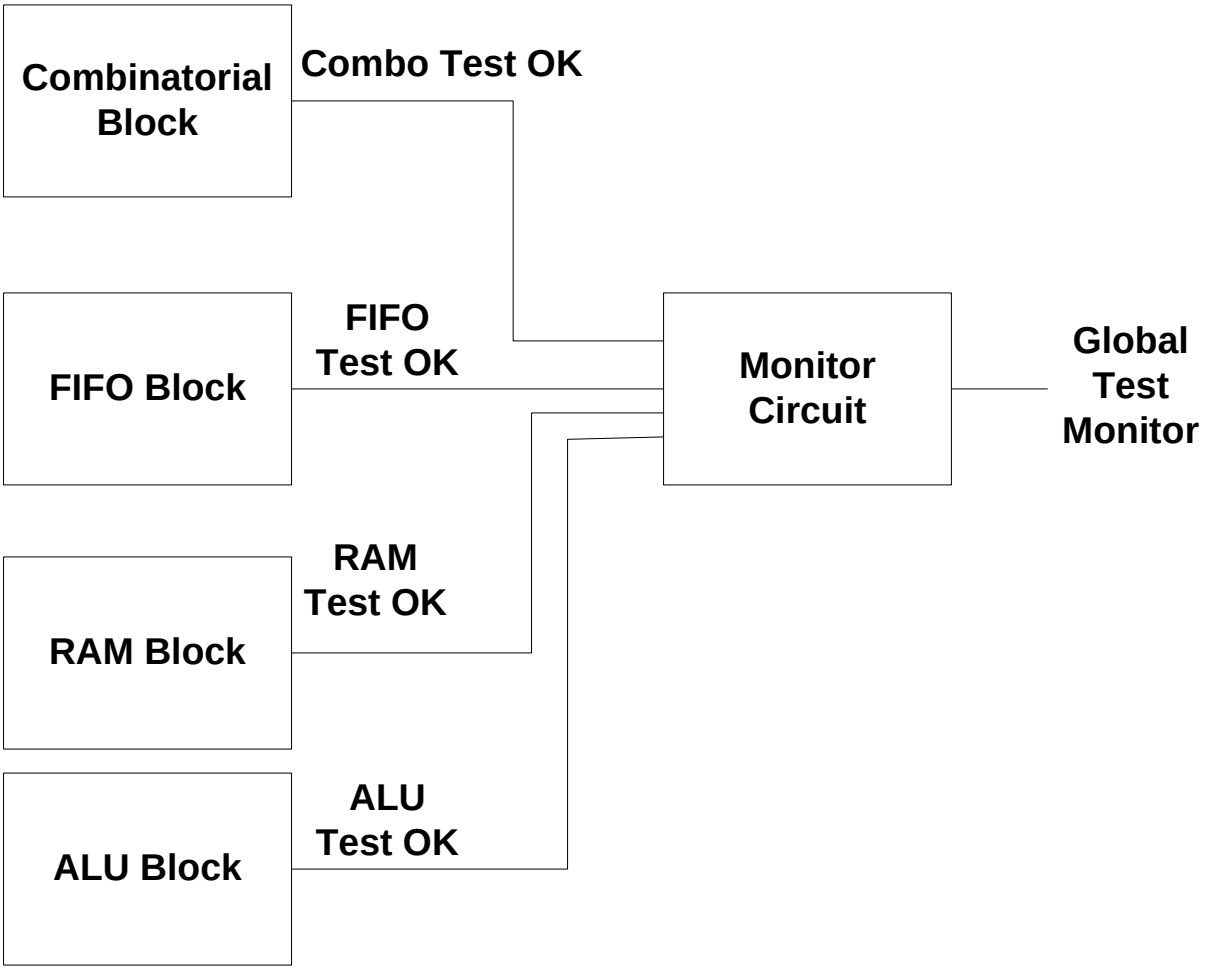

Figure B1 QBI Block – Top level design

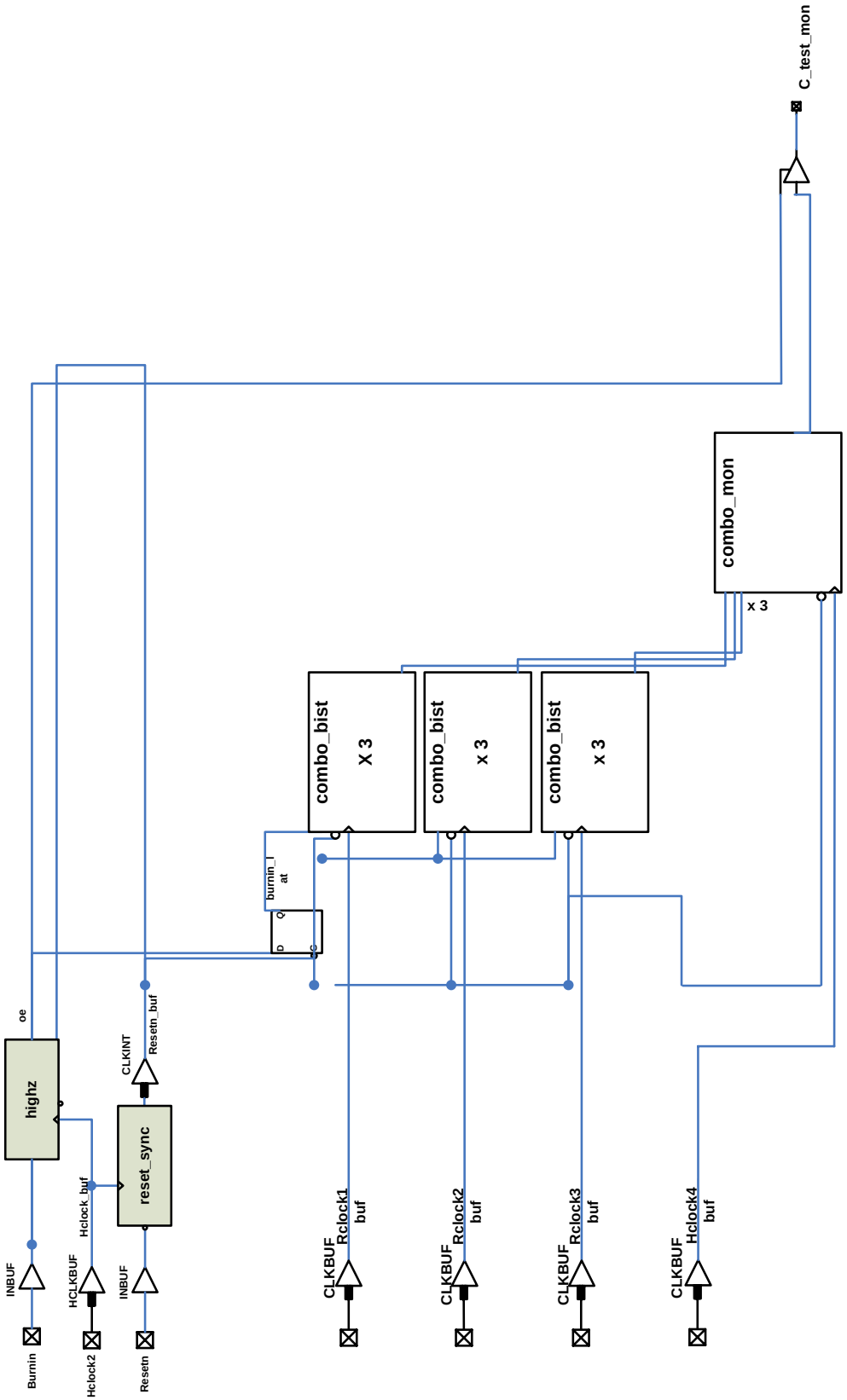

Figure B2 QBI Block – Combinatorial Test (Top Level)

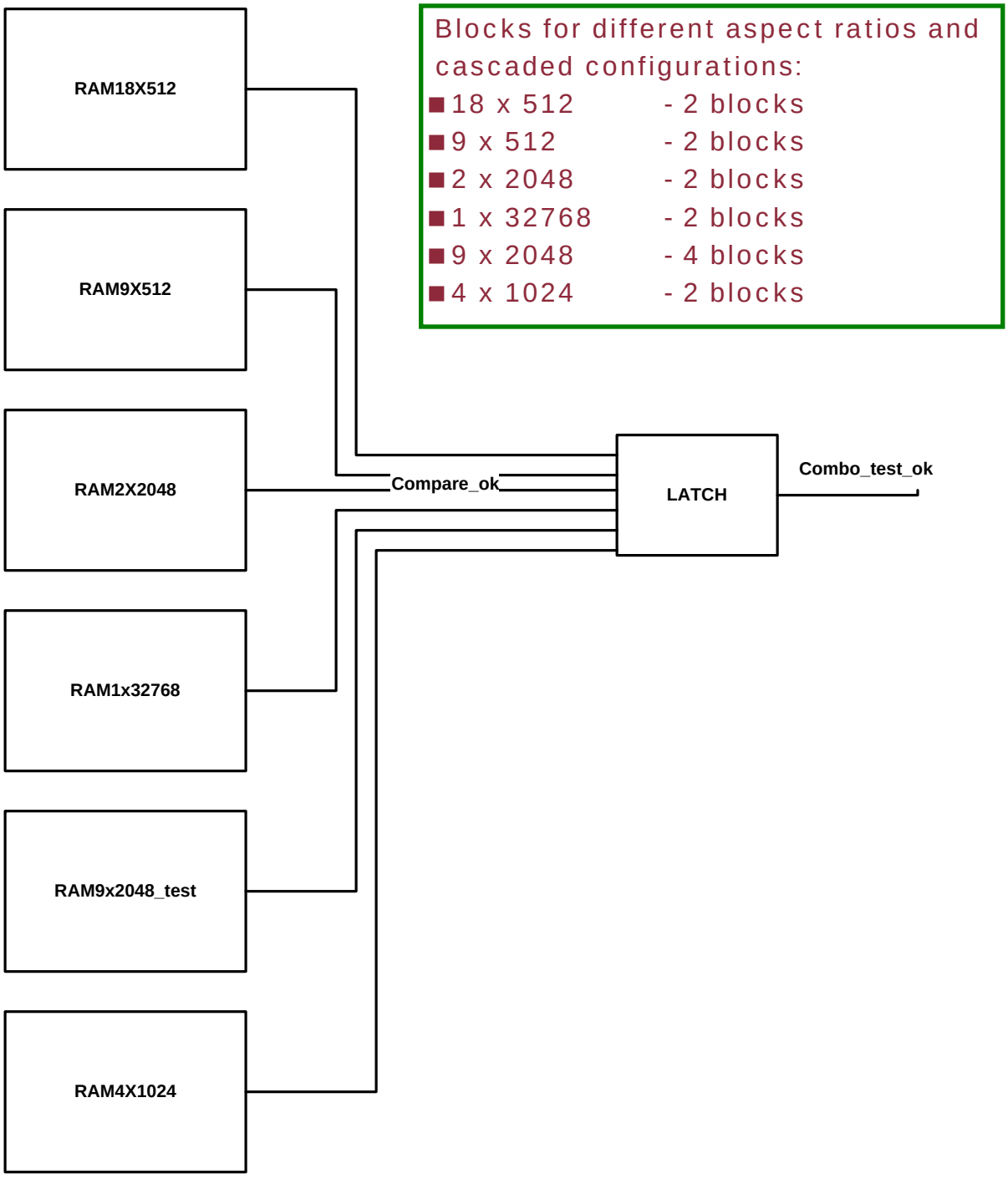

Figure B3 QBI Block – RAM Test (Top Level)

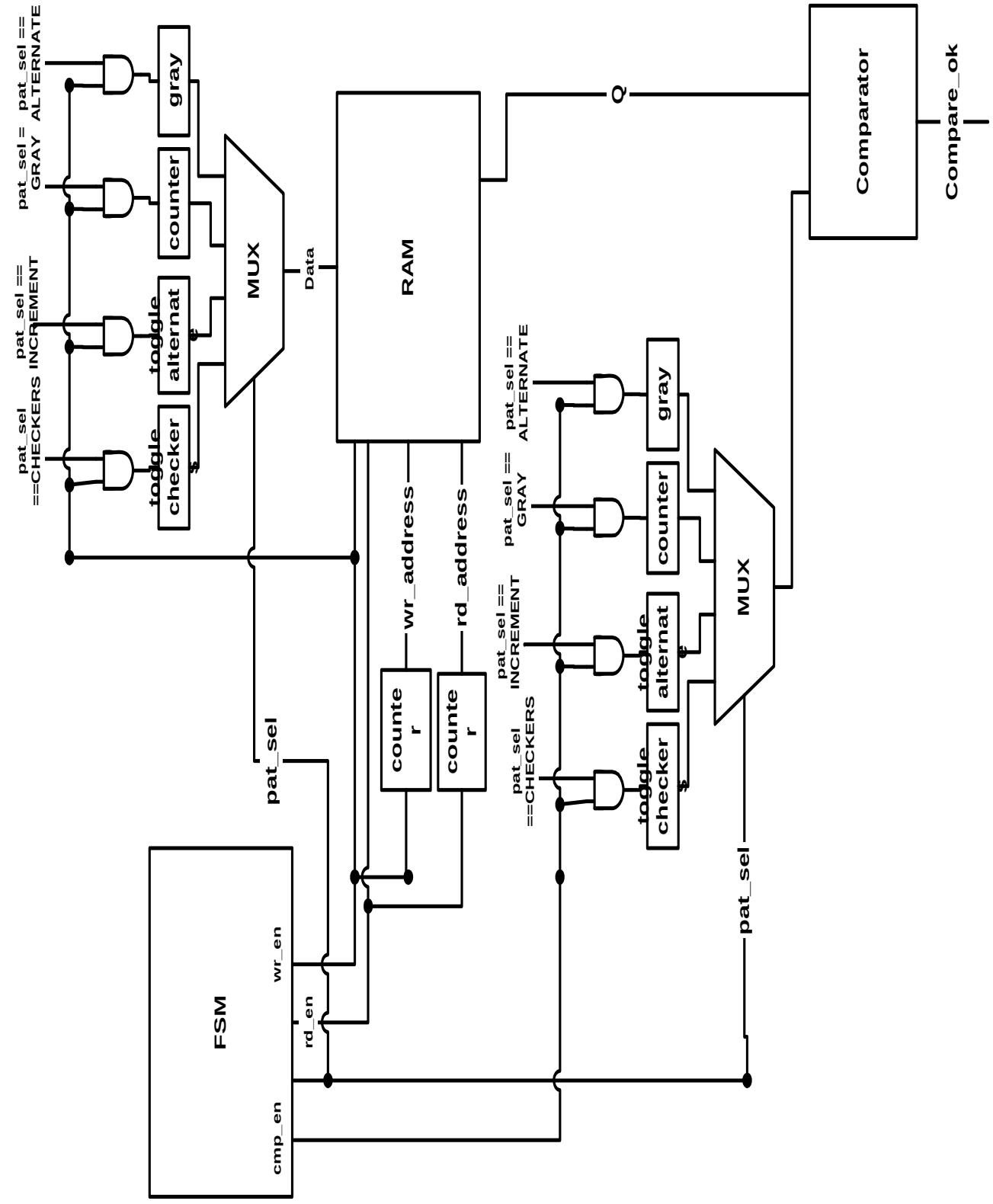

Figure B4 QBI Block – RAM Block

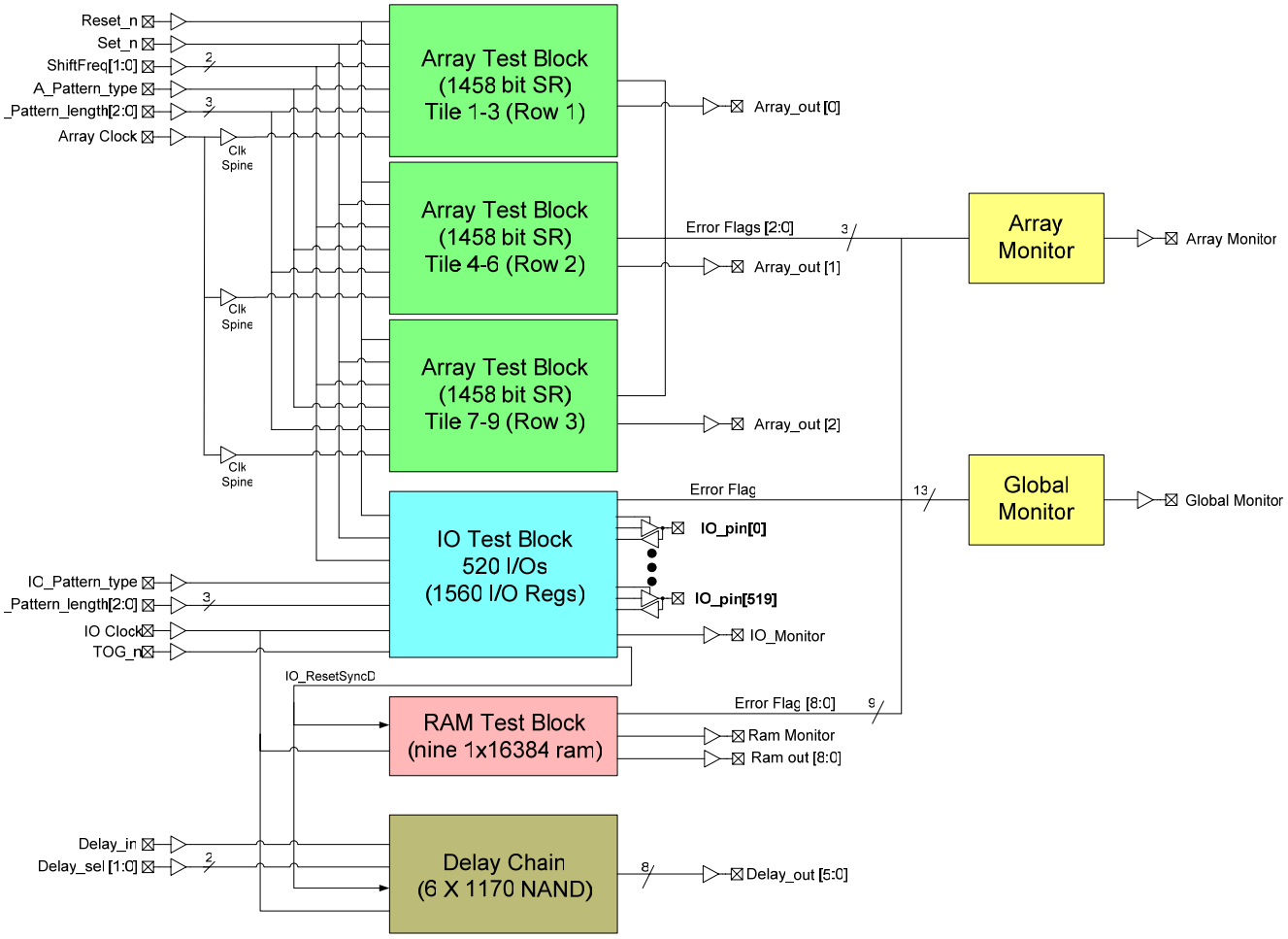

Figure B5 EAQ Block – Top Level

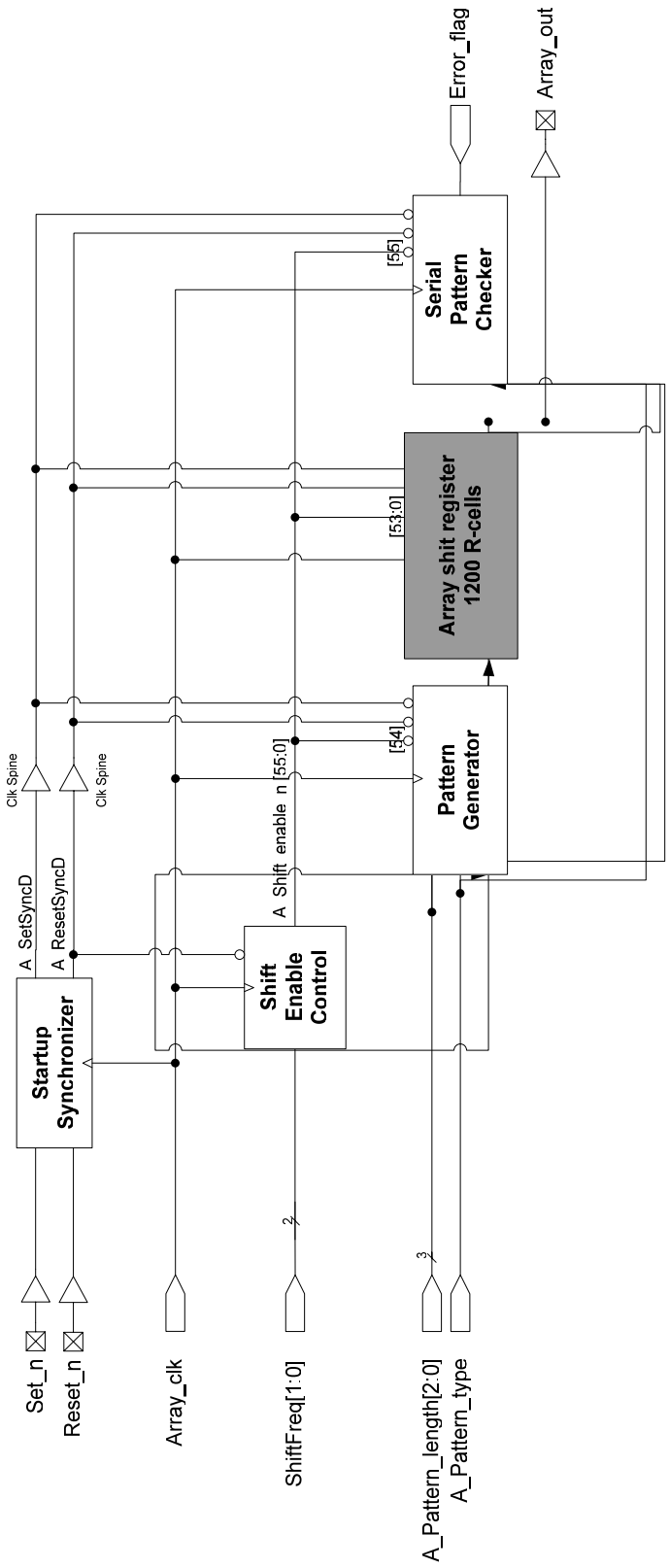

Figure B6 EAQ Block – Array Test (Shift Register)

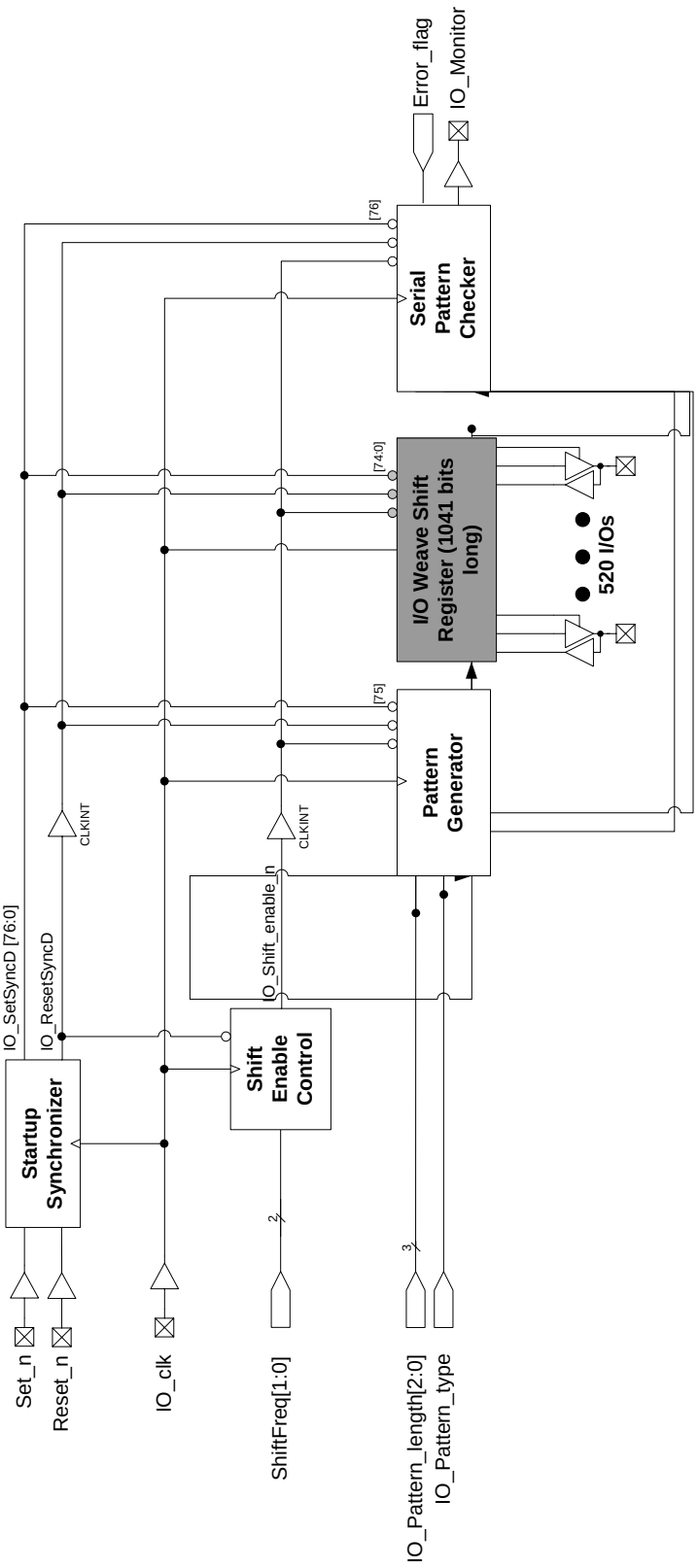

Figure B7 EAQ Block – I/O Test (Top Level)

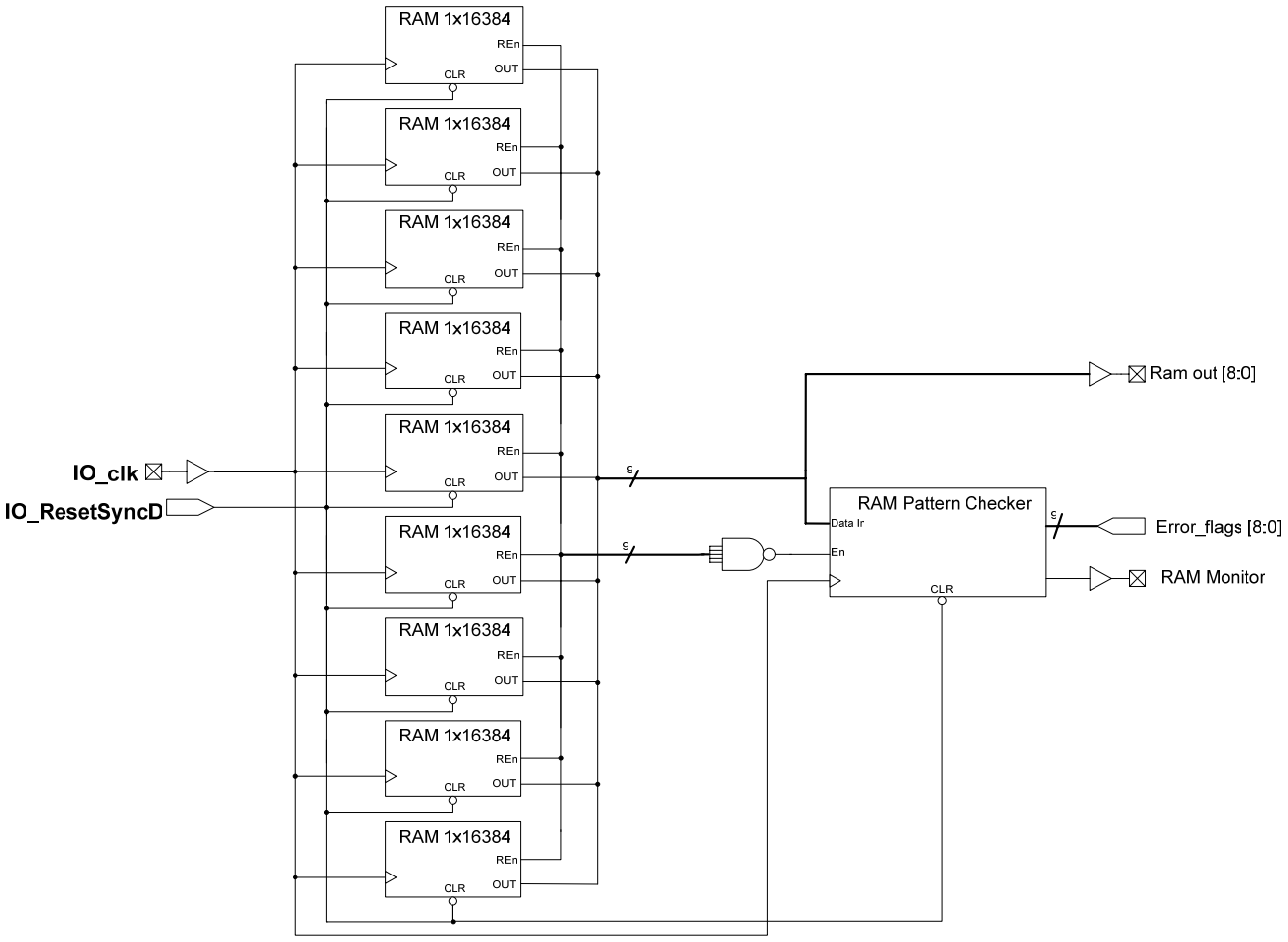

Figure B8 EAQ Block – SRAM Test (Top Level)