PD69104B Based Design of a 4-port Auto Mode System (IEEE802.3af/802.3at Compliant)

APPLICATION NOTE

Introduction

This application note provides detailed information and circuitry design guidelines for the implementation of a 4-port Power over Ethernet Technology consortium system, based on Microsemi's™ 4-channel PoE manager; PD69104B An I^2C or UART interface is available for communication with a hosting system.

This document allows circuitry designers to integrate PoE capabilities, as specified in the IEEE802.3af and IEEE802.3at standards, into an Ethernet switch.

PD69104B, 4 port PoE manager implements real time functions as specified in IEEE 802.3af and IEEE802.3at standards. These include detection, classification and port-status monitoring. Furthermore it implements system level activities such as power management and MIB (Management Information Base) support for system management. The PoE manager is designed to detect and disable disconnected PDs (Powered Devices), using DC disconnection method, as specified in the standard.

Applicable Documents

- IEEE 802.3af-2003 standard, DTE Power via MDI
- IEEE802.3at-2009 standard, DTE Power via MDI
- PD69104B datasheet, catalogue number DS_PD69104B
- PD69104B Reg Map User guide, catalogue number PD69104B-HP_UG_Reg_Map

Background

PD69104B operates in Auto mode, managed by using a Host Control or by using an E^2PROM that configures the system when it turns on.

This application note defines:

- Communication with the Host Controller via an I^2C bus
- PD69104B configuration

Features

- IEEE 802.3af-2003 compliant
- IEEE802.3at-2009 compliant, including two-event classification
- Configurable AT/AF modes
- Single DC voltage input (44-57V)
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Low power dissipation (0.36Ω sense resistor and 0.3Ω internal MOSFET R_{DS_ON})
- Internal power on reset
- Includes Reset command pin
- 4 direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable standard and legacy detection mode
- Power soft start mechanism
- On-chip thermal protection
- Voltage monitoring/protection
- Built in 3.3V and 5V regulators
- Low internal MOSFET R_{DS_ON} of 0.3Ω
- Emergency power management supporting four configurable power bank I/Os
- Can be cascaded to up to 12 PoE devices (48 ports)
- LED Support for every port
- Auto mode for standalone systems
- MAX_LED for indicating max power budget
- I^2C or UART communication
- Power Management
- E^2PROM support
- Wide temperature range: -10°C to +85°C
- RoHS compliant
- 4 Pairs support

Integration

The system can work with up to 48-port switch. Same design can be applied to 1 to 12 PoE managers controlling 4 ports each (from 4 to 48 ports in multiplies of 4).

PoE-system daughter board can be easily integrated on top of a switch and thereby provides the capability to add any PoE application while using a different daughter application.

System Configuration

An **Automode** system with PD69104B can be configured through one of 3 options:

- Host I^2C communication
- E^2PROM configuration
- Hardware configuration (see Figure 1)

Overall Description

Circuit includes the following blocks:

1. PD69104B 4 Ports Auto Mode Circuit. See Figure 1.
2. An Isolation Circuit for I^2C bus. See Figure 2.
3. An E^2PROM to configure PD69104B by I^2C communication. See Figure 1.

General Circuit Description

A 4-port configuration for a PoE Automode system, shown in Figure 1, comprises 1 PoE manager circuit (PD69104B) that functions as slaves to a Host controller. Host controller utilizes the I^2C bus to control PD69104B. "Extended Registers Support" operations are performed automatically by PoE manager circuits, while the PoE Host controller performs power management and other tasks.

Communication Flow

Host CPU issues commands, utilizing a dedicated I^2C Communication Protocol to PD69104B through an isolation component.

This isolation is a basic requirement of IEEE802.3 PoE standards.

Isolation

Used isolation circuitry comprises opto-coupler and digital isolator destined to provide $1500V_{rms}$ isolation required by standards (IEEE802.3af/IEEE802.3at) See Figure 2.
Following are Isolation signals that cross over the isolation circuitry:

- I^2C (SDA,SCL)
- Reset (xPoE_RESET)
- Interrupt (nINT See Figure 3)

Isolation voltage parameters from host side:

- $V_{IH} > 1.6V$
- $V_{IL} < 0.4V$
- $V_{OH} > 3V$
- $V_{OL} < 0.2V$

Main Supply

PoE system operates within a supply range of 44V to 57V (802.3at high power port's supply range is 50 to 57V). To comply with UL SELV regulations, maximum output voltage should not exceed 60V. System Power supply should supply power for 4 ports.
Each port can consume up to 40W, 720mA depending on the current set (see Table 4 line 33)

Grounds

Several grounds are utilized in the system:

- Analog
- Digital
- Chassis
- Floating

Digital and analog grounds are electrically same ground. However, to reduce noise coupling, grounds are physically separated and connected only at a single point U3 @ Figure 1.

Chassis ground is connected to switch's chassis ground. This ground plane should be $1500V_{rms}$ isolated from PoE circuitry.

Floating ground is actually controller's digital ground.

3.3V Regulator

The PD69104B comprises a built in regulator used for the PD69104B internal circuitry and PoE domain side isolation circuit. The host (switch domain) should provide 3.3V/5mA ($2.7V \le V_{DD1} \le 3.6$) to the host domain side of the isolation circuit.

Detailed Circuit Description

The following sections describe the overall block diagram of a PD69104B (refer to Figure 1).

Communication Interfaces

Interface between Ethernet switch and PoE ICs is a $1500V_{rms}$ isolation I^2C interface. Note that each side of the circuitry is fed by a separate power supply. Isolation circuit is detailed in Figure 2 .

Control and Indication Signals

Control/Indication signals are of single H/W lines type that runs between Host controller and PoE manager. These signals are isolated to achieve $1500V_{rms}$ isolation (Refer to Figure 2 & Figure 3).

- nINT: When this pin is configured to work as an interrupt pin, a signal generating by the PoE manager indicates events such as Port On, Port Off, Port Fault, PoE Manager Fault, Voltage Out of Range, etc. nINT pin output voltage shall be >3V with a 10KΩ external pull-up resistor to 3.3V. If not utilizing as

nINt, the pin functions as a CAP or RES detection configuration pin as explained in Table 4 line 36

- xPoE_RESET signal generate by the Host, resets all PoE managers throw an isolation reset line See Figure 2. All PoE managers reset input lines should be connected together with a pull-up resistor.

Reference Current Source

Reference for internal voltages within the PoE manager is set by a precision resistor of 30.1KΩ (R15). See Figure 1.

I²C Interface

Host controller can communicate with PoE managers using I²C communication.

I²C communication between Host CPU and PD69104B is managed by setting the address of the ICs. This is done by selecting add0-add3 pins which can be connect to 3.3V or GND.

These pins set I²C address as shown in Figure 1.

Ground Interface Connection (AGND)

Power Supplies Ground connector enables the current path back to power supply.

Ground connection should be capable of carrying all strings current back to power supplies.

Thermal Design

Design for IEEE802.3at PoE standard should take into account power dissipation of PoE manager, associated circuitry and maximum ambient operating temperature of the switch. Adequate ventilation and airflow should be part of the design so as to avoid thermal over-stress on components detailed below.

Ambient Temperature

Application's thermal design should take into account temperature derived by the power dissipation of the switch and by PoE daughter board when powered at maximum load.

Current set

When a port is in Auto mode, I_{CUT} and I_{LIM} shall be set automatically after port powers up successfully. Levels for I_{CUT} and I_{LIM} shall depend on:

- Chip hardware configured in pin 33
- E²PROM configured by communication
- Host CPU configuration by communication

See Current set description for full parameters (Table 4 line 33).

E²PROM

When PD69104B is configured to work with E²PROM, pin 34 (COMM_MODE) should be open. E²PROM (U1 at Figure 1) communicates with PoE manager by dedicated I²C lines (pins 42 43) as shown in Figure 1. In multi PoE managers system each one should have its own E²PROM.
(Note for EVB - When E²PROM is needed to be programmed, R6 and R7 should be removed in order to allow the programmer to communicate with the E²PROM and not to the PoE manager).

LED indication

- When PD69104B turns one of its ports on, the LED of this port is activated (pins 7,8,29,30).
- MAX_LED analog output indication that consumption is below Power Guard Band determined by the user

Output Protection

F1-F4 is a current limiting device, operating as specified in the IEC 60950-1:2001 requirements.

The fuse is not required in case power supply is lower than 100W.

4 Pairs

PD69104B can be configured to work in a 4-pairs mode, which means ports 1&2 or ports 3&4 are synchronized to be turned on together when PD 4 pairs is connected.

In order to work in a 4 pairs mode, pin 32 (4_pairs) should be connected to VCC or open as explained in Table 4 row 32.

The second port of each pair is the master and the first one in the slave, (port 1 and 3 are masters, port 0 and 2 are slaves)

When working in mode half IC 4 pair and half is 2 pairs ,the first 2 ports are working as 4 pairs (port0 & port1) and ports 2&3 working as normal 2 pair ports.

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Table 1: LED Indication

PIN	Status	LED
LED<3:0>	Port Power On	On
	Power Management event	0.4Hz Blink
	Port Over Load Port Short Circuit Port failed at Startup	0.8Hz Blink
	V_{main} Out of Range or Over Temp	All LEDs :3.3Hz Blink
	Port Off	Off
	4 Pairs on	2 Leds On
	4 Pairs off	2 Leds Bilnks
MAX_LED	Total power consumption is below Power Guard Band determined by the user	Off
	Total power consumption is above Power Guard Band but below total budget.	On
	Total power consumption is above total budget, or Power Integral is still positive	Blink

Bill of Materials for PoE System

Table 2: Main Components

Block	QTY	Reference	Description	PCB Footprint	Manufacturer	Manufacturer's Part Number
Main	2	C2,C3	CAP CRM 4.7uF 10V 10%^^X7R 0805 SMT	PD -0805	Taiyo Yuden	LMK212B7475KG-T
	1	C4	CAP CRM 47nF 100V 10%++X7R 0805 SMT	PD-0805	Murata	GRM40X7R473K100
	4	C6,C7,C24,C25	CAP CER 0.1uF 10V X7R 10% ^^0402 SMT	PD-0402	Walsin	0402B104K100CT
	1	C9	CAP CRM 47nF 100V 10%^^X7R 0805 SMT	PD-0805	Novacap	0805B473K101CTM
	1	C19	CAP ALU 22uF 100V 20% 105C 8X10.2 2000Hr	D8H10_2F9P3_2-SMD	Sanyo	100CE22FS
	4	C20,C21,C22,C23	CAP CRM 47nF 100V 10%^^X7R 0805 SMT	PD-0805	Vishay	VJ0805Y473KXBAT
	6	D1,D15,D16,D17,D18,D19	LED SuperYelGrn 100-130o 20-40mcd h=1 0603 SMD	led-0603-a	Everlight	19-21-SYGCS530E3TR8
	4	D2,D3,D4,D5	DIO RECOV. REC 400V 1A++SMA SILICON SMT	PD-SMA	Diodes Inc.	S1G
	4	F1,F2,F3,F4	FUSE 1.5A 63V V. FST BLO++1206 SMT	PD-1206	AVX	F1206B1R50FW-TR
	1	JP1	Header Shrouded 2X5pin^^Vertical Voided Pins Tin	MOL-10P-2R-90130-21	Molex	90130-2114
	1	J1	CON DC POWER JACK RA^^2.0X6.3 T/H	SWITCHCRAFT-RAPC722	Switchcraft	RAPC722-TB13
	4	R1,R9,R12,R14	RES TCK FLM 10K 1% 62.5mW ^^0402 SMT	PD-0402	Vishay	CRCW0402-1002F RT7
	3	R5,R6,R7	Resistor, 0 Ohm, 5%, 1/16W 0402	PD-0402	ASJ	CR10-000ZK
	3	R8,R11,R13	Resistor, 0 Ohm, 5%, 1/16W 0402	PD-0402	ASJ	CR10-000ZK
	6	R10,R18,R29,R30,R31,R32	RES TK FLM 51.1K 125mW^^1% 0805	PD-0805	Yageo	RC0805FR-0751K1L
	1	R15	RES TCK FLM 30.1K 1% 62.5mW ^0402 SMT	PD-0402	Panasonic	ERJ2RKF3012X
	4	R25,R26,R27,R28	RES TCK FLM 0.360R 1% 0.5W 200PPM^1210 SMT	PD-1210	Rohm	MCR25JZHFLR360
	1	U3	Ori, 4 Ports PSE IC Auto mode	PD-QFN48-8x8-1	Microsemi	PD69104AILQ
	1	U4	IC MEM E^2PROM 2WIRE 2K^^256X8 TSSOP8 SMT	PD-TSSOP8	Atmel	AT24C02-10TU-2.7
	1	U1	IC Dig.Iso	PD- SOW16	Analog Devices	AD80273ARWZ RL**

**Special part number for Microsemi PoE application; preferential pricing for Microsemi customers.

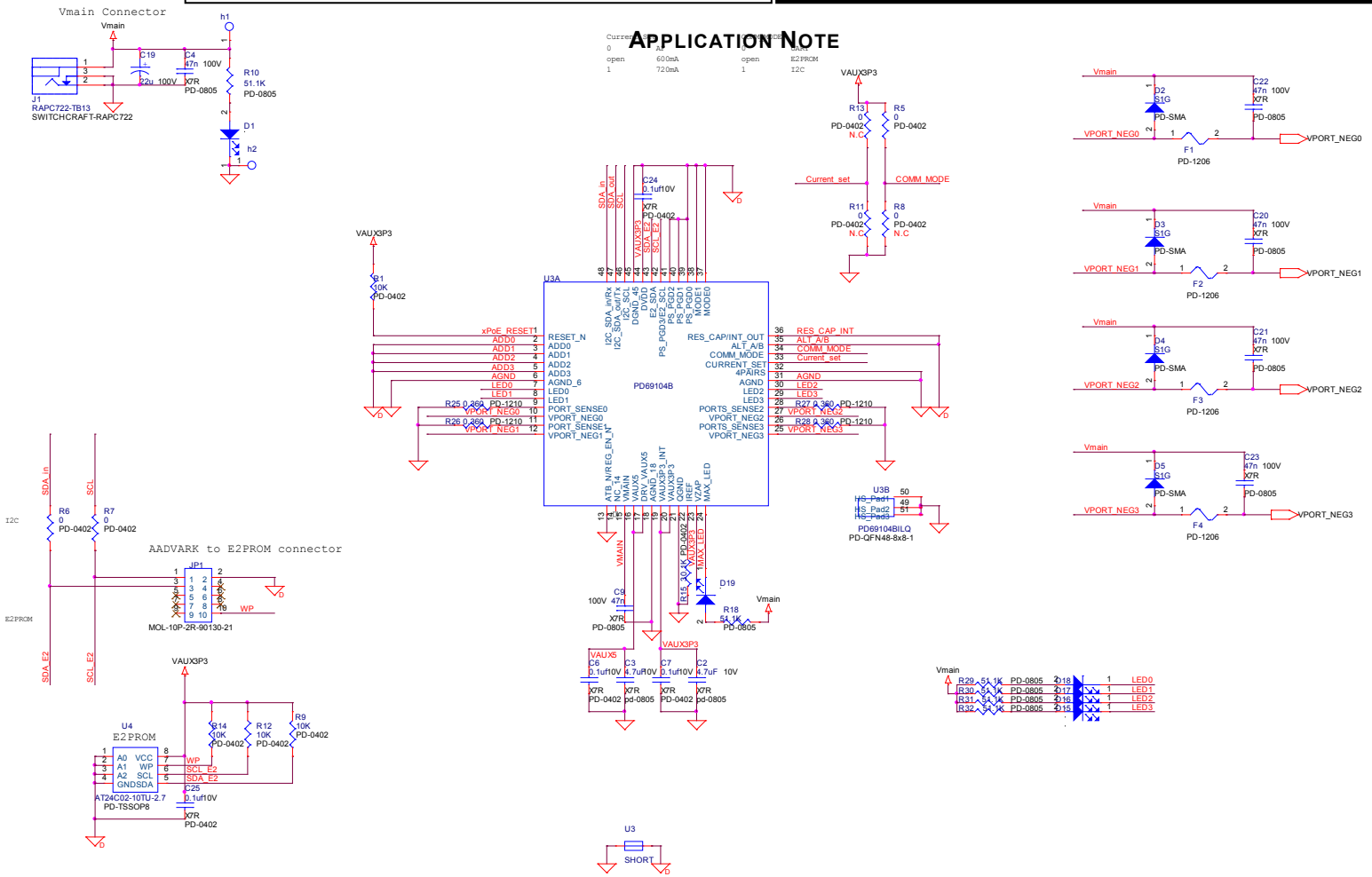

Figure 1: 4 Ports Auto Mode Circuit

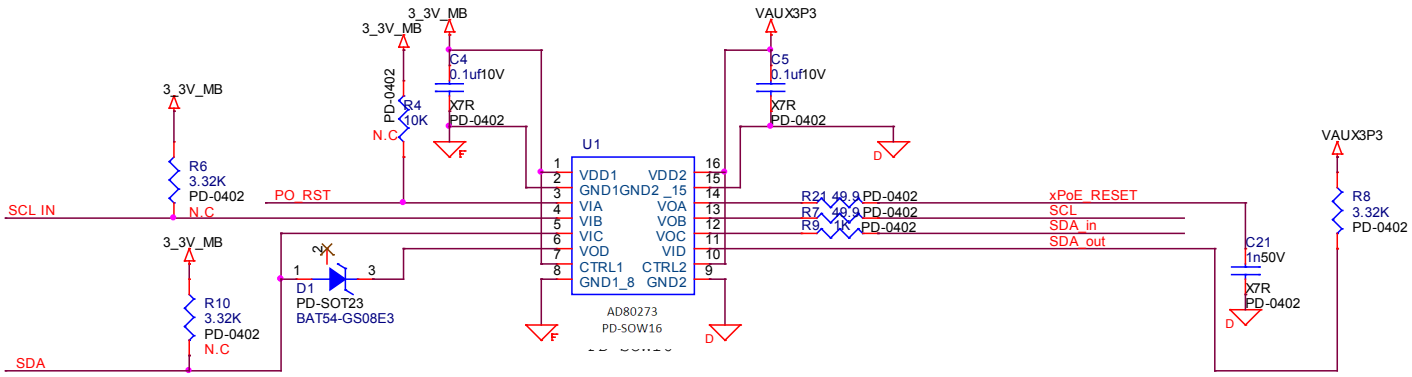

Figure 2: I²C and reset isolation

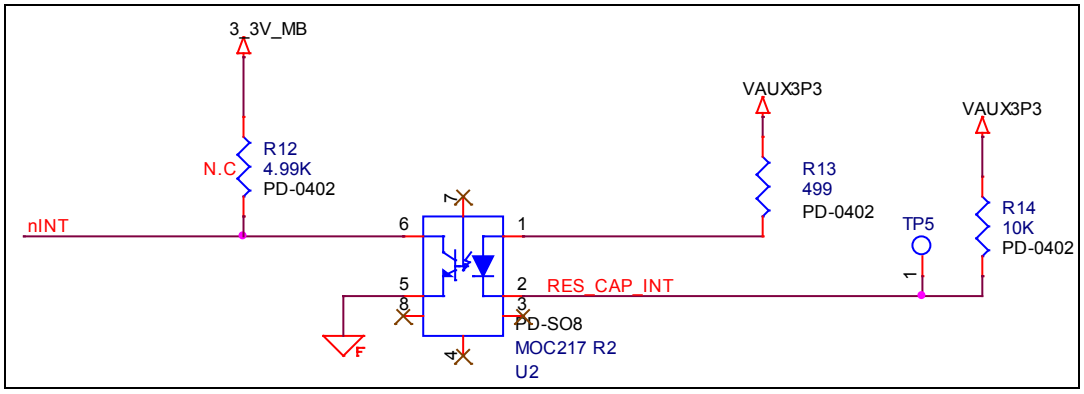

Figure 3: Interrupt Isolation Circuitry

Table 3: MODE of Operation

Mode 1 Pin38	Mode 0 Pin37	Mode	Comm. to the IC	Functionality	Remarks
0	0	MSCC Extended Auto Mode	I²C or UART (see COMM_MODE pin)	fully autonomous operation without a host with Extended Registers Map support Default: No interrupt (can be enabled by communication)	I²C or UART Protocol to Host with extended register map and PM support
0	1	Semi Auto mode	I²C or UART (see COMM_MODE pin)	Host should manage the ports	I²C Protocol to Host
1	0	Test mode			For internal use only
1	1	Auto mode	I²C or UART (see COMM_MODE pin)	fully autonomous operation without a host controller with interrupt out support	I²C Protocol to Host

Table 4: PD69104B PIN Description

PIN	PIN NAME	PIN TYPE	DESCRIPTION
0.	PAD	Gnd	Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin whenever possible (refer to PD69104B Layout Design Guidelines)
1.	RESET_N	Digital Input	Reset input – active low ('0' = reset)
2.	ADDR0	Digital Input	Address bus to set chip address
3.	ADDR1	Digital Input	Address bus to set chip address
4.	ADDR2	Digital Input	Address bus to set chip address
5.	ADDR3	Digital Input	Address bus to set chip address
6.	AGND	Power	Analog ground
7.	LED0	Analog output	Port 0 LED indication – Active low ('0' - LED on)
8.	LED1	Analog output	Port 1 LED indication – Active low ('0' - LED on)
9.	PORT_SENSE0	Analog Input	Sense resistor port input
10.	VPORT_NEG0	Analog I/O	Negative port output
11.	PORT_SENSE1	Analog Input	Sense resistor port input
12.	VPORT_NEG1	Analog I/O	Negative port output
13.	REG_EN_N	Analog I/O	An input pin that enables control of the $3.3V_{DC}$ internal regulator. Disables internal $3.3V_{DC}$ regulator in case external $3.3V_{DC}$ is used to supply the chip. If connected to GND – internal regulator is enabled. If connected to $3.3V_{DC}$ – internal regulator is disabled
14.	NC	Analog I/O	A test pin used only during production. Keep unconnected.
15.	VMAIN	Power	Main High Voltage Supply voltage. A low ESR 1µF (or higher) bypass capacitor, connected to AGND should be placed as close as possible to this pin through low resistance traces.
16.	VAUX5	Power	Regulated 5V output voltage source; needs to be connected to filtering capacitor (at least 4.7µF).
17.	DRV_VAUX5	Power	Driven output terminals for $5V_{DC}$ external regulations. In case internal regulation is used, connect to pin 16. In case an external NPN is used to regulate the voltage, connect this pin to "Base".
18.	AGND	Power	Analog ground
19.	VAUX3P3_INT	Power	In case internal 3.3 V_{DC} regulator is used, connect to VAX3P3 (pin 20). In case external $3.3V_{DC}$ regulator is used, connect to VAUX5 (pin 16).
20.	VAUX3P3	Power	Regulated 3.3V output voltage source. Connect a 4.7µF capacitor between this pin and AGND.
21.	QGND	Power	Quiet analog ground
22.	IREF	Analog Input	Reference resistor pin. Connect a 30.1 KΩ ±1% resistor to QGND
23.	TRIM	Test Input	Test Input pin; Connect to V_{dd}
24.	MAX_LED	Analog output	MAX LED analog output; Indication that consumption is below Power Guard Band determined by the user
25.	VPORT_NEG3	Analog I/O	Negative port output
26.	PORT_SENSE3	Analog Input	Sense resistor port input
27.	VPORT_NEG2	Analog I/O	Negative port output
28.	PORT_SENSE2	Analog Input	Sense resistor port input
29.	LED3	Analog output	Port 3 LED indication – Active low ('0' - LED on)
30.	LED2	Analog output	Port 2 LED indication – Active low ('0' - LED on)

PIN	PIN NAME	PIN TYPE	DESCRIPTION
31.	AGND	Power	Analog ground
32.	4_Pairs	Analog Input	3 state input pin. - select 4 pairs mode • "0" (GND) - 4 ports of 2 pairs • "open" (N.C) - 2 ports of 2 pair & 1 of 4 pair • "1" (VCC) - 2 ports of 4 pair.
33.	Current_SET	Analog Input	3 state input pin – select output current and AF/AT mode • "0" (GND) – AF mode, • "open" (N.C) – AT 600 mA , • "1" (V_{DD}) – High AT Mode 720mA
34.	COMM_MODE	Analog Input	3 state input pin communication select. • "0" (GND) – UART active, • "open" (N.C) – E^2PROM connected • "1" (V_{DD}) – I^2C active
35.	ALT A/B	Digital Input	User input pin to set chip working mode • "0": ALT B mode (Midspan, Back Off,) • "1": ALT A mode (Endspan / Switch, NO Back off,)
36.	RES_CAP / INT_OUT	Digital I/O	A user input pin to set chip working mode • "1": IEEE802.3af compliant resistor detection only • "0": AF/AT Detection and Legacy (non-standard) line detection When working in extended PoE mode, used as an interrupt out pin, indicating an interrupt event has occurred An external 10K pull-up resistor should be connected between this pin and DVDD.
37.	Mode0	Digital Input	IC operational mode select – See Table 3
38.	Mode1	Digital Input	IC operational mode select – See Table 3
39.	PS_PGD0	Digital input	Power good 0; Power Budget Set pin – for Fast Power Control
40.	PS_PGD1	Digital input	Power good 1; Power Budget Set pin – for Fast Power Control
41.	PS_PGD2	Digital input	Power good 2; Power Budget Set pin – for Fast Power Control
42.	PS_PGD3 / E2_SCL	Digital I/O	PGD3: Power good 3; Power Budget Set pin – for Fast Power Control *Or* E2_SCL: I^2C Clock Out to EPROM
43.	E2 SDL	Digital I/O	E^2PROM I^2C data I/O pin – for Stand Alone Auto Mode systems - Power Up Configuration
44.	DVDD	Power	Digital 3.3V Power input
45.	DGND	Power	Digital GND
46.	I2C SCL	Digital Input	I^2C bus, serial clock input
47.	I2C_SDA_out / Tx	Digital Output	I^2C bus, data output / UART Tx output
48.	I2C_SDA_in / Rx	Digital I/O	I^2C bus, data input / UART Rx input

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 29 Nov 10	-	Initial Release
0.2 / 24 Oct 11		
1.0 / 01 Dec 11	Detailed Circuit Description	Information and a table were added
1.1 / 04 Dec 11		Structural changes
1.2/ 01 Jan 12		PG pins names were changed
1.3/ 11 Jan 12		Res_cap_int pin description with pull up
1.4/ 30 Jan 12		Adding 4 pairs description

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