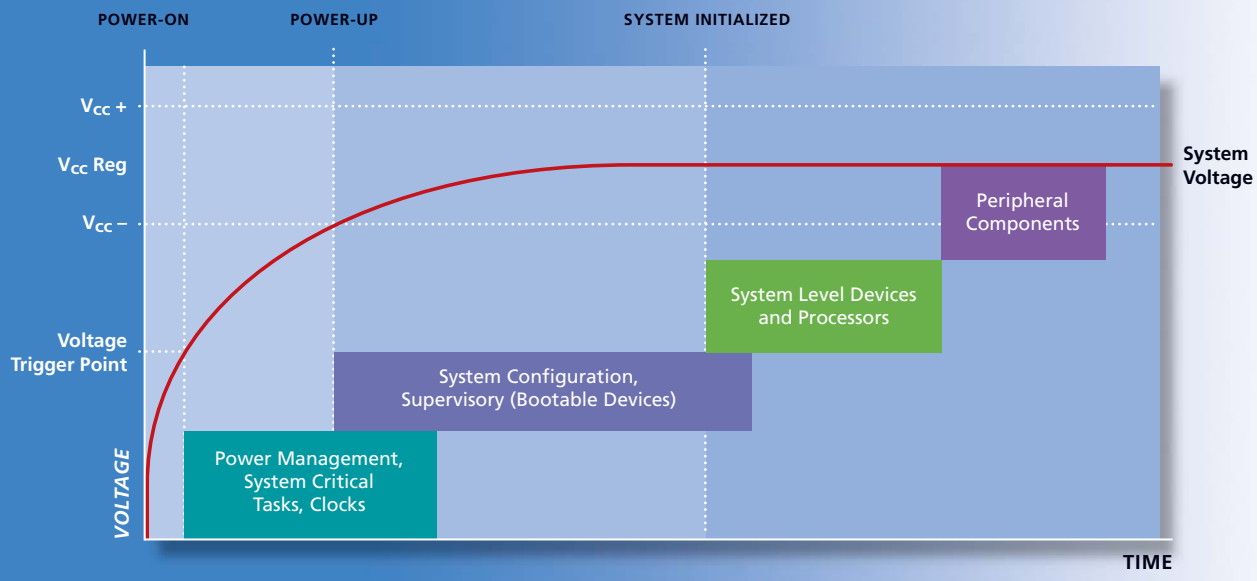
Power-Up Device Classification

Typical system power-up sequence and device operation in each stage with a single "critical" supply voltage



	POWER-ON	POWER-UP	SYSTEM INITIALIZED
Level	0	1	2
Level Description	Live at power-up	Live after power-up	Live after system initialization
Activity	Regulates critical tasks for system environment setup. Provides clocks and critical logic functions during power ramp-up until system is powered up	System configuration and initialization, supervisory, and monitoring tasks. Set up memories and interfaces for microprocessors access	Processor initialization (boot) after environment setup. Periphery component setup least critical to system operation
Device that Can Be Used at this Level	• NVM FPGAs (Flash and antifuse) • Some CPLDs • ASICs • Some ASSPs	• Hybrid CPLDs/FPGAs (SRAM plus NVM) • Some ASSPs	• SRAM-based FPGAs loaded from boot PROM or from microcontroller/processor • Processor