AC396
Application Note
SmartFusion2/IGLOO2 FPGAs in Hot Swapping and Cold Sparing Applications

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 7.0

The document was updated with information about current leakage of the MSIO inputs. For more information, see Cold Sparing, page 6.

1.2 Revision 6.0

The document was updated with information about current drawn at the I/O pins. For more information, see Internal Clamp Diode, page 5.

1.3 Revision 5.0

The following is a summary of the changes made in revision 5.0 of this document.

- Information about cold sparing was updated. For more information, see Cold Sparing, page 6.
- The document was changed to the new template.

1.4 Revision 4.0

Updated I/O Standards for Hot Swapping and Cold Sparing, page 9 (SAR 78476).

1.5 Revision 3.0

Updated Hot Swapping, page 5 (SAR 66982).

1.6 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Updated I/O State During Power-Up and Power-Down, page 2 (SAR 64130).
- Updated Table 1, page 4 and added Table 2, page 5.
- Removed the Driving an Unpowered Device section.
- Updated Hot Swapping, page 5 (SAR 66982).
- Updated Cold Sparing, page 6.

1.7 Revision 1.0

The following is a summary of the changes made in revision 1.0 of this document.

- Updated the Hot Swapping, page 5 for MSIOs and SerDes pins support (SAR53021).
- Updated Table 1, page 4 for IGLOO2 devices of hot swap and cold spar (SAR53021).
- Updated the document for IGLOO2 support (SAR53021)

1.8 Revision 0

Revision 0 was the first publication of this document.

2 SmartFusion2/IGLOO2 FPGAs in Hot Swapping and Cold Sparing Applications

Microsemi SmartFusion®2 SoC FPGA and IGLOO®2 FPGA multi-standard user I/Os (MSIO) can be used in hot swapping and cold sparing applications. Hot swapping is the capability to connect external circuitry to SmartFusion2/IGLOO2 MSIOs even after power-up. Cold sparing is the capability of applying voltage to MSIOs before and during power-up. This document describes the characteristics of SmartFusion2/IGLOO2 MSIOs during power-up and provides recommendations for configuring hot swapping and cold sparing.

2.1 Power Supply Sequencing and Power-On Reset

SmartFusion2/IGLOO2 devices are designed with advanced power-up management circuitry. These circuits ensure easy transition from power-off state to power-up state. The SmartFusion2/IGLOO2 system controller performs systematic power-on reset (POR) whenever the device is powered on or reset. All the I/Os are held in a high-impedance state by the system controller until all power supplies are at their required levels and the system controller has completed the reset sequence.

VDD refers to the supply voltage to the SmartFusion2/IGLOO2 device core and VDDI refers to the supply voltage to the bank I/O buffers and I/O logic. In SmartFusion2/IGLOO2 devices, only MSIO banks are capable of hot swapping and cold sparing. The leakage current must be in microampere (µA) range for these I/Os.

On detection of a power-up event, the POR circuit sends the power-on reset signal to the system controller and reset controller in the SmartFusion2/IGLOO2 device. The power-on reset circuitry in SmartFusion2/IGLOO2 devices require the VDD and VPP supplies to ramp monotonically from 0 V to the minimum recommended operating voltage within a predefined time. There is no sequencing requirement on VDD and VPP. Four ramp rate options are available during design generation: 50 µs, 1 ms, 10 ms, and 100 ms. Each selection represents the maximum ramp rate to apply to VDD and VPP. The ramp rates can be configured by using the Libero® software.

The SERDES_VDDAIO and SERDES_VDD supplies must be powered at the same voltage as the core VDD supply. These three voltage supplies must be ramped up and down at the same time.

2.2 I/O State During Power-Up and Power-Down

Before powering up, all SmartFusion2/IGLOO2 I/Os are in tri-state mode. These I/Os remain in tri-state mode during power-up until the voltage supplies (VDD and VDDI) have reached their functional levels. After VDD and VDDI reach the functional level, the outputs exit the tri-state mode and are driven to the value determined by the design.

The behavior of SmartFusion2/IGLOO2 I/Os is independent of the VDD and VDDI sequence. Figure 1, page 3 shows a scenario where VDD is powered first, and followed by VDDI. Figure 2, page 3 shows the scenario where VDDI is powered first, and followed by VDD.

During power-down, SmartFusion2/IGLOO2 I/Os enter into tri-state mode when either of the power supplies (VDD or VDDI) drops below its brownout voltage level.

Figure 1 • **I/O State When VDD is Powered Before VDDI**

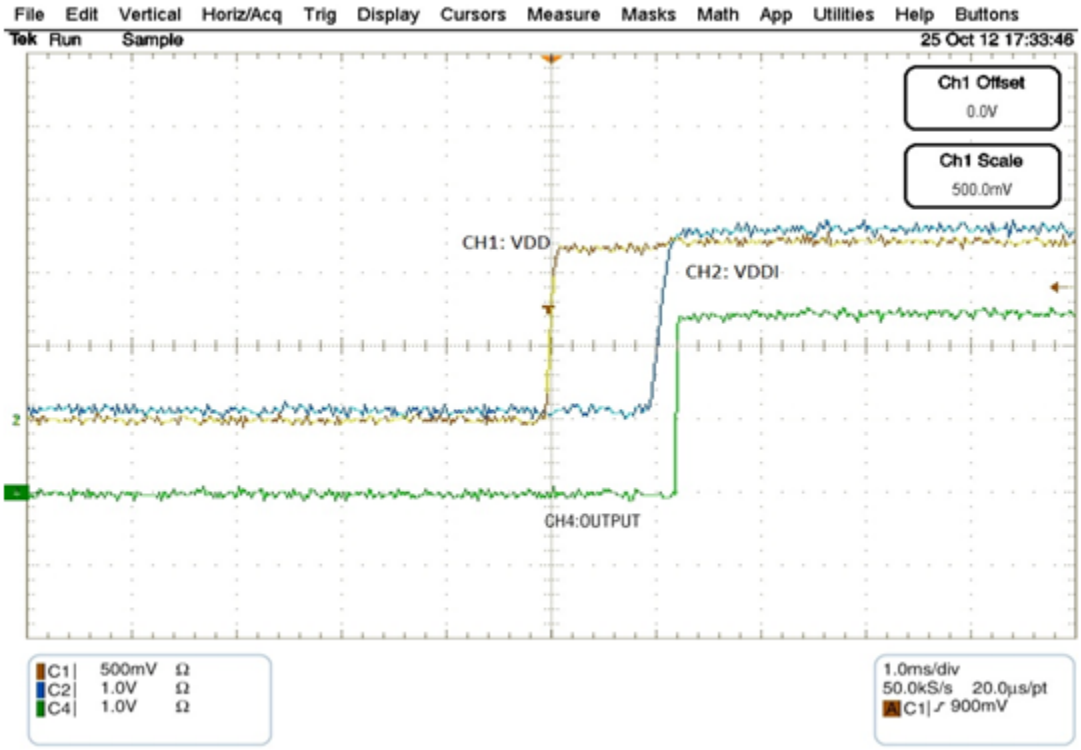
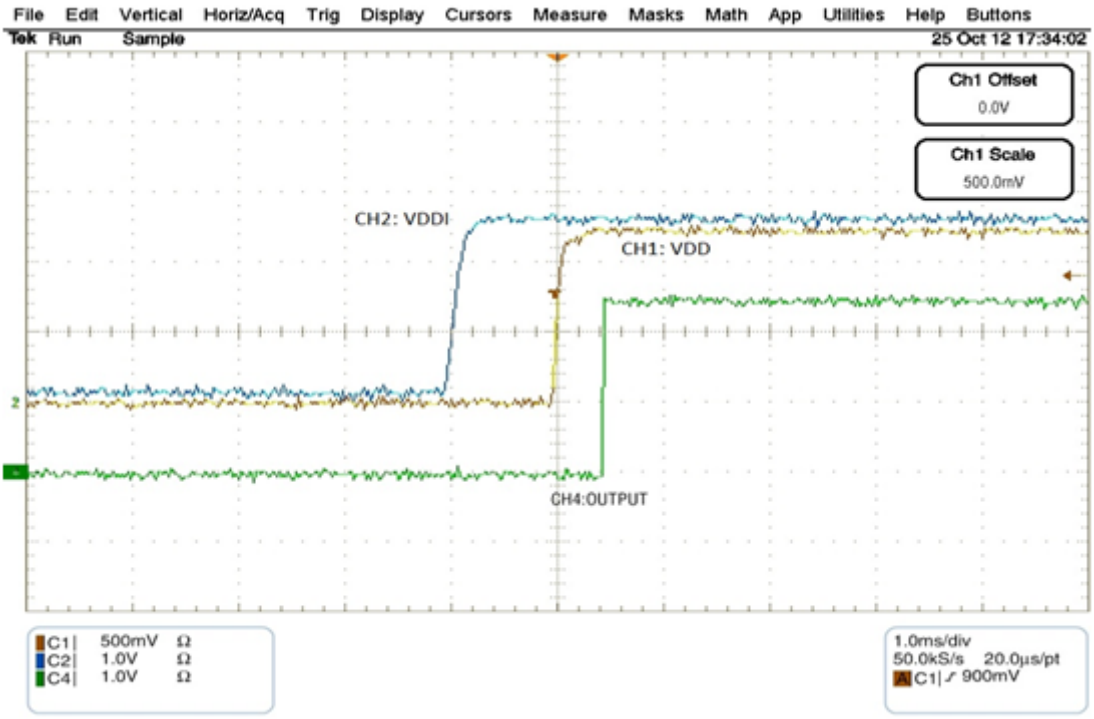


Figure 2 • **I/O State When VDDI is Powered Before VDD**



2.3 Internal Pull-Up and Pull-Down

SmartFusion2/IGLOO2 I/Os are equipped with internal weak pull-up and pull-down resistors. If used, these internal pull-up and pull-down resistors are enabled during power-up, when both VDD and VDDI have reached their functional activation level. Similarly, during power-down, these internal pull-up and pull-down resistors are disabled when either of the supply voltage (VDD or VDDI) falls below its brownout detection level.

The following table lists the devices and the banks that support hot swapping and cold sparing features.

Table 1 • **SmartFusion2/IGLOO2 Hot Swappable and Cold Sparable Banks**

Packages	Devices	Hot Swapping and Cold Sparing Capability
FC1152	M2S150T/M2GL150T	Banks 0, 3, 4, 5, 6, 8, 11, 14, 17, 18
FG896	M2S050T/M2GL050T	Banks 1, 2, 3, 8
FG676	M2S090T/M2GL090T	Banks 0, 2, 3, 5, 8
	M2S060T/M2GL060T	Banks 0, 2, 3, 4, 6, 9
FCS536	M2S150T/M2GL150T	Banks 0, 3, 4, 5, 8, 11, 14, 17, 18
FCV484	M2S150T/M2GL150T	Banks 3, 4, 5, 6, 11, 14, 17
FG484	M2S090T/M2GL090T	Banks 2, 3, 5, 8
	M2S050T/M2GL050T	Banks 1, 3, 8
	M2S025T/M2GL025T	Banks 1, 2, 4, 7
	M2S010T/M2GL010T	Banks 1, 2, 4, 7
	M2S005S/M2GL005S	Banks 1, 2, 4, 6
VF400	M2S060T/M2GL060T	Banks 2, 4, 6, 9
	M2S050T/M2GL050T	Banks 1, 3, 8
	M2S025T/M2GL025T	Banks 1, 2, 4, 7
	M2S010T/M2GL010T	Banks 1, 2, 4, 7
	M2S005S/M2GL005S	Banks 1, 2, 4, 6
FCS325	M2S090T/M2GL090T	Banks 2, 3, 5, 8
	M2S050T/M2GL050T	Banks 1, 2, 3, 8
	M2S025T/M2GL025T	Banks 1, 2, 4, 6, 7
VF256	M2S025T/M2GL025T	Banks 1, 2, 4, 7
	M2S010T/M2GL010T	Banks 1, 2, 4, 7
	M2S005S/M2GL005S	Banks 1, 2, 4, 6
TQ144	M2S010/M2GL010	Banks 2, 4, 7
	M2S005S/M2GL005S	Banks 2, 4, 6

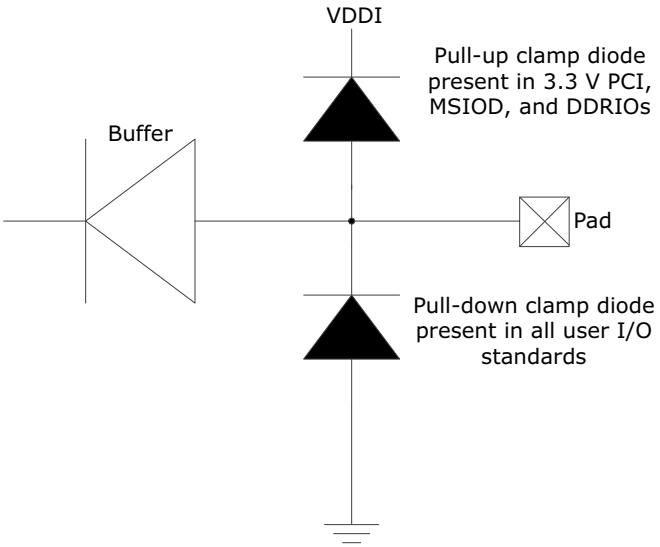
2.4 Internal Clamp Diode

The system controller puts all the user I/Os in tri-state mode during power-up. All the user I/Os have internal clamp diodes to protect the device I/Os. All MSIOs are cold sparable, because the internal clamp diodes are always disabled. If the MSIOs are configured in the PCI I/O standard, they are not cold sparable.

Note: Depending on the board configuration, each I/O pin may draw current in the order of hundreds of microamperes until VDDI is fully powered up. Therefore, do not apply voltage to the I/O pins before VDDI is powered up. This is applicable only for I/O pins that are not configured as PCI pins.

The following figure shows the internal clamp diode circuitry.

Figure 3 • **Internal Clamp Diode**



2.5 Hot Swapping

Hot swapping refers to the ability to insert or remove a board into or out of a system during system operation without causing undesirable effects to the host system or the boards. SmartFusion2 and IGLOO2 devices support hot swapping on the MSIO pins. To operate in hot swap mode, MSIO pins must be configured as either an input or a tri-state using INBUF or TRIBUF (OE=0) macros in Libero. In these configurations, the clamp diodes are disabled, and it avoids high surge current passing through the pads. To support hot swap feature, MSIOs must not be configured as output or in PCI I/O standard.

Note: MSIOD, DDRIO, and SerDes do not support the hot swapping feature.

Table 2 • **Hot Swap Functionality**

I/O Standard	Configuration	OE	Clamp Diode	Notes
MSIO	Tri-state	0	Off	Hot swap enabled
MSIO	Input		Off	Hot swap enabled
MSIO	Output		On	Hot swap disabled
PCI			On	Hot swap disabled

2.6 Cold Sparing

In cold sparing applications, voltage can be applied to device I/Os before and during power up. Cold sparing applications require the following characteristics to be supported by the device:

- I/Os must be tri-stated before and during power up.
- Voltage applied to I/Os must not power up any part of the device.
- SERDES_VDDAIO and SERDES_VDD must be powered at the same voltage as the core VDD supply. These three voltage supplies must be ramped up and down at the same time.
- Device reliability must not be compromised if voltage is applied to I/Os before or during power up.

As discussed in the I/O State During Power-Up and Power-Down, page 2, the MSIOs of SmartFusion2/IGLOO2 are in tri-state mode during power-up. Cold sparing applications rely on this silicon feature. To implement cold sparing, see the following figure.

When these conditions are met, any I/O of an unpowered device can be safely driven with very minimal leakage current. It is a good design practice not to use outputs of an unpowered (or partially powered) SmartFusion2/IGLOO2 devices to drive other components in the system.

In SmartFusion2/IGLOO2 devices, only MSIOs support cold sparing feature. The reliability of SmartFusion2/IGLOO2 MSIOs is guaranteed, if the voltage level applied to the device I/Os is less than 3.6 V as specified in the product datasheets. Therefore, SmartFusion2/IGLOO2 MSIOs meet all the requirements stated earlier in this section and are suitable for cold sparing applications.

During cold sparing, the actively driven MSIO I/O pad leaks current of up to 200 uA through VDDI rail (that is, I/O bank supply) to the ground. The amount of the current leakage depends on the resistivity of the VCCI rail to ground when unpowered. For example, this current leakage is eliminated, if the VDDI rail is floating when not powered (that is, no resistive path to the ground) and it will be at its maximum if the I/O bank VDDI is shorted to the ground when not powered.

Since, this leakage current is simply a resistive leakage to ground (that is, no clamp diodes), it does not bias the not powered rail. Moreover, this current leakage has no reliability implications on the device. However, it is recommended to provide VDDI supply voltage to the cold spare part. Since, this reduces the MSIO leakage by a factor of 100.

The leakage current of the MSIO inputs are different for biased and un-biased circuitries (<10 uA for biased and ~80 uA in biased). When the inputs are driven high and the device is not powered to determine the pull-up or series resistor values to keep the I/O voltage levels within the specification.

Note: MSIOD, DDRIO, and SERDES and JTAG pins do not support the cold sparing feature.

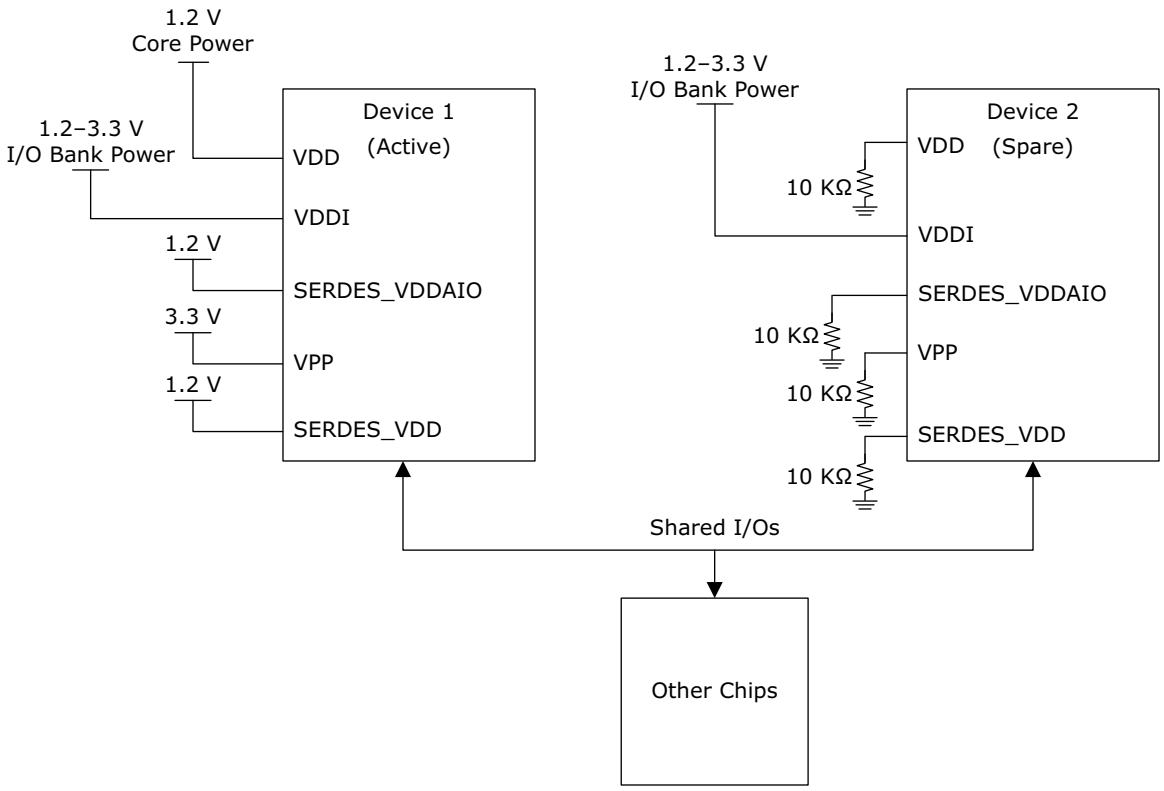
A typical cold sparing application integrates two parallel devices with shared I/O connections, as shown in the following figure. These devices must be connected as follows:

- The core VDD, SERDES_VDDAIO, SERDES_VDD, VPP, and I/O bank supplies of the primary device (Device 1) must be powered and fully functional until a swap of devices is necessary.
- The core VDD, SERDES_VDDAIO, SERDES_VDD, and VPP supplies of the secondary device (Device 2) must be pulled down to ground using a 10 kΩ resistor. This arrangement establishes a low-power, protected state for the spare device.
- At any point, cold swap can be made by powering down core VDD, VPP, SERDES_VDD, and SERDES_VDDAIO of the primary device and powering up core VDD, VPP, SERDES_VDD, and SERDES_VDDAIO of the spare device while following the configuration sequence for each device.
- If the input pins of the spare device are unused, ground it or tie it to VDDI via a 10 kΩ resistor.
- If the output pins of the spare device are unused, float it.

Note: All VDDI supplies with activity on I/O pins must be powered on the spare device.

Device 1 and device 2 are identical, and only one of the two can be active at a time. When core VDD, VPP, SERDES_VDD, and SERDES_VDDAIO are high, the device is activated. When core VDD, VPP, SERDES_VDD, and SERDES_VDDAIO are low, the device is deactivated.

Figure 4 • **Cold Sparing**



The spare device must tie the VPP, core VDD, SERDES_VDD, and SERDES_VDDAIO to ground through 10 kΩ resistors. Avoid hard-grounded and floating supplies, because this can put the device at high risk of latch-up. Supplies can be grouped to a single 10 kΩ resistor or grounded separately using 10 kΩ resistors according to the design requirements. All VDDI supplies with activity on I/O pins must be powered on the spare device. All unused supplies must be tied to ground through 10 kΩ resistors and must not be left floated.The following table lists the cold sparing board tie offs.

Table 3 • **Cold Sparing Board Tie Off**

Supply	Tie Off	Description
VDD	10 kΩ to GND	Power for core pins.
PLL_VDDA	Connect to supply or tie off 10 kΩ to GND	Power for PLLs.
VPP	10 kΩ to GND	Power for digital and analog programming blocks.
SERDES_VDDAIO	10 kΩ to GND	Power for SerDes analog blocks
SERDES_VDDPLL	Connect to supply or tie off 10 kΩ to GND	Power for SerDes PLLs.
SERDES_VDD	10 kΩ to GND	Power for SerDes core.
VREF	10 kΩ to GND	Power for FDDR/MDDR voltage reference pins.

Note: In some package devices, SERDES_VDD pins are connected to core VDD pins internally. For more information, refer to AC393: Board and Layout Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note.

The following are the advantages of cold sparing:

- Spare device is deactivated.
- Spare device I/O buffers are disabled, but powered. Therefore, there is no current leakage in the spare device.
- The spare part in flash freeze mode is to avoid the current leakage.

2.6.1 I/O Standards for Hot Swapping and Cold Sparing

The following table lists the I/O standards that support hot swapping and cold sparing.

Table 4 • **IO Standards for Hot Swapping and Cold Sparing**

	Fabric I/Os			Hot-Swap/Cold-Spare
I/O Standard	**MSIO**	**MSIOD**	**DDRIO**	**MSIO**
LVTTL	Yes	–	–	Yes
PCI	Yes	–	–	–
LVPECL (Input only)	Yes	–	–	Yes
LVDS33	Yes	–	–	Yes
LVCMOS12	Yes	Yes	Yes	Yes
LVCMOS15	Yes	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes
LVCMOS25	Yes	Yes	Yes	Yes
LVCMOS33	Yes	–	–	Yes
SSTL2I	Yes	Yes	Yes	Yes
SSTL2II	Yes	–	Yes	Yes
SSTL18I	–	–	Yes	–
SSTL18II	–	–	Yes	–
SSTL15I (only for I/Os used by MDDR/FDDR)	–	–	Yes	–
SSTL15II (only for I/Os used by MDDR/FDDR)	–	–	Yes	–
HSTLI	–	–	Yes	–
HSTLII	–	–	Yes	–
LVDS	Yes	Yes	–	Yes
RSDS	Yes	Yes	–	Yes
Mini LVDS	Yes	Yes	–	Yes
BUSLVDS	Yes	Yes	–	Yes
MLVDS	Yes	Yes	–	Yes
SUBLVDS (Output only)	Yes	–	–	Yes

2.7 Conclusion

SmartFusion2/IGLOO2 devices do not require power-up and power-down sequencing and have extremely low power-up inrush current in any power-up sequence. SmartFusion2/IGLOO2 devices have both cold sparing and hot swapping capabilities.