HALT Evaluation of SJ BIST Technology for Electronic Prognostics

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***Abstract*—This paper presents the design, test, and results of a highly accelerated life test (HALT) evaluation of a soft-core called Solder Joint Built-in Self-Test™ (SJ BIST™), a method for detecting faults caused by solder-joint fractures in monitored input/output (I/O) pins of field programmable gate array (FPGA) devices, especially those in ball grid array (BGA) type of packages. Modern electronics utilize large FPGAs packages attached to electronic boards by means of solder joints, such as solder balls, between the package and the board. Thermo-mechanical stresses – primarily heat and vibration – cause fatigue damage and eventual fracture failure of one or more balls, which causes intermittent operational faults leading to catastrophic failures in critical systems. Such intermittent faults are difficult to reproduce on a test bench and many field returns of electronic modules with intermittently failing solder balls are diagnosed with code "no trouble found/could not reproduce." The SJ BIST soft-core offers a solution because it detects faults in monitored pins caused by fractured solder joints of programmed FPGAs on deployed electronic boards.**

At the end of the three-month HALT, selected FPGAs were subjected to die-and-pry and cross-section examination and comparison to the collected data. Analysis confirmed that SJ BIST did report the occurrence of faults on damaged pins, and SJ BIST did not report any false negatives. The HALT confirmed the efficacy, accuracy, and reliability of SJ BIST as both a prognostic and diagnostic tool for FPGAs in BGA type of packages.

Keywords-solder joint; solder balls; FPGA; BIST; field programmable gate array; HALT; BGA

I. INTRODUCTION

Under NAVAIR[1] funding BAE Systems, Johnson City, NY designed and ran a highly accelerated life test (HALT) using Solder Joint Built-in Self-Test™ (SJ BIST™)[2] from Ridgetop Group, Inc., Tucson, Arizona. The primary objectives of the jointly-defined HALT were to evaluate the efficacy, accuracy, and reliability of SJ BIST to detect faults caused by fractured solder joints of input/output (I/O) pins of ball-grid-array (BGA) devices such as field programmable gate arrays (FPGAs). The secondary objective was to confirm or deny the assertion that I/O pins nearest a corner of a BGA device were likely to fail sooner than other pin locations. The SJ BIST HALT successfully detected faults caused by the following: wiring errors in the board, loss of power to the board, damaged cables, and fractured solder joints. There were no false alarms. The overall evaluation is the HALT confirmed the efficacy, accuracy, and reliability of SJ BIST as both a prognostic and diagnostic tool for FPGAs in BGA type of packages. The Johnson City half of the team commented: "We believe in the SJ BIST approach and that it works."

Modern electronics utilize large FPGAs in high-density, array-type of packages that are attached to electronic boards by means of solder joints, such as solder balls, between the package and the board. Thermo-mechanical stresses – primarily heat and vibration – cause fatigue damage and eventual failure of one or more balls (Fig. 1) leading to intermittent operational faults and eventual catastrophic failures. Such intermittent failures are difficult to reproduce on a test bench and many field returns of electronic modules are diagnosed with "no trouble found/could not reproduce" codes.

The SJ BIST soft-core offers a solution because it detects fracture faults in monitored pins of FPGAs on programmed, deployed electronic boards.

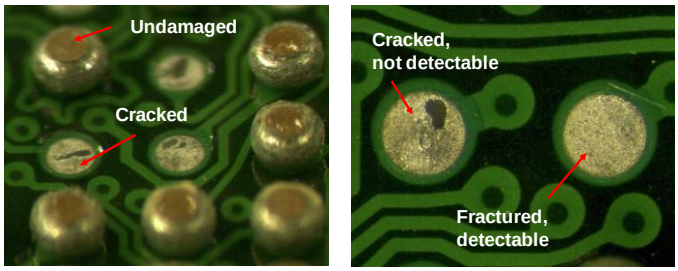

Figure 1. Damaged and undamaged solder balls.

II. DESIGN OF EXPERIMENT

The design of experiment included the system configuration and control, the test evaluation boards (TEBs), the physical mounts, and the HALT regime. In addition to hardware,

[1] *Naval Air Systems Command: contract N68335-07-C-0172*

[2] U.S. patent 7,501,832, Mar. 10, 2009

firmware and software was written to synchronize the HALT cycles and the collection of data produced by the SJ BIST firmware. The block diagram of the SJ BIST HALT system is shown in Fig. 2.

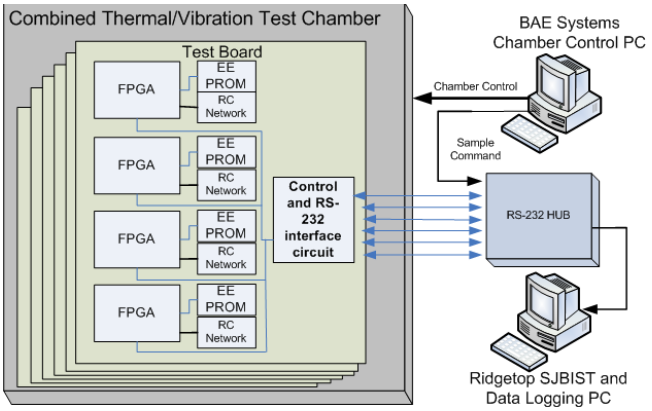

Figure 2. Block diagram of the SJ BIST HALT system.

A. *System Configuration*

The HALT system configuration is comprised of six test evaluation boards (TEBs) mounted in a combined thermal-vibration test chamber. Each board is populated with four Xilink® FGG900[3] (lead-free) 900-pin FPGAs running an SJ BIST program, which is loaded from a programmable read-only memory (PROM) programmed via JTAG (Joint Test Action Group) interface standardized as IEEE 1149.1 Test Access Port and Boundary Scan. The SJ BIST program monitors pairs of I/O pins connected to capacitors. A BAE-written chamber program controls the cycling of the boards, the application of vibration steps during each thermal dwell, and the sending of a "Sample" command to a Ridgetop-written program. SJ BIST fault data from each FPGA on each board is logged at each HALT cycle to a laptop Personal Computer (PC) using an RS-232 interface and a serial port (Universal 1600-8) as a hub.

B. *Board Layout - Programming Interface*

Fig. 3 shows the layout of the programming interface of the TEBs. Firmware is loaded into a controller PROM-FPGA pair to (1) control the programming for each device under test (DUT) FPGA on a TEB and (2) to control the collection of data from the DUTs.

C. *Board Layout – Data Interface*

Fig. 4 shows the data interface between the DUTs and the controller FPGA. Data is serially output from the controller FPGA using the RS-232 interface.

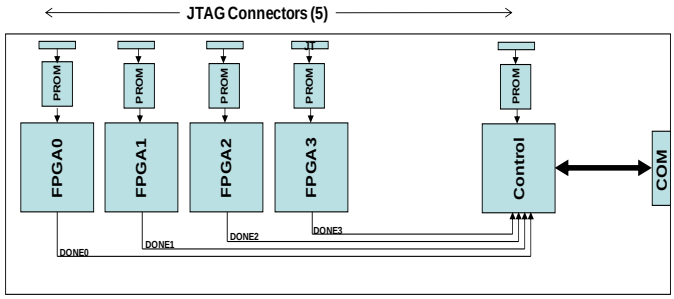

Figure 3. Board programming interface.

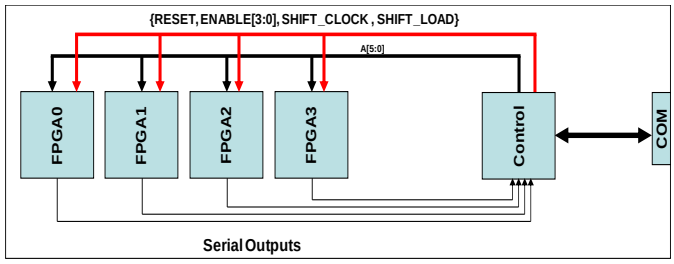

Figure 4. Data output interface

D. *Board Cabling and Mounting*

Fig. 5 shows a single-board, pre-HALT cabling setup used to verify the board design and correct operation of SJ BIST in the FPGAs; Fig. 6 shows a mounting fixture (1 of 2) with three boards.

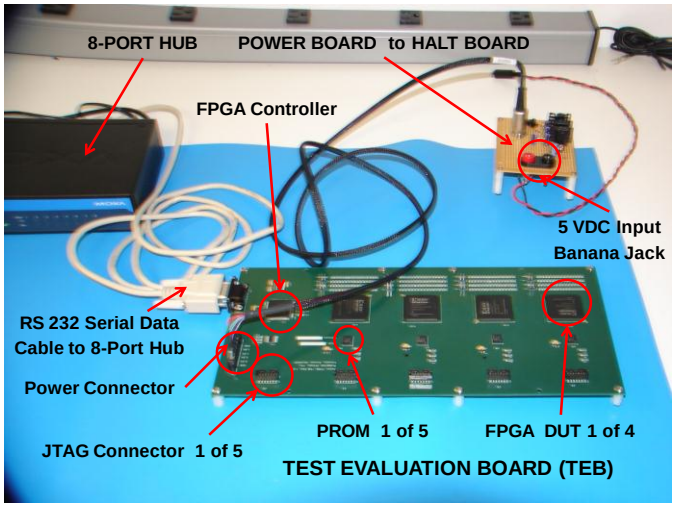

Figure 5. Single board cabling setup used for pre-HALT verification.

E. *HALT Regime*

Table I shows the specifications for the three-hour thermal cycles. The induced vibration was random: power spectral densities (PSDs) equal to 0.005 g^2/Hz. The frequency range was 20 Hz to 600 Hz. Then the induced vibration was linearly decreased (0.0005 g^2/Hz at a fixed frequency of 2,000 Hz). This vibration step started 20 minutes after the start of each dwell and lasted for 20 minutes.

[3] SPARTAN® XC3S4000™ FGG900EGQ080 D3124927A

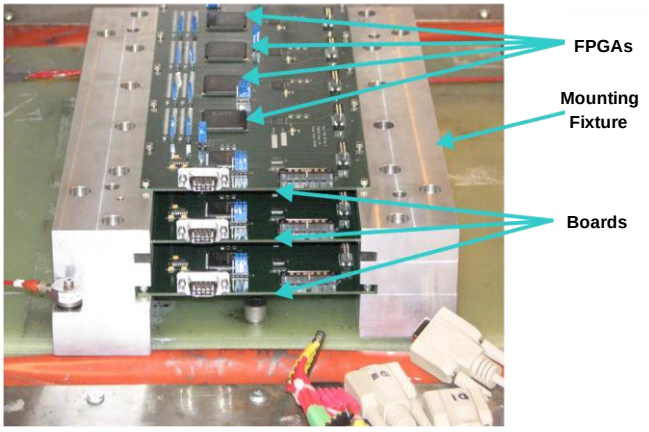

Figure 6. One of two mounting fixtures, three boards each.

TABLE I. THERMAL CYCLE SPECIFICATIONS

Temperature	Time	Description
-55 °C	1 Hour	Dwell at Cold
-55 to125 °C	0.5 Hour	Ramp from Cold to Hot
125 °C	1 Hour	Dwell at Hot
125 to -55 °C	0.5 Hour	Ramp from Hot to Cold

F. SJ BIST Operation

For each selected group of 2 pins, SJ BIST writes a '10' bit pattern through a first I/O port of a two-pin group to charge and discharge a capacitor attached to that group. The second I/O port of the group is used to read the '1' bit immediately after it is written. When the resistance of the first I/O port becomes too large, the charge on the capacitor will be insufficient to be read as a '1' bit (see Fig. 7). In the next clock cycle, the '10' is written using the second I/O port and the first I/O port is used to read the '1' bit.

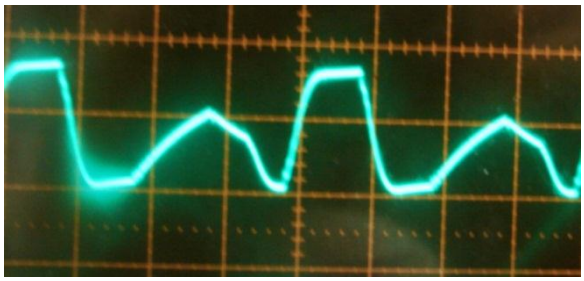

Figure 7. High solder-joint resistance in an I/O port causes faults.

G. HALT Pin Pairs (Groups)

The two-pin soft-core for SJ BIST was used to create a firmware program that monitored 32 groups of two pins; 64 pins total. The monitored groups are shown in Fig. 8, and the group and pin numbers are shown in Table II.

III. HALT RESULTS

A three-month HALT was run from 16 November 2009 and continued through 16 February 2010. Because of preliminary checks, the first actual HALT cycle was logged as number four.

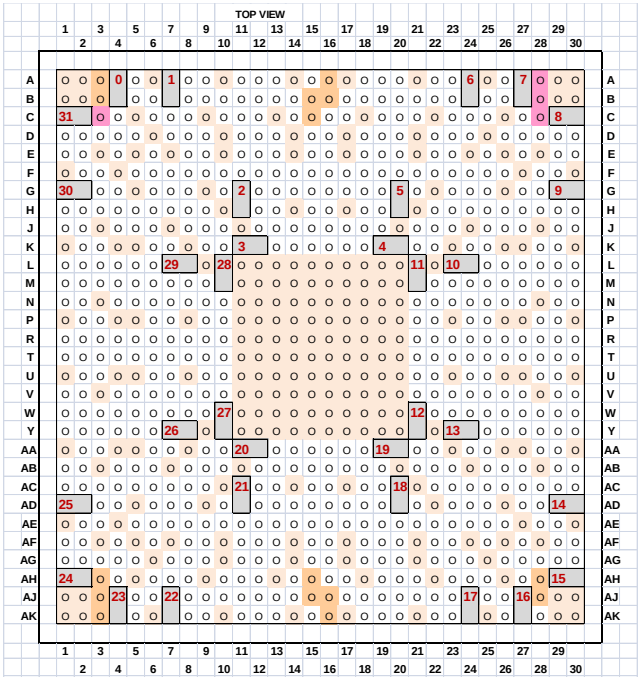

Figure 8. Monitored groups of two pins each.

TABLE II. GROUP AND PIN NUMBERS

Group Number	Pin 0	Pin 1	Group Number	Pin 0	Pin 1
0	A4	B4	16	AJ27	AK27
1	A7	B7	17	AJ24	AK24
2	G11	H11	18	AC20	AD20
3	K11	K12	19	AA19	AA20
4	K19	K20	20	AA11	AA12
5	G20	H20	21	AC11	AD11
6	A24	B24	22	AJ7	AK7
7	A27	B27	23	AJ4	AK4
8	C29	C30	24	AH1	AH2
9	G29	G30	25	AD1	AD2
10	L23	L24	26	Y7	Y8
11	L21	M21	27	W10	Y10
12	W21	Y21	28	L10	M10
13	Y23	Y24	29	L7	L8
14	AD29	AD30	30	G1	G2
15	AH29	AH30	31	C1	C2

A. Cycle 4 (28 October 2009): Verify Electrical

Five of the 24 FPGAs were found to be nonresponsive prior to starting the HALT: Board 2, FPGAs 0 and 1; board 5, FPGA 0; and board 6, FPGAs 0 and 1. Because of time and budget constraints, we elected to not fabricate replacement boards. The logged data for HALT cycle 4 (HC4) confirmed the null responses from those FPGAs.

In addition to reporting a null response from FPGA 0 and 1, the data log (see Fig. 9) for board 2 showed pin group 0 of FPGA 2 had a hard error on both pins. This same error occurred on FPGA 2 on all boards. The data log also indicated that both pins in group 23 of that FPGA were open: subsequent cycles indicated that group experienced intermittent faults. The "POWER ON" record indicates this is the first log after the board was powered on.

```
          BOARD START: 2
POWER ON:
NULL FPGA RESPONSE: 0   <----
NULL FPGA RESPONSE: 1
FPGA DATA: 2
0202000F00010001        <----
0202170F00010001        <----
02021F0000000000
FPGA DATA: 3
02031F0000000000
          BOARD END: 2
```

Figure 9. Partial data log for board 2.

Fig. 10 is a graphical view of the HALT status: ■ = no response from the indicated FPGA, ■= solid error(s) in the indicated pin group; ■ = intermittent faults in the indicated pin group, ■= no data written, and ■= over 100 intermittent faults in the indicated pin group. The eight outlined groups are those nearest a corner of a DUT.

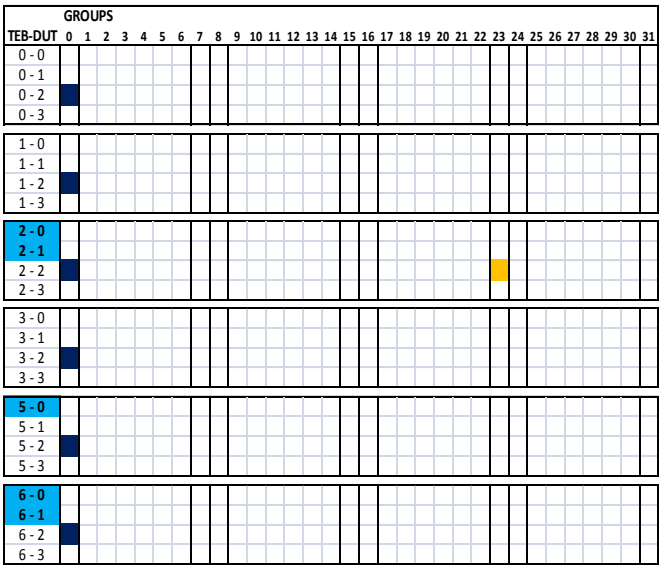

Figure 10. HALT status for cycle 4.

B. *HALT Cycles 5 – 23(20 November):Verify Logging*

Continuous HALT cycling began 16 November and on 20 November the logged data for cycles 5 through 23 were sent to Tucson for analysis to verify the firmware and software to collect and log data were working correctly. Fig. 11 shows intermittent faults occurring in six additional pin groups.

C. *HALT Cycles 24 – 72 (30 November): Over Current*

On 25 November, it was noticed the 5A 5VDC power supply was going into current-limiting mode. We decided to reduce the oven temperature to 85°C (see Fig. 12) until we could replace the original with a larger power supply. When we examined the logged data records, and we determined the previous damage to boards 2 and 6 had increased as shown in Table III, Table IV, and Fig. 13:

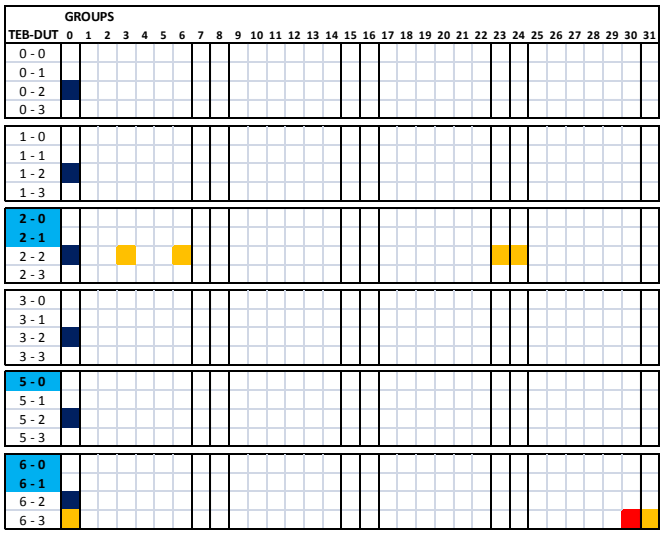

Figure 11. HALT status for cycle 23.

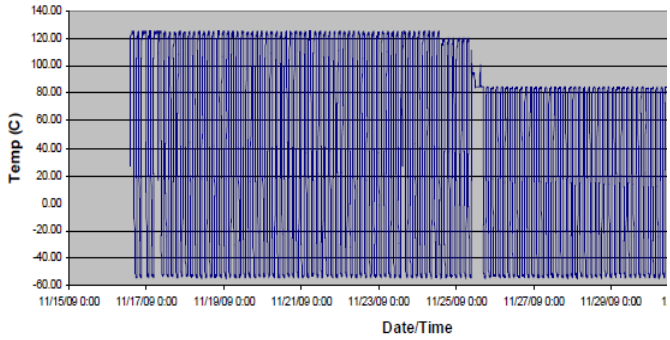

Figure 12. Partial profile of the chamber temperature.

TABLE III. LOG RECORDS, HALT CYCLE 35

	HC 35	Logged Record
1	Board 2, FPGA 2, group 23: hard open	0202170F00010001
2	Board 6, FPGA 3, grp 30: high intermittency	06031E0F00050F0F

TABLE IV. LOG RECORDS, HALT CYCLE 72

	HC 72	Logged Record
1	Board 1 and 6: no change	
2	Board 5: FPGA 0, 2, and 3	NULL FPGA RESPONSE
3	Board 5: FPGA 1 - all pins broken (suspicious)	050100050F0F0F0F
4	Board 0, 2, and 3	NO SIGNAL

D. *HALT Cycles 73 – 257 (29 January 2010)*

The HALT was suspended on 30 November until the 5VDC power supply was replaced 5 December. A power outage in Johnson City on 15 December shutdown the HALT power supplies, a condition that was not noticed until 21 December.

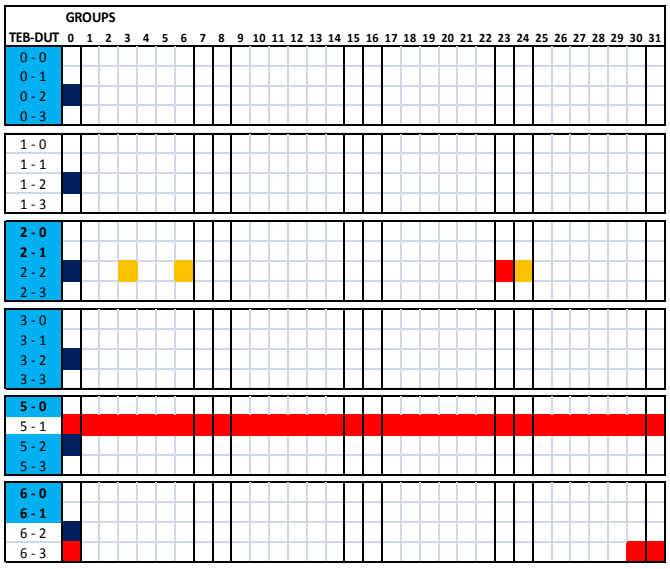

Figure 13. HALT status at end of cycle 72 (30 November).

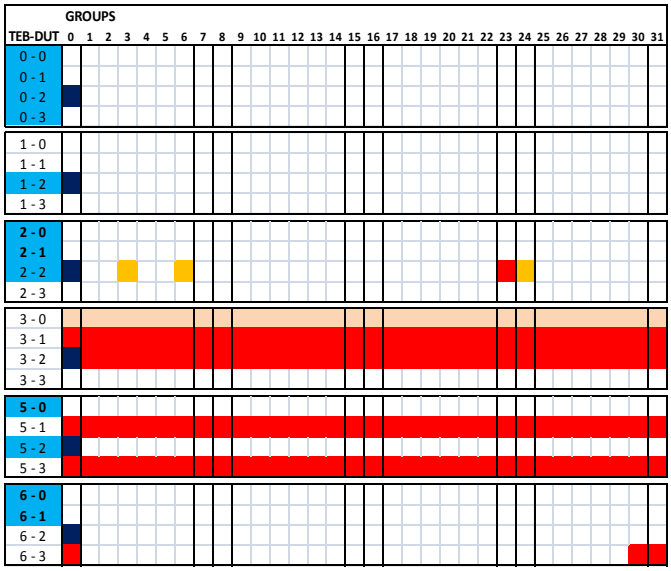

Figure 14. HALT status at end of cycle 204 (13January 2010).

The logged data records ending 13 January were sent to Tucson for examination: nine new error and fault conditions were noted as shown in Table V and Fig 14. The team in Tucson asked the team in Johnson City to examine the cables: the RS-232 cables exhibited high-heat damage to include brittle and broken insulation, and interior material liquefied and oozing (see Fig. 15). The HALT was again suspended on 29 January pending replacement of the RS-232 cables. Board 0 was returned to Tucson for physical examination: there was no visible sign of damage.

TABLE V. NEW ERRORS AND FAULTS: HALT CYCLE 204

	HC 204	Logged Records
1	Board 0, no response from the controller	missing all records
2	Board 1, FPGA 2 stopped responding	NULL FPGA RESPONSE: 2
3	Intermittent power off-on	0103200505050505
		POWER ON:
		0103210505050505
4	Board 2, FPGA 2 stopped responding	NULL FPGA RESPONSE: 2
5	Board 3, FPGA 0, bad dummy record	0300200000000000
	instead of 03000200505050505	
6	Board 3, FPGA 1 through 3, high fault counts	for example:
	248 and 208 faults	030100050F080D08
	149 and 172 faults	0301010509050A0C
	32 and 38 faults	0301020502000206
7	Board 5, FPGA 1, moderate counts: 25 and 39	0501000501090207
	16 and 14	050101050100000E
	2 and 4	0501020500020004
8	Board 5: FPGA 2 stopped responding	NULL FPGA RESPONSE: 2
9	Board 5: FPGA 3, fairly high counts: 160 and 4	0503000501000004
	161 and 7	0503010501010007
	14 and 3	05030205000E0003

The log records for 29 January showed three additional error conditions: boards 2 and 5 stopped responding and FPGA 3 on board 3 showed high fault counts. Only boards 1 and 6 showed operational FPGAs (see Fig. 16): five operational FPGAs out of 24.

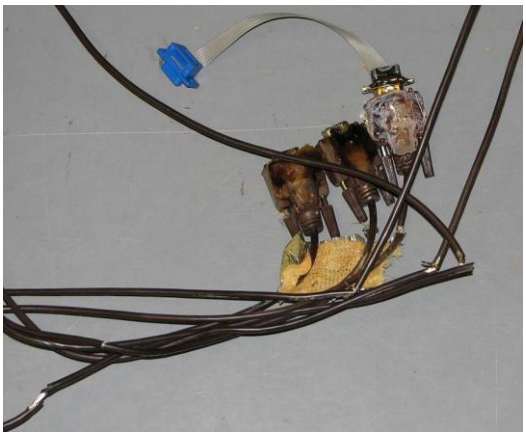

Figure 15. Heat damaged RS-232 cables.

E. HALT Cycles 287 – 324 (16 February)

The HALT was resumed 9 February after the RS-232 cables were replaced (cycle 258) with logging resumed that day starting with cycle number 287. Examination of the logged records indicated that three boards were once again responding: board 2, FPGA 3 (no faults); board 3, FPGAs 1, 2 and 3 (no faults); and board 5, FPGAs 1, 2, and 3 (high fault counts on all three FPGAs)[4]. 12 operational FPGAs out of the 20 on the remaining five boards (board 0 had been returned for inspection).

We ended the HALT on 16 February (cycle 322): the logged records at the end of the HALT were identical to those at the restart on 9 February (cycle 287): no additional errors or faults occurred. Fig. 17 shows the status.

[4] Cable swapping did not change the high fault counts: board five is definitely damaged – might be the controller FPGA on that board.

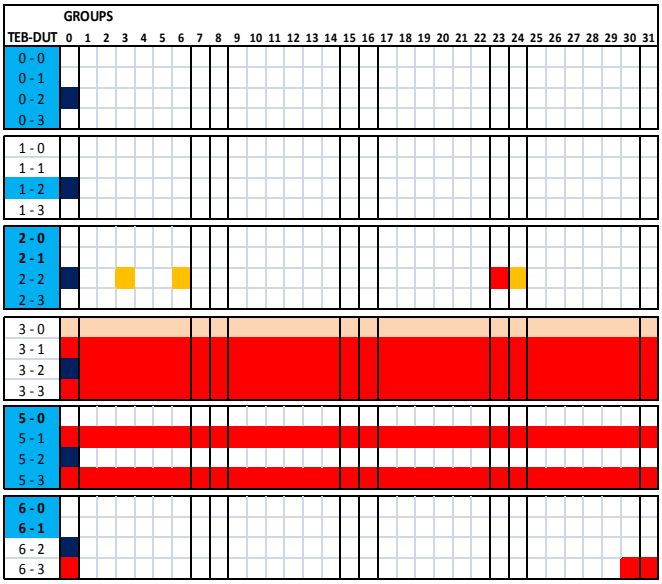

Figure 16. HALT status at end of cycle 257 (29 January).

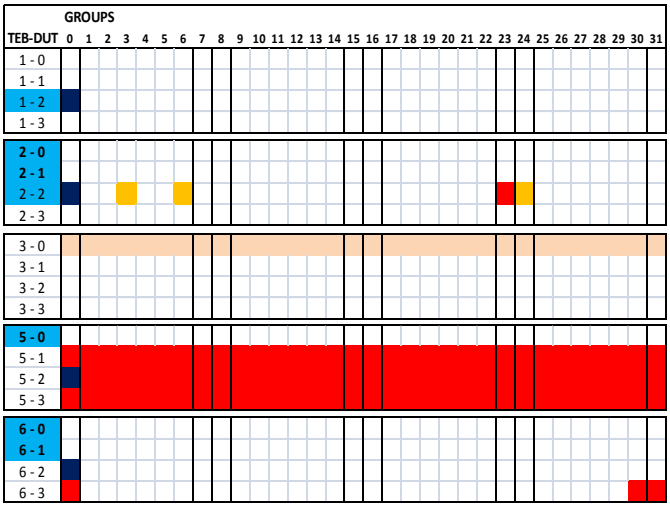

Figure 17. HALT status for cycle 287 and 322 (9 – 16 February).

IV. Post Halt Analysis

After the HALT ended, we did a limited number of dye and pry and cross-section examinations.

A. Dye and Pry

For the dye and pry examination (37 images), we selected board 2, FPGA 0, which was reported as null response from the very start of the HALT. Fig. 18 shows the one of the corners (A30) and clearly shows a failed pin next to the four corner (ground) pins, and three of the four ground pins fractured. At all four corners, there was at least one ball next to the corner that was fractured.

Looking at the middle clock pin shown in Fig. 18, the appearance of the ball indicates it was not securely attached to the board land – there is a lack of solder damage from the pry. This might have caused a loss of the clock, which might explain the non-responsiveness of that FPGA.

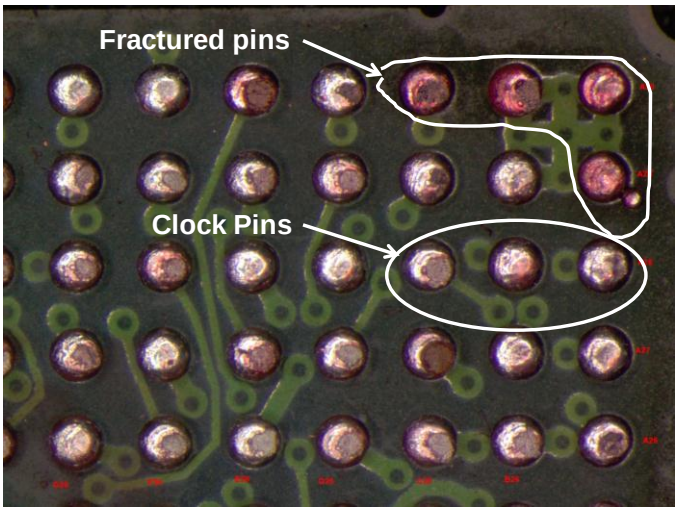

Figure 18. Dye and pry of board 2, FPGA 0.

B. Cross Sectioning

We cross sectioned 48 pins and examined 103 images. We concluded the following: pins that SJ BIST reported as having faults were fractured (no false alarms), an example of two pins C1 from group 31, board 6, FPGA 3 and G1 from group 30, board 6, FPGA 3 are shown in Fig. 19. Both balls are fractured, and referring to Fig. 17, SJ BIST detected high number of faults. With one possible exception (see Fig. 21), no fractures were found in pins SJ BIST reported as healthy. Fig. 20 shows two pins monitored by SJ BIST and for which no faults were reported: those pins were not fractured.

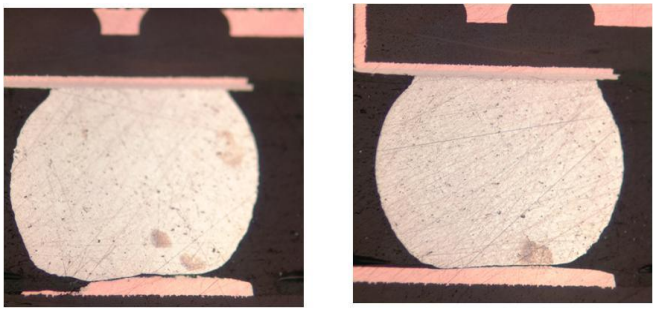

Figure 19. Pins C1 (left) and G1 (right), board 6, FPGA 3.

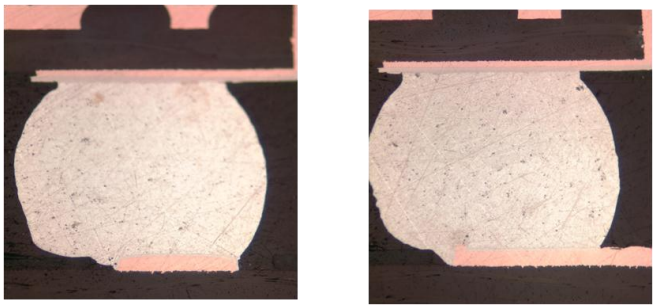

Figure 20. Pins C30 (left) and G30 (right), board 6, FPGA 3.

V. Intermittent Nature of Solder-Joint Faults

In addition to the possible contact point shown in Fig. 21, a fault might not occur for any number of other reasons: (1) The cross sectioning might have hidden a partial contact point (see

Fig. 22); (2) Vibration stresses might not have caused the fractured surfaces to open: conformal coating might dampen the effect of a vertical strain on device; and (3) The fault duration might be too short: the minimum fault duration is one-half of a clock cycle (20ns for this HALT). Guaranteed fault detection requires the fault to last at least 2 clock periods (80ns) and have an effective open resistance of 100Ω or more.

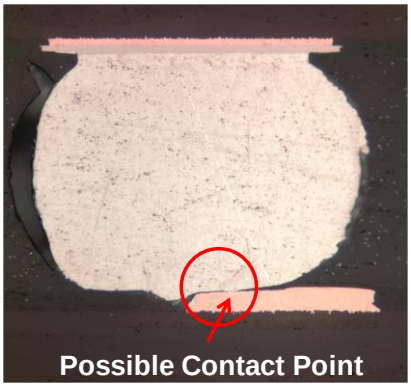

Figure 21. Fault not detected:board 6, FPGA 3, pin A24.

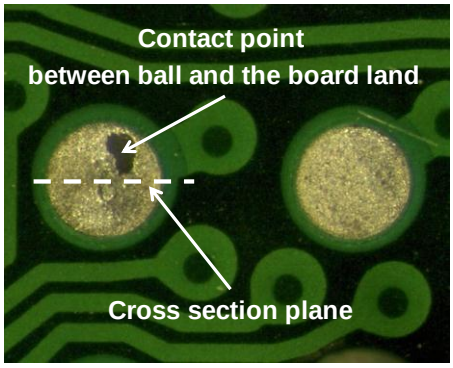

Figure 22. Cross sectioning can hide a partial contact point.

This apparent fracturing with no detectable occurrence of faults is an example of the intermittent nature of solder-joint caused faults. Another example is cycle 54: SJ BIST reported the occurrence of only two faults each for board 6, FPGA 3, group 31, pins C1 (which Fig. 19 shows is clearly fractured) and C2. There were a total of 270 billion – yes, billion – writes of a '1' bit to each of those two pins in that 3-hour HALT cycle. Such a low intermittency rate makes it extremely difficult to diagnose in real time or in a bench type of test

VI. Summary, Conclusion, and Lessons Learned

A. *Summary and Conclusion*

Faults caused by the following were detected: wiring errors in the board, loss of power to the board, damaged cables, and fractured solder joints. There were no false alarms. Of the seven faulty 2-pin groups, five were as near as possible to an outer corner of an FPGA; one group was only four pin rows away; and the seventh was nearest a corner of the interior ground pins. The objectives of the HALT were more than met and SJ BIST is a proven effective tool for detecting write faults in programmed FPGAs on electronic boards.

B. *Lessons Learned*

Some of the lessons we learned about using SJ BIST for HALTS are the following:

- Reduce the write-read for each group from two clock periods to four clock periods. This reduces the I/O current requirement by one-half.
- Only monitor 8 pins interior pins instead of 32: two at each corner of the inner periphery and use the other 24 pins to monitor the outer periphery.
- Design and develop a real-time graphics display of the faults – similar to that shown in Fig. 18.
- Ensure all commercially-obtained cable harnesses are rated for 100°C.
- At 125°C, the required I/O current is much higher than at 100°C – perhaps double the rated maximum of the FPGA.

Acknowledgement

We greatly appreciate the assistance and support given to us by our Naval Air technical points of contact during the initial Small Business Innovation Research Phase I and Phase II efforts to design and develop this technology and then to further prove that technology in a HALT: Mr. Michael Begin and Mr. Thomas Dabney, Joint Strike Fighter Program Office.