Prototyping for Space-Flight Designs with Microsemi RT-PROTO FPGAs

To facilitate lower-cost prototyping and design validation activities, Microsemi SoC Group (formerly Actel) offers RTSX-SU, RTAX-S, RTAX-DSP, and RT ProASIC3 FPGAs in "RT-PROTO" form. RT-PROTO devices use the same silicon and the same packages as the flight-model FPGAs, however in order to reduce costs, some flight-model tests are not performed on the RT-PROTO devices.

Please note the following in regard to RT-PROTO units:

1. RT-PROTO parts are intended for hardware timing verification only. They should not be used for space flight applications. They should also not be used for applications or activities which require the quality of space flight parts, such as qualification of space flight hardware.
2. RT-PROTO FPGAs are offered in ceramic packages. The hermeticity of the lid seal is not tested and is not guaranteed.
3. RT-PROTO parts are tested across the full military temperature range (-55°C, room temperature, and 125°C). No Mil-Std 883 class B testing is performed. RT-PROTO parts are not subjected to temperature cycling, fine and gross leak testing, X-ray inspection, PIND testing, assembly lot Group B testing, or burn-in.
4. The lids of RT-PROTOs have a shallow dimple drilled through the top plating layers but not penetrating the thickness of the lid. The purpose of this dimple is to deter counterfeiting. The drilling operation does not cause operating characteristics of the device to deteriorate.
5. RT-PROTO units may be assembled using an assembly process that is not qualified for space flight.
6. RT-PROTO units will be marked as "PROTO".
7. RT-PROTO units may have cosmetic visual imperfections.
8. RT-PROTO units are not DSCC or QML certified.
9. No data will be shipped with RT-PROTO units.
10. Microsemi will not perform TID testing on RT-PROTO units.
11. If programming at the Microsemi factory is required, the programming files must be supplied at the time of order placement; Microsemi cannot reserve inventory or units from lots in process pending receipt of customer programming files.
12. No special or customer specific testing will be available for RT-PROTO units. Requests for Single Lot Date Code, specific date codes, Single Wafer Lot, date code restrictions, or specific wafer lots will not be accepted.
13. Microsemi cannot guarantee availability of flight units from the same wafer lot or date code as the RT-PROTO units.
14. No customer QA clauses will be accepted on RT-PROTO orders. There will be no review of customer Terms and Conditions on RT-PROTO orders -- orders will be accepted to Actel's standard Terms and Conditions only.
15. RT-PROTO units are under the same export controls as standard RT units.

Although the RT-PROTO devices are assembled in ceramic packages with a hermetic lid seal process, the lid hermeticity is not tested and is not guaranteed. The seal integrity should be sufficient to protect the FPGA during normal PCB manufacturing and cleaning processes. However, since hermeticity is not guaranteed, the RT-PROTO devices should not be subjected to thermal vacuum tests. System level flight-model qualification should be performed with flight-qualified FPGAs, meaning FPGAs screened to at least Mil Std 883 class B.

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