VHDL VITAL and Verilog Compile Instructions for Standalone Model*Sim* with Libero® IDE

If you have a standalone version of Model*Sim*, it can be integrated with Actel Libero Integrated Design Environment (IDE) software in such a way that if you run simulation inside Libero IDE, it will:

- Automatically map the compiled VITAL (VHDL) or Verilog library
- Compile source code and testbench

You can download VITAL and Verilog library source files from the Actel website. You must compile the Actel source library and map it during simulation.

To automatically map your compiled libraries and compile your source code and testbench:

1. Open **Libero IDE**. From the **Options** menu, select **Profile**.
2. Add the **Model*Sim*** standalone executable. Type in the full location of the Model*Sim* executable in the **Location** field (Figure 1).

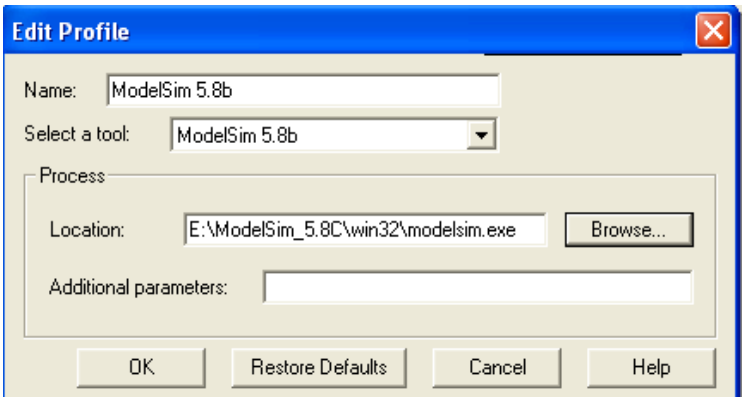

Figure 1 • **Profile Dialog Box**

You must compile the VITAL and/or Verilog libraries in a specific directory.

Compile the VHDL VITAL Library

The procedure below describes how to compile an Actel VITAL library in the **<Drive>:\ModelSim\Actel\VHDL** directory.

1. Create a new directory tree called **\Actel\VHDL\src** directory in your Model*Sim* installation directory, i.e **<Drive>:\ModelSim\Actel\VHDL\src**. Copy the source library you downloaded from the Actel website into the src folder you just created.
2. Invoke the Model*Sim* HDL simulator.
3. Change your directory to **<Drive>:\ModelSim_install\Actel\VHDL**. Type the following command at the prompt:

   ```
   cd <Drive>:/ModelSim_install/Actel/VHDL
   ```

4. Create a family library directory **<fam_lib>** for your simulator. Type the following command at the prompt:

   ```
   vlib <fam_lib>
   ```

   i.e., `vlib a54sxa`

5. Map the Actel VITAL library to the **<fam_lib>** directory. Type the following command at the prompt:

   ```
   vmap <fam_lib> <Drive>:/ModelSim_install/Actel/VHDL /<fam_lib>
   ```

6. Compile the library. Type the following command at the prompt:

   ```
   vcom -work <fam_lib> src/<act_fam>.vhd
   ```

   For example, to compile the SX-A library for your simulator, type the following command:

   ```
   vcom -work a54sxa src/54sxa.vhd
   ```

7. (Optional) Compile the migration library. Only perform this step if you are using the migration library. Type the following command at the prompt:

   ```
   vcom  -work <fam_lib> src/<act_fam>_mig.vhd
   ```

Verilog Library Compile

The procedure below explains how to compile an Actel Verilog library in the **<Drive>:\ModelSim\Actel\Vlog** directory.

1. Create a new directory tree called **\Actel\Vlog\src** in your Model*Sim* installation directory. Copy the source library you downloaded from the Actel website into the src folder you just created.
2. Invoke the Model*Sim* HDL simulator.
3. Change directory to the **<Drive>:\ModelSim_install\Actel\Vlog** directory. Type the following command at the prompt:

   ```
   cd <Drive>:/ModelSim_install/Actel/vlog
   ```

4. Create a family library directory **<fam_lib>** for your simulator. Type the following command:

   ```
   vlib <fam_lib>
   ```

i.e., `vlib 54sxa`

5. Compile the Actel library. Type the following command:

   ```
   vlog -work <fam_lib> src/<act_fam>.v
   ```

6. (Optional) Compile the migration library. Only perform this step if you are using the migration library. Type the following command:

   ```
   vlog -work <fam_lib> src/<act_fam>_mig.v
   ```

Sample Scripts

In following scripts add32.vhd, add32_tb.vhd, and add32.sdf are source code, testbench, and the SDF file, respectively. The add32_0 is the instance for add32 in testbench.

Pre-Synthesis Simulation

```
vmap work ./work_presyn
vcom -93 -work work_presyn ../hdl/add32.vhd
vcom -93 -work work_presyn ../stimulus/add32_tb.vhd

vsim work_presyn.testbench
add wave /testbench/*
run 1000ns
```

Post-Synthesis Simulation

```
vlib work_postsyn
vmap work ./work_postsyn
vcom -93 -work work_postsyn ../synthesis/add32.vhd
vcom -93 -work work_postsyn ../stimulus/add32_tb.vhd

vsim work_postsyn.testbench
add wave /testbench/*
run 1000ns
```

Post-layout Simulation

```
vlib work_postlayout
vmap work ./work_postlayout
vcom -93 -work work_postlayout ../designer/add32.vhd
vcom -93 -work work_postlayout ../stimulus/add32_tb.vhd

vsim -sdfmax /add32_0=../designer/add32.sdf work_postlayout.testbench
add wave /testbench/*
run 1000ns
```

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