Overview of iRoC Technologies Report

"Radiation Results of the SER Test of Actel FPGA December 2005"

Introduction

Following the study on neutron effects completed by iRoC Technologies in 2003, Actel commissioned iRoC to perform a further set of tests, which took place in December 2005. This new set of tests was designed to evaluate the effects of neutron bombardment on recently-introduced field programmable gate arrays (FPGAs) using advanced process technologies that were unavailable when the original tests were performed in 2003. Further, the new tests were designed to evaluate not just configuration upsets, which can disrupt the operation of an FPGA, but also data upsets in flip-flops, combinatorial logic, and embedded user-accessible memory.

iRoC Technologies is an independent third-party test company and was selected to perform this testing because of their ability to perform this testing in an unbiased manner using the industry-standard JESD-89 test methodology.

Neutron Effects—Background Information

Sub-atomic particles present in cosmic galactic rays enter the Earth's atmosphere and collide with atoms of atmospheric gases. These collisions produce a wide variety of sub-atomic particles, many of which recombine quickly. However, a significant quantity of high-energy neutrons are produced by these collisions. Neutrons possess no electrical charge, and do not recombine; instead they are slowly attenuated by the atmosphere. The greatest quantities of neutrons (called the peak neutron flux density) occur at an altitude of 60,000 feet. However, a substantial quantity of neutrons penetrate the atmosphere and reach the earth's surface.

It has been discovered that these high-energy neutrons can cause flip-flops and memory cells in modern semiconductor electronics to change state. Several industry studies and papers have been published discussing neutron effects in discrete memory ICs. The effects of neutrons on programmable logic devices, which use memory cells to determine their functionality, is a major concern. In response to this concern, iRoC Technologies conducted a series of tests in 2003 to determine the configuration memory failure rates of five different architectures of FPGAs. Following that testing, iRoC Technologies conducted an additional set of tests to determine the failure rates of three new FPGA products, using three different architectures and two different programming technologies.

Testing FPGAs for Susceptibility to Neutrons—Experiments and Results

Testing in the natural environment on the Earth's surface is a slow process, due to the low neutron flux relative to higher altitudes. Accelerated testing can be performed in an expeditious and repeatable manner to overcome this problem. Fortunately the neutron test facility at the Los Alamos Neutron Sciences Center (LANSCE) at Los Alamos National Laboratory, New Mexico, has a neutron source with an energy spectrum that closely matches the energy spectrum observed in atmospheric neutrons, but at a much higher neutron flux level. This allows for rapid acceleration of testing while maintaining close correlation with real-world conditions.

In December 2005, iRoC Technologies conducted a set of experiments designed to test the effects of atmospheric neutrons on recently-introduced FPGAs. The test methodology and results are documented in the iRoC report "Radiation Results of the SER Test of Actel FPGA December 2005" (available on request from Actel). Testing was performed on ProASIC®3, the latest Flash-based FPGAs from Actel, and Stratix®2 and Cyclone™2 SRAM-based FPGA architectures from Altera. Tests were performed in compliance with JEDEC specification JESD-89, which is recognized as the industry standard specification for the measurement of neutron effects. Each device tested was exposed to a cumulative neutron fluence of at least 2.42×10^{10} n/cm^2, which is equivalent to exposure to natural background neutron radiation at sea level for > 300,000 years (calculated for New York city). The test team developed designs which were used to detect anomalous behavior indicative of changes in FPGA functionality. Changes in functionality are called logic errors or single event functional interrupts (SEFIs). Because these changes remain until detected and cleared, they are referred to as firm errors. Because of redundancy in FPGA routing architectures, not every configuration upset causes a logic error (SEFI).

The testing demonstrated that Actel ProASIC3 Flash-based FPGAs are not subject to loss of configuration due to neutron effects as expected. They also demonstrated that both of the SRAM-based FPGA architectures are vulnerable to configuration loss due to neutron effects, and provided an indication of how frequently a configuration upset results in a logic error in each SRAM FPGA. The results are documented in Table 1. The failure rates are shown in failures in time (FITs). One FIT is defined as one failure in 10^9 hours. Therefore, a FIT rate of 732 equates to 732 configuration failures where the FPGA ceased operating as intended in 10^9 hours. Integrated circuits typically have FIT rates lower than 100. In high-reliability applications, component engineers will look for overall FIT rates in the range of about 30. It is clear that the FIT rates for SRAM FPGAs, particularly if used at high altitudes, are significantly worse than required.

Table 1: **Rates of Functional Failure Arising From Neutron-Induced Configuration Upsets (firm errors)**

Vendor	Device	Firm Error FIT Rates, per Mbit of Configuration Memory	Firm Error FIT Rates, Per Device			
			Sea Level	5,000 Ft	30,000 Ft	60,000 Ft
Actel	A3PE600	No Failures Detected	No Failures Detected	No Failures Detected	No Failures Detected	No Failures Detected
Altera	EP2S30	165	1,591	5,469	235,718	751,062
Altera	EP2C20	188	732	2,516	108,439	345,518

JESD-89 describes how neutron flux increases as altitude increases, up to a maximum at 60,000 feet. This was used to calculate the failure rates for the altitudes that are listed in Table 1. A failure in the configuration memory in an SRAM FPGA is a potentially catastrophic event which can result in the FPGA operating in an unpredictable and uncontrollable manner. In existing SRAM FPGAs these effects can be

prevented only by the use of a triple module redundant implementation, which requires three copies of each FPGA with a neutron-immune majority vote circuit that monitors the outputs of all three FPGAs.

The testing also monitored each FPGA for indications of latch-ups. A latch-up can occur when a parasitic diode in the silicon substrate becomes forward-biased, causing it to conduct large amounts of current. Latch-ups are very significant because they can cause serious and permanent damage to an integrated circuit. Even if they are not destructive, they may require power to the integrated circuit to be cycled in order to clear the latch-up. This obviously presents an unacceptable situation in a high-reliability or high availability application. Two instances of bursts of logic errors concurrent with excessive increases in current consumption were detected in the Altera Stratix2 devices. This is consistent with latch-up.

In addition to these catastrophic failure mechanisms, the latest series of tests also investigated the occurrence of data upsets in flip-flops, combinatorial logic and embedded user-accessible memory. These upsets typically affect only single bits of data and can be prevented or corrected by the use of error detection and correction codes, parity bits, and CRC (cyclic redundancy checks). It was determined that all of the devices tested had approximately equal susceptibility to data upsets in flip-flops and embedded user-accessible memory. Actel ProASIC3 FPGAs showed a higher susceptibility on a per-MBit basis in the embedded memory than the two Altera products (Table 2), but as discussed, errors of this type are easily remedied. Note that a FIT rate of 175 per device in this case means that in one device, in 1 billion hours of operation, a total of 175 single-bit data errors could be expected in the memory. Transient errors in the combinatorial logic occurred too rarely to allow calculation of a meaningful FIT rate for any of the devices tested.

Table 2: **Rates of Neutron-Induced Data Upsets (Sea Level, New York)**

Vendor	Device	Flip-Flop SEU FIT Rates		Embedded Memory SEU FIT Rates	
		Per Million Flip-Flops	Per Device	Per Mbit	Per Device
Actel	A3PE600	889	12	1,580	175
Altera	EP2S30	329	9	493	656
Altera	EP2C20	613	11	770	164

The FIT rates in Table 2 are shown for sea level at New York city. FIT rates at other altitudes can be calculated using the altitude multiplication factor described in JESD-89. The multiplication factors for some commonly-used altitudes are shown in Table 3.

Table 3: **Altitude Multiplication Factors**

Altitude (Ft.)	Multiplication Factor From Sea Level
5,000	3.4
30,000	146
60,000	471

Conclusion

Neutrons arising from atmospheric collisions of galactic cosmic particles pose a significant reliability risk for many different types of high-reliability and high availability electronic equipment, both airborne and ground-based. SRAM-based FPGAs use SRAM cells to store the configuration data that gives the devices their functionality. An upset to one of these SRAM cells could potentially result in the FPGA losing its configuration. When this happens, it may cause the host system to malfunction.

Testing of data upsets in embedded user memory and data flip-flops indicated that all of the devices tested had roughly the same degree of sensitivity. Single bit errors in user memory and data flip-flops are easily mitigated.

The latest radiation testing data has shown that Actel Flash-based ProASIC3 FPGAs are not subject to loss of configuration due to neutron-induced upsets. This makes them eminently suitable for applications—both ground-based and airborne—where high reliability is imperative.

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