SET Characterization and Mitigation in RTAX-S Antifuse FPGAs

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Abstract—Heavy-ion test results utilizing novel test methodologies of non-volatile antifuse-based FPGAs are presented and discussed. In particular, the programmable architectures in the RTAX-S FPGA-family including the I/O structures, and the FPGA core were tested and their cross-sections measured. Previously available SET mitigation solution based on SET filtering was implemented on the RTAX-S test designs and their efficacy proven to reduce the saturation cross-section and increase the LET threshold of the mitigated test designs.[1] [2]

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1. INTRODUCTION

Radiation effects on high-scaled integrated circuits could disrupt the normal operation of any integrated circuit if it is not hardened by design or by embedded fault-tolerance techniques. Among these effects, a Single Event Upset (SEU) that can flip the content of a sequential element and a Single Event Transient (SET) that can induce an SEU in a memory element if the SET is clocked into the memory. The ACTEL RTAX-S 0.15-µm Space-Flight Field Programmable Gate Array (FPGA) family has been hardened by design for SEU by employing Triple Module Redundancy (TMR) on all of its register cells (R-Cell); it is also enhanced with a self-refreshing mechanism so that no accumulation of two SEUs in a TMR'd R-cell could occur between clock pulses. However, no embedded hardwired SET mitigation was implemented in the Combinational-Cells (C-Cells) of these FPGAs. Recent radiation testing performed by the radiation group of NASA-Goddard showed observable SET-cross-sections even at low and medium frequencies (15 and 30 MHz) and with increased SET sensitivities as the operating frequency is increased [1]. On the other side, Gaisler engineers did not observe any error in Cf252 beam on the FT-LEON3 when implemented on an RTAX2000S, using approximately 50 % of the FPGA resources and running at 20 MHz for approximately 168 hours [2].

This paper will target primarily a comprehensive SET characterization and mitigation of the RTAX-S FPGA family (RTAX250S-CQ352 and RTAX2000S-CQ352), mainly the FPGA core and the IO blocks when configured with two IO standards (LVDS 2.5 and LVCMOS 2.5). SET characterization for the RTAX-S FPGAs is mainly based on previously employed test techniques for the ACTEL ProASIC3 Flash-based FPGA family [3]. This characterization allows the measurements of the SET cross-section of a single C-Cell and the maximum resulting SET pulse widths in an RTAX-S FPGA. Furthermore, this paper will present two SET mitigation techniques, based on SET

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[1] 978-1-4244-2622-5/09/$25.00 ©2009 IEEE.
[2] IEEEAC paper #1421, Version 3, Updated November 2, 2008

filtering at the input of a TMR'd sequential cell, in heavy-ion beams [3-7]. They are derived from some of the previously presented mitigation solutions in [3], in particular the techniques using the guard-gate cells (with temporal delay of the logic C-Cells) and for the first time new re-routing mitigation solutions (to filter SETs), with no additional hardware overhead but a slight time penalty (less than the maximum SET pulse width). The details of these mitigation approaches as well as their efficacy in mitigating all SET effects in beam will be demonstrated and presented.

Heavy-ion-beam tests were performed on several campaigns at the Lawrence Berkeley National Laboratories with a wide heavy-ion (HI) cocktail (Neon, Argon, Cupper, Krypton and Xenon) at normal incidences and two additional tilt angles (30 and 45). No testing with rolling angles was performed or differentiation in the data between the data collected at normal incidence or tilt angles is provided in this paper. The test results are reported and discussed along with additional suggestions on mitigation methodologies suitable for the target device.

2. Devices Under Test and Test Setup

DUT

Actel RTAX-S architecture, derived from the A54SX-A architecture, has been designed for high performance and total logic module utilization as shown in Fig. 1. Unlike traditional FPGAs, the entire floor of the RTAX-S device is covered with a grid of logic modules. The RTAX-S family uses a metal-to-metal antifuse programmable interconnect element that resides between the upper two layers of metal. This eliminates the channels of routing and interconnect-resources between logic modules, as implemented on traditional FPGAs, and enables this type of architecture. The antifuses are normally open circuit and, when programmed, form a permanent, passive, low impedance connection, leading to fast signal propagation. In addition, the extremely small size of these interconnect-elements gives the RTAX-S family abundant routing resources [8].

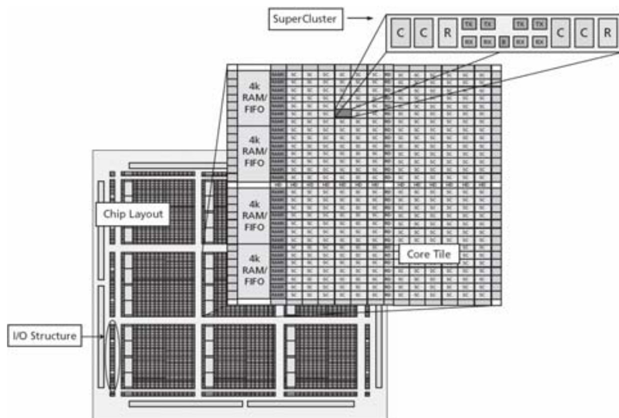

Figure 1 – RTAX-S FPGA Block Diagram Architecture

Actel's RTAX-S family provides two types of logic modules: the register cell (R-cell) and the combinational cell (C-cell). The C-cell can implement more than 4,000 combinational functions of up to five inputs (Fig. 2) with carry logic for the implementation of arithmetic functions. While each SEU-hardened R-cell appears as a single D-Type flip-flop to the user, each is implemented in silicon using triple redundancy.

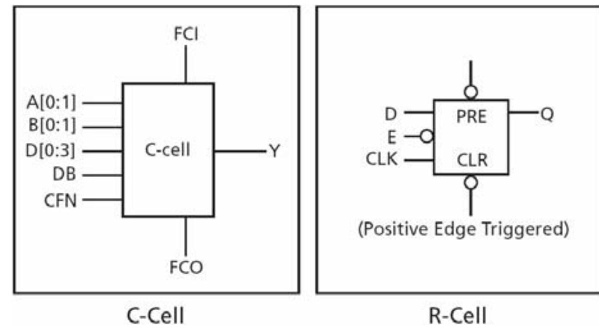

Figure 2 – C & R-Cell Block Diagram Architecture

Each TMR R-cell consists of three master-slave latch pairs, each with asynchronous self-correcting feedback paths. The output of each latch on the master or slave side votes with the outputs of the other two latches on that side. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents that change from feeding back and permanently latching. Care was also taken in the layout to ensure that a single ion strike could not affect more than one latch (Fig. 3). The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and active-low enable control signals (Fig. 2). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while conserving clock resources.

The clock source for the R-cell can be chosen from the hardwired clocks, routed clocks, or internal logic. Two C-cells, a single R-cell, and two Transmit (TX) and two Receive (RX) routing buffers form a Cluster, while two Clusters comprise a SuperCluster (Fig. 1). Each SuperCluster also contains an independent Buffer (B) module, which supports buffer insertion on high-fanout nets by the place-and-route tool, minimizing system delays while improving logic utilization. The logic modules within the SuperCluster are arranged so that two combinational modules are side-by-side, giving a C–C–R – C–C–R pattern to the SuperCluster. This C–C–R pattern enables efficient implementation (minimum delay) of two-bit carry logic for improved arithmetic performance.

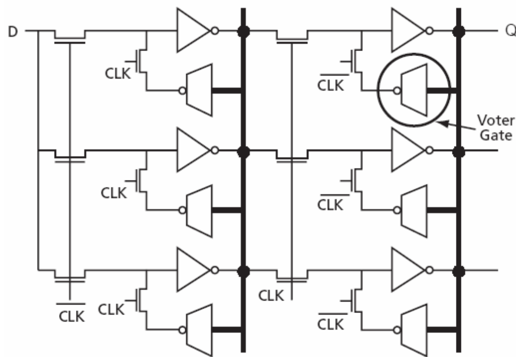

Figure 3 –R-Cell Implementation Using Voter Gate Logic

For the beam test experiments, two devices from the RTAXS product family were selected: the RTAX250S and the RTAX2000S. Each selected part is in a CQ352 package. Table 1 shows the features of the two selected parts. The test primarily targets three configurable architectures in the A3P FPGA: 1) the I/O structures, single-ended (SE) and low voltage differential signal (LVDS), 2) the FPGA Core, and 3) the Clock Network mainly the four hardwired clocks (HCLK) and the four routed clocks (RCLK).

Table 1. Features of the Selected Parts

Part	RTAX250S	RTAX2000S
System Gates	250K	2M
R-Cells	1408	20160
RAM Kbits	54K	288K
Secure (AES) ISP	Yes	Yes
Clocks (Hardwired & Routed)	4 H and 4 R	4 H and 4 R
I/O Banks	8	8
User IOs	198	840

Experimental Test Setup

A new test setup was built for the RTAX-S radiation testing. It includes three boards: 1) a “master” board for the monitoring and control of the DUT operation in-beam and 2) a daughter-board that routes the DUT IOs to the motherboard IO connectors and 3) a “slave” board for the communication between the host PC and the master board through two USB ports. The “master” board includes an A3P1500-FG484, called “master” FPGA, while the daughterboard includes a socket for an RTAXS-CQ352. The slave board includes an A3P1000-PQ208; it allows the data acquisition and data transfer to the host PC.

IO “channels” of an input (SE or LVDS) routed immediately to a nearby output are also added between the “master” FPGA and the DUT mainly for IO testing. There are 10 SE and 44 LVDS I/O channels on the master FPGA and the DUT FPGA. This type of board architecture allows the implementation of several separate designs on the same DUT to be tested simultaneously.

For communication with the host PC, a generic user interface was designed to communicate with the slave board. The communication protocol between the slave board and the host PC remains always the same for easy and fast implementation of any new SEE test experiment, always with a maximum of 64 display counters available to the designer, which functions are adjustable according to the running experiments. These counters are usually used for display of number of SEE events among other indicators of the operation of the DUT design. More details about this user interface are given in [6].

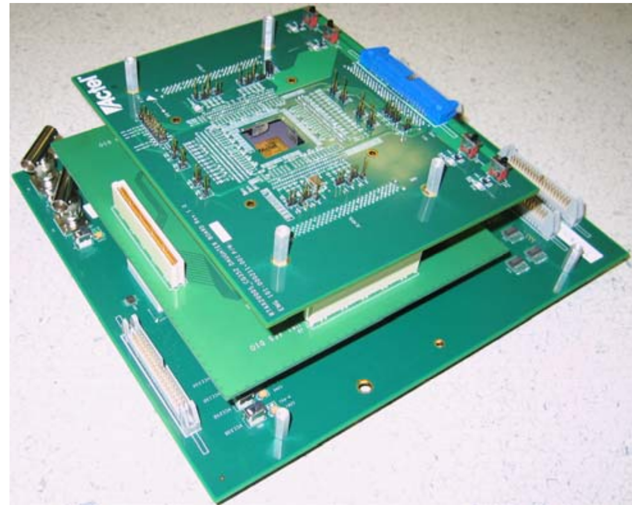

Figure 4 – Experimental Test-Setup

3. Test Designs and Experimental Results

IOs SET Characterization

Test Design

Two IO standards have been targeted for beam testing: LVCMOS2.5 (Low Voltage CMOS operating at 2.5V) and LVDS25 powered at 2.5V. The DUT FPGA is configured with designs that implement 10 short SE “channels” of an input routed immediately to a nearby output, and 44 LVDS IO channels routed also in the same manner. Using pins in close physical proximity minimizes the routing structures. The IO test design was tested at four different frequencies (6, 30, 60 and 90 MHz). Fig. 5 illustrates the test design for ten single-ended IO channels.

The radiation test results given in Figures 6 and 7 show higher sensitivities to SET for LVDS IO channels compared to the SE IO channels. In addition and as expected, for both channel-types (LVDS and SE), the SET cross-sections increased with the design’s frequency. Furthermore, as shown in Fig. 6 and only for the LVDS IO channels, a global error was observed for each IO bank, and was measured at around 4.36x 10^{-7} cm^2/(IO-Bank). The WEIBULL parameters used for the drawing and later on for the error-rate predictions are given in Tables 2 and 3.

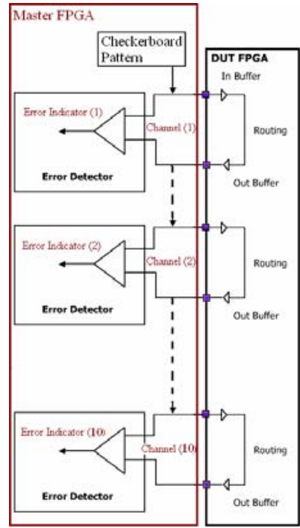

Figure 5 –Test Design of the IO Structures

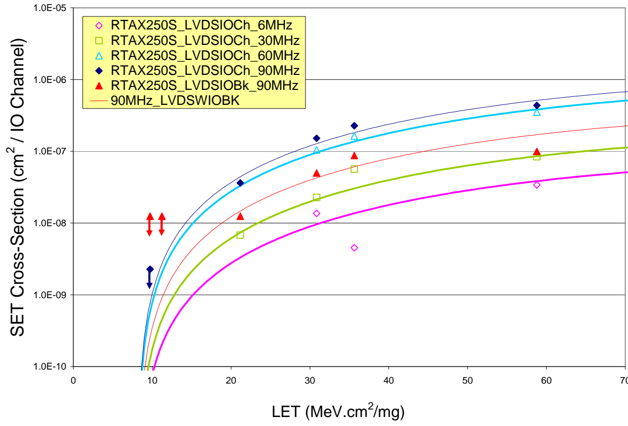

Figure 6 – SET Cross-Sections for the LVDS IO Channels vs. Frequency

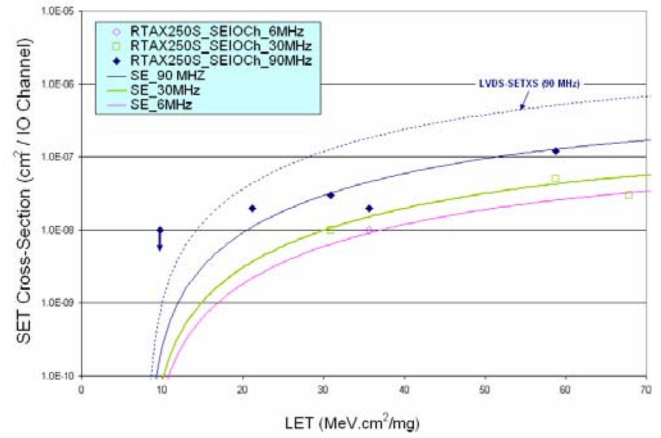

Figure 7 – SET Cross-Sections for the SE IO Channels vs. Frequency

Table 2. WEIBULL Parameters of Single-Ended IO Channels (RTAX250S-LVCMOS25)

Frequency [MHz]	S	W	Limit [cm^2/IO-Ch]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/IO-Ch]
6	2	6	6E-8	8	$9.74 < LET_{th} < 21.17$	3.39E-8
30	2	8	1E-7	8	$9.74 < LET_{th} < 21.17$	5.65E-8
90	2	6	3E-7	8	$9.74 < LET_{th} < 21.17$	1.69E-7

Table 3. WEIBULL Parameters of Differential IO Channels (RTAX250S-LVDS25)

Frequency [MHz]	S	W	Limit [cm^2/IO-Ch or IO-Bk]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/IO-Ch or IO-Bk]
6	2	68	9E-8	8	$9.74 < LET_{th} < 21.17$	5.08E-8
30	2	68	2E-7	8	$9.74 < LET_{th} < 21.17$	1.13E-8
60	2	68	9E-7	8	$9.74 < LET_{th} < 21.17$	5.08E-7
90	2	68	1.2E-6	8	$9.74 < LET_{th} < 21.17$	6.77E-7
IO-Bank	2	68	4E-7	8	$9.74 < LET_{th} < 21.17$	2.26E-7

HCLK and RCLK SET Characterization

Test Design

To estimate worst-case cross-sections for the HCLK and RCLK networks, a static test design for the clock structures was implemented and is shown in Fig. 8. In the DUT design, four hardwired clocks (HCLK) and two routed clocks (RCLK) were each connected to three R-Cells. Having seen the RTAX-S schematics, we made sure that most of the clock structures (buffers, multiplexers, etc.) are used in this design. Because of the lack of statistics, HCLK and RCLK cross-sections were combined. The resulting SET cross-sections for an HCLK/RCLK for both of the RTAX250S and the RTAX2000S are given in Fig. 9. The WEIBULL parameters used for Fig. 9 and later on for the error-rate predictions are given in Table 4.

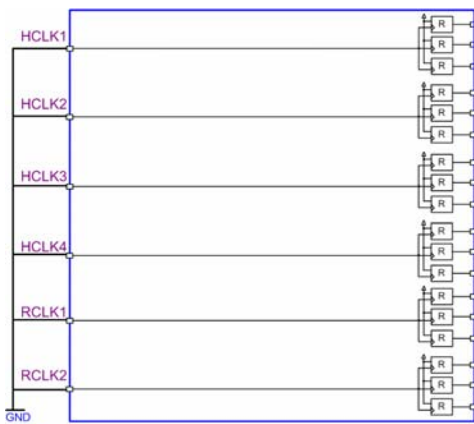

Figure 8 – Static SET Characterization of the HCLK and RCLK in RTAX2000S

The radiation test results given in Fig. 9 show slightly higher SET sensitivities for the RTAX2000S compared to the RTAX250S at LET lower than 50 MeV.cm^2/mg and vice versa at higher LET. This could be due to the higher number of logic gates in the clock networks in the RTAX2000S than in the RTAX250S leading to higher cross-sections in the RTAX2000S case. There is no clear explanation to the higher cross-section of the RTAX250S compared to the RTAX2000S at LET 60 MeV.cm^2/mg. It could be simply due to the lack of statistics or to the two competing phenomenon on the clock networks: 1) the higher clock loads in the RTAX2000S relatively to the RTAX250S inducing natural SET filtering and 2) the increase of SET pulse widths with the LET increasing consequently their SET rates. It is possible that at very high LET, SET pulses are wide enough so fewer SETs are filtered due to higher loading on the clock network. Based on this assumption, SETs on highly loaded designs should be reduced. It is hard to prove which one of these two phenomenons is mostly affecting the SET rates. The lack of statistics does not allow us to decide between them.

Furthermore, in a given design where HCLK and RCLK are used to clock a design, their effective cross-section should be a fraction of the ones given in Fig.10. Indeed, in a real design, the duty cycles of the transferred data between consecutive R-Cells should be taken in account. For instance, if the transferred data between two R-Cells is toggling at half the rate of the clock frequency, then these cross-sections should be divided by two. This will be shown in the remainder of this paper, when testing a shift register design where the data is toggling at half of the clock frequency.

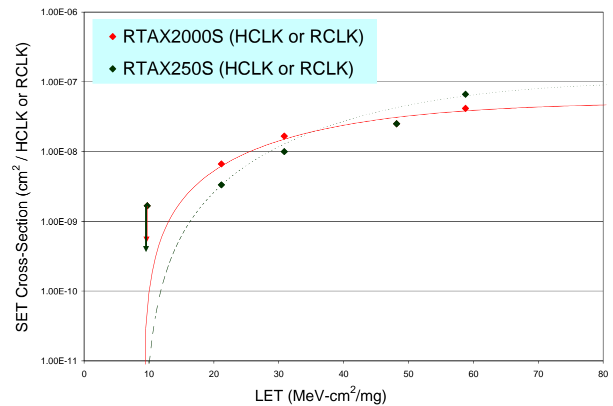

Figure 9 – SET Cross-Sections for HCLK and RCLK

Table 4. WEIBULL Parameters of HCLK and RCLK (LVTTL Standard)

RTAX-S	S	W	Limit [cm^2/IO-Ch]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/IO-Ch]
RTAX250S	2.4	50	1E-7	9	$9.74<LET_{th}< 21.17$	6.83E-8
RTAX2000S	1.7	40	5E-8	9	$9.74<LET_{th}< 21.17$	4.15E-8

FPGA Core SEE Characterization (R-Cells)

The purpose of this testing is to determine the SEE cross-section of an R-Cell in an RTAX-S FPGA. As mentioned above, the R-Cell should be SEU immune because of the TMR implementation of all of its CMOS gates leading to the registration of an input signal. This means that in a static mode (with no clocking of the R-Cells) or at very low-frequencies, an R-Cell should not exhibit any sensitivity to radiation. However, since an R-Cell output should converge to one output-signal, the output-buffer of each R-Cell was not TMR'd and is built based on transistors having the smallest geometries of a 0.15-µm technology. Consequently, the R-Cell SEE cross-section is expected to be increasing with the frequency. This SEE cross-section is mainly due to SET on each R-Cell output buffer.

Test Design

To measure the SEE cross-sections of the R-Cells, a basic test design including four shift registers (SR), each one of them uses a set of R-Cells configured as D-Flip-Flop (DFF) and one global clock signal with no reset signals. Each of the first two sub-designs (called also channels) is using a hardwired HCLK signal while each of the two subsequent channels is using one routed clock (RCLK). To avoid software minimum delay variations, which means having a data-path faster than the routed clocks, a single C-Cell was always added at the data-input of each R-Cell. More details about the mitigation to minimum delay variations in the RTAX-S FPGA are given in [9]. A detailed block diagram of the test design implementation is given in Fig. 10.

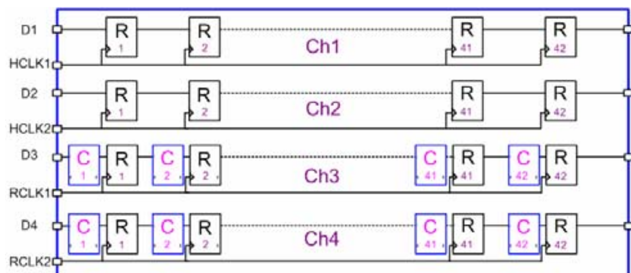

Figure 10 – Block Diagram of the R-Cells Test Design Implemented on an RTAX250S

The testing was performed at the clock frequencies of 6, 60 and 120 MHz. It should be mentioned that implementing the same design on several channels will help check the repeatability and the consistency of the tests for its non-dependency of different tested channels. Moreover, it allows checking for SEE on common global signals other than the user global clock and reset signals. Since all IOs were using single-ended IOs, global errors were observed only on the HCLK and RCLK signals.

Heavy Ion Beam Test Results

The SR test design was implemented on two DUTs: RTAX250S (with 42 R-Cells in each channel) and RTAX2000S (with 302 R-Cells/Channel). For the SR test design implemented on the RTAX250S, the obtained results show two types of errors: 1) single error on one channel, and 2) single or multiple errors on all the design-channels associated to a common HCLK or RCLK global signal. All errors were transient and did not require any reconfiguration or power cycle of the FPGA. Type 1 is most likely due to an SET in the R-Cell output buffer. Type 2 could be due to the clock signal and its cross-section as expected and mentioned above is half of the cross-section given in Fig 9, demonstrating the duty cycle effect on the reduction of the clocks cross-sections. Fig. 11 shows the single R-Cell cross-sections at three different frequencies (6, 60 and 120 MHz) obtained from the test data. Note that for better visibility and lack of data points for the test data at 6 MHz; WEIBULL curves in Fig. 11 (also in Fig. 14) have been drawn only for the 60 and 120MHz data.

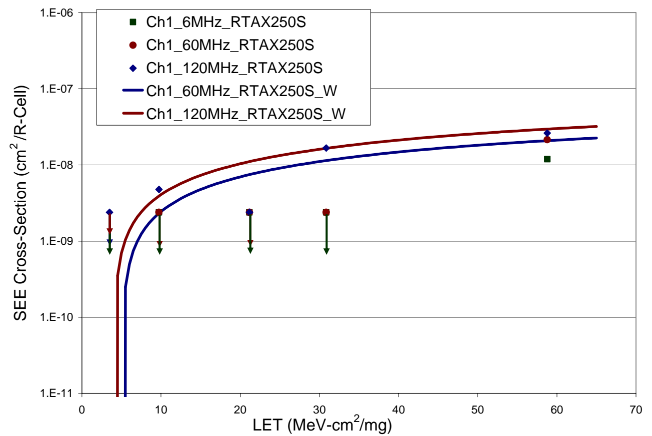

Figure 11 – SEE Cross-Sections for an RTAX250S R-Cell vs. Frequency

Table 4. WEIBULL Parameters of SET on a Single R-Cell in RTAX250S

Frequency [MHz]	S	W	Limit [cm^2/R-Cell]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/R-Cell]
60	1	100	5E-8	4	$3.49<LET_{th}<9.74$	2.39E-8
120	1	100	9E-8	4	$3.49<LET_{th}<9.74$	4.35E-8

The data shows almost no sensitivity at 6 MHz till an LET of 58.78 MeV.cm^2/mg, proving the efficacy of the TMR implementation in mitigating SEU. Note that more beam data is needed to show the actual SEE cross-sections at 6 MHz. If the R-Cells were tested in the static mode, with no clocking of the R-Cells, no errors would have been

observed on the R-Cells. However, when the clock frequency was increased, the SEE cross-sections mainly attributed to SET on the R-Cells' output-buffers, reached a saturation-cross-section of 4.29×10^{-8} cm^2/R-Cell.

Furthermore, the obtained beam data at 120 MHz for the four tested channels (Fig. 12) showed no major variation with the insertion of C-Cells added to avoid minimum delay variations. This clearly proves that the resulting SET cross-sections are dominated by the R-Cell SET cross-sections at the high-frequencies and LET upto 30.86 MeV.cm^2/mg.

The same SR test design was implemented on the RTAX2000S and run at a maximum frequency of 90 MHz. The number of the R-Cells was increased from 42 to 302 per channel. As shown in Fig. 13, the beam data demonstrated a perfect linear proportionality of the SET cross-section with the design's frequency. This finding should allow the designer to predict the R-Cell cross-section at any frequency. Fig. 13 shows also an example of that prediction at 120 MHz. Furthermore, as shown in Fig. 14, lower SET cross-sections were observed for an RTAX2000S R-Cell compared to the RTAX250S. Indeed, this result was expected simply because of the higher load effects in the RTAX2000S compared to the RTAX250S which are inducing higher SET filtering effects.

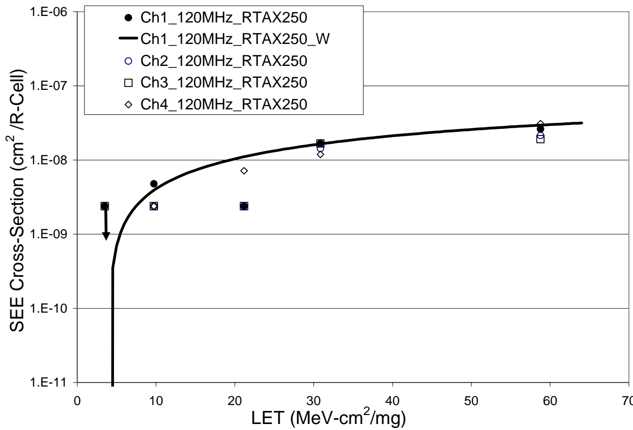

Figure 12 – SEE Cross-Sections for an RTAX250S R-Cell vs. Frequency
***when C-Cells are added to avoid minimum delay variations**

The WEIBULL parameters used to draw the figures 11 to 14 are given in Tables 4 and 5.

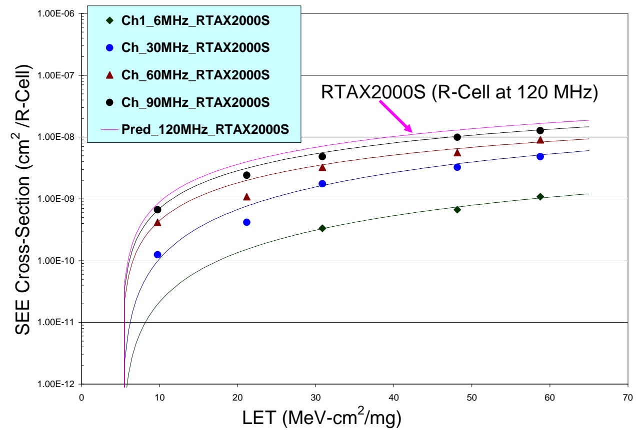

Figure 13 – SEE Cross-Sections for an RTAX2000S R-Cell vs. Frequency

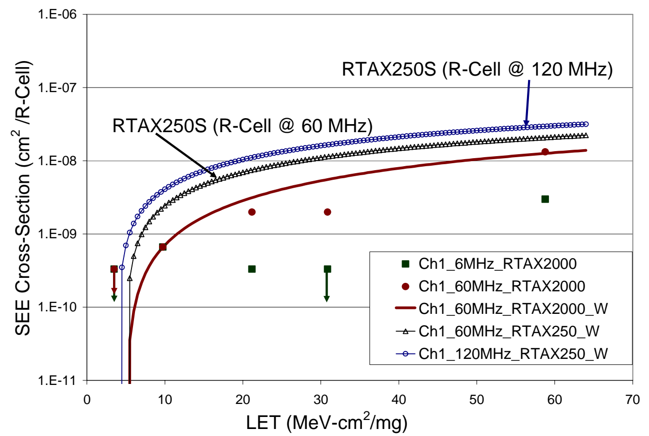

Figure 14 – RTAX250S R-Cell Cross-Sections vs. RTAX2000S R-Cell Cross-Sections

Table 5. WEIBULL Parameters of SET on a Single R-Cell in RTAX2000S

Frequency [MHz]	S	W	Limit [cm^2/R-Cell]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/R-Cell]
6	1.68	120	4.50E-9	5	$3.49<LET_{th}<9.74$	1.35E-9
30	1.68	120	2.25E-8	5	$3.49<LET_{th}<9.74$	6.76E-9
60	1.3	120	2.80E-8	5	$3.49<LET_{th}<9.74$	1.02E-8
90	1.3	120	4.40E-8	5	$3.49<LET_{th}<9.74$	1.60E-8
120_Predicted	1.3	120	5.60E-8	5	$3.49<LET_{th}<9.74$	2.03E-8

FPGA Core SET Characterization & Mitigation (C-Cells)

The purpose of this testing is to determine the SET cross-section of a given C-Cell in both of the RTAX250S and RTAXS2000S when configured as an inverter. The block diagram of the C-Cell internal architecture is given in Fig. 15. In addition, similarly to what has been done and presented in [3], the maximum SET-pulse widths were measured by insertion of variable low-pass SET filters (of SET as wide as 1 and 2 ns). More details about the employed SET filters are given in [3].

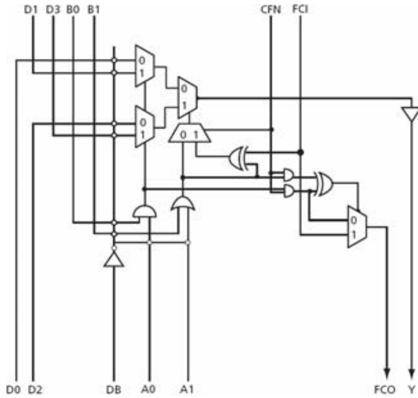

Figure 15 – RTAX-S C-Cell Internal Architecture

Test Design

Four sub-designs were implemented and are shown in Fig. 16. Indeed, being aware of the high number of capacitances available in the RTAX-S part, a fourth sub-design was added where the C-Cells configured as inverters are manually placed far from each other across the die by means of the Actel LIBERO design tools. The resulting SET cross-sections for each inverter implemented in each sub-design are given in Fig. 17 and the used WEIBULL parameters are given in Table 6.

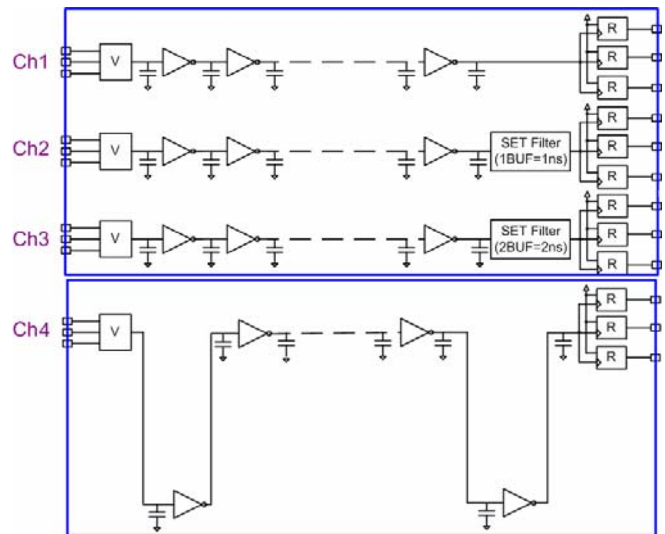

Figure 16 – SET Characterization Test Design of the RTAX-S C-Cells

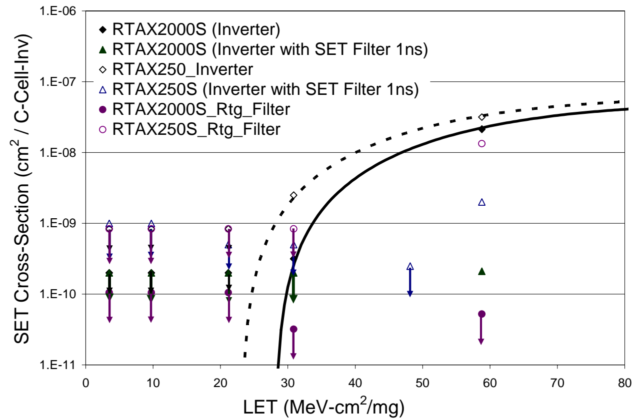

Figure 17 – SET Cross-Sections for an RTAX2000S C-Cell Configured as an Inverter

Table 6. WEIBULL Parameters of SET on a Single C-Cell-Configured as an Inverter

RTAX-S	S	W	Limit [cm^2/C-Cell]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/C-Cell]
RTAX250S	2	40	6E-8	23	$21.17 < LET_{th} < 30.86$	5.21E-8
RTAX2000S	2	40	5E-8	28	$21.17 < LET_{th} < 30.86$	4.08E-8

Heavy Ion Beam Test Results

In Figure 17, the beam data showed a relatively high LET threshold for SET in a C-Cell configured as an inverter compared to the R-Cells. For an SET cross-section lower than 10^{-11} cm^2/C-Cell, the LET is around 22 MeV.cm^2/mg for the RTAX250S and 28 MeV.cm^2/mg for the RTAX2000S. Furthermore, the saturation cross-section of a single C-Cell in the RTAX250S is around the 4.96×10^{-8} cm^2/C-Cell, while for the RTAX2000S, it is around the 3.17×10^{-8} cm^2/C-Cell.

Having checked the internal schematics of both parts (RTAX250S and RTAX2000S), the C-Cells dimensions are identical in the RTAX250S and RTAX2000S. But, although they are identical in both parts, the test designs used to test them are very different. Indeed, by increasing the number of inverters from 120 to 950, the test design implemented in the RTAX2000S crossed on average four more high-capacitance columns and three more rows, which were filtering some of the SETs. Consequently, most of the SET that have narrow pulse-widths have been filtered. As a result, both of the LET threshold and the saturation cross-

section of the RTAX2000S have decreased. Although, this filtering effect is typical in a real design since the C-Cells are usually placed and routed by the LIBERO software tool, one should be conservative and consider the RTAX250S SET measurements as the worst-case for both FPGAs. For even more conservative SET measurements, the user should implement these inverters in one set of rows and columns in such a way that there will be no crossing of the high capacitance vertical and horizontal lines.

Furthermore, as shown in channels 2 and 3, all observed SET on the inverter-C-Cells were shorter than 1 ns upto an LET of 30.86 MeV.cm^2/mg (Xe ions) and always shorter than 2 ns at all LETs including those of the Xenon heavy-ions. Moreover, SETs with a pulse wider than 1 ns are ten times less frequent in the RTAX2000S than in the RTAX250S, most likely because of the SET filtering due to the placement of the higher number of inverters.

On the other side, no errors were observed on channel 4 showing the strong RC filtering effects naturally available in the RTAX-S FPGAs. Note that most of the user designs are routed by the Libero software tools and therefore are often placed far from each other favoring a spontaneous SET filtering. The SET cross-sections corresponding to the worst-case are obtained nevertheless from the SET cross-section of Ch1. Indeed, since all inverters were placed right next to each other, all SETs were captured by the R-Cells if their pulse widths are higher than the R-Cell setup-time and this independently of the design's frequency.

In real designs, the cross-sections of the SET inducing SEU in the following R-Cells should be lower than the SET cross-section calculated in Ch1 because of the impact of the design's frequency, the design's placement and the C-Cell configuration if its setup-time is higher than the inverter setup-time. Table 7 provides a summary of the observed SEE cross-sections in the RTAX2000S programmable circuits and their corresponding orbital error rates.

Table 7. GEO Orbital-Error Rate Predictions and Radiation Sensitivities of the RTAX2000S Features

RTAX2000S	Frequency [MHz]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/C-Cell]	GEO Orbital Error Rate [Error/Cell/Day]	GEO Orbital Error Rate for RTAX2000S @120 MHz
R-Cell	120	$9.74<LET_{th}<21.17$	1.60E-8	4.75E-9	**1.75**/RTAX2000S/100 years
C-Cell	-	$21.17<LET_{th}<30.86$	4.08E-8	4.19E-10	**1.5**/RTAX2000S/1000 years
SE IO-Channel	90	$9.74<LET_{th}<21.17$	1.69E-7	1.96E-8	**1.96E-8** /SE IO-Ch/Day
LVDS IO-Channel	90	$9.74<LET_{th}<21.17$	6.77E-7	1.25E-7	**1.25E-7** /LVDS IO-Ch/Day
LVDS IO-Bank	90	$9.74<LET_{th}<21.17$	2.26E-7	2.93E-8	**2.93E-8** /LVDS IO-Bk/Day
HCLK or RCLK	-	$9.74<LET_{th}<21.17$	4.15E-8	5.22E-9	**5.22E-9** /HCLK or RCLK/Day

4. FPGA CORE SEE MITIGATION

Test Design

The purpose of this testing is to determine the worst-case of SEE cross-sections of a given test design in the RTAX2000S when combining the R-Cells with the C-Cells. For these purposes, a shift register combining R-Cells with C-Cells was implemented. It included 202 R-Cells, operated at 60/120 MHz where ten/four inverter-C-Cells are inserted between each two R-Cells as shown in Fig. 18. In addition, two mitigation solutions were tested. The first one uses an SET filter similar to what has been implemented for the SET characterization of the RTAX-S C-Cells and as previously shown in Fig. 13. Each SET Filter includes a majority voter with a feedback path connecting its output to one of its inputs and a delay element which is a C-Cell configured as a buffer. To allow insertion of the SET filter between the inverter-string and each R-Cell, while keeping the same frequency, the number of inverters was reduced from ten to eight when operating the design at 60 MHz and from four to three when operating the design at 120 MHz. These test designs were implemented on an RTAX2000S.

Furthermore, a second mitigation design invoking the routing filter approach was implemented where each last C-Cell in an inverter-string between two consecutive R-Cells is placed far away from the next R-Cell. That spacing is adding at least a delay of 2 ns (based on the smart tool output). Figure 19 shows an example of that spacing. Although this design could barely run at 120 MHz, we have preferred running it at 90 MHz to avoid any added violations in the timing constraints and to make sure that the beam data is accurate as possible.

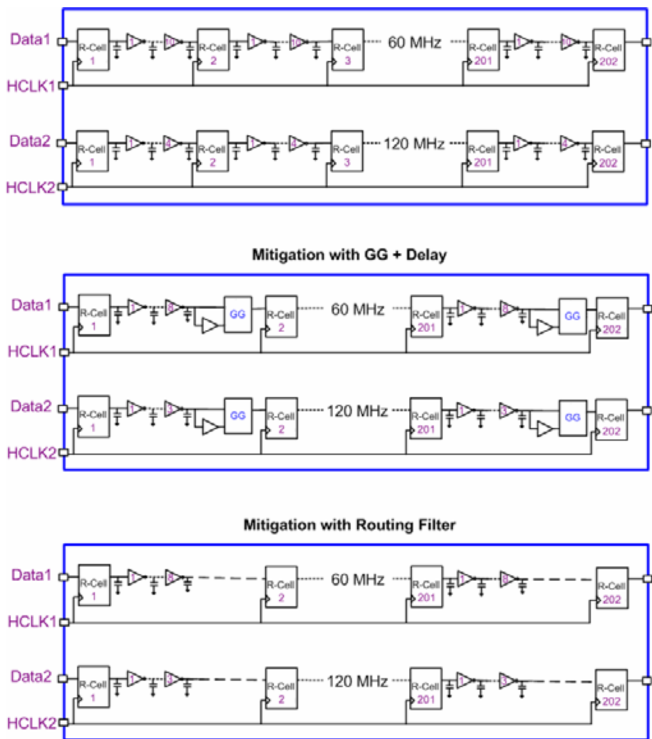

Figure 18 – SEE Characterization of Test Designs similar to Real Test Designs

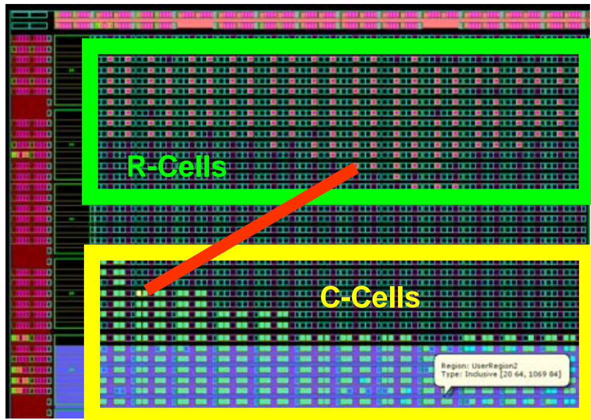

Figure 19 –Example of the Spacing of the R-Cells from the C-Cells for the Routing Filter Implementation on the RTAX2000S operated @ 120 MHz

Heavy Ion Beam Test Results

As shown in Figures 20 and 21, the SEE cross-sections of an R-Cell combined with the ten/four C-Cells that precede it in the non-mitigated design (TD3_No Mitigation) when running at 60/120 MHz is very similar to the SEE cross-section of a single R-Cell in the RTAX-S previously given in Fig. 13. This similarity is valid till an LET of 30.86 MeV.cm^2/mg. Indeed, it is clear that the resulting SET cross-section of an R-Cell with ten/four C-Cells is dominated by the SET cross-section of the R-Cell itself. Moreover, for LET that are lower than 20 MeV.cm^2/mg, the C-Cells themselves were filtering the SET disturbing the R-Cells' output-buffers. SET effects on the C-Cells are however clear starting from an LET of 30.86 MeV.cm^2/mg. This result was expected from the C-Cells' SET characterization shown previously in Fig. 17.

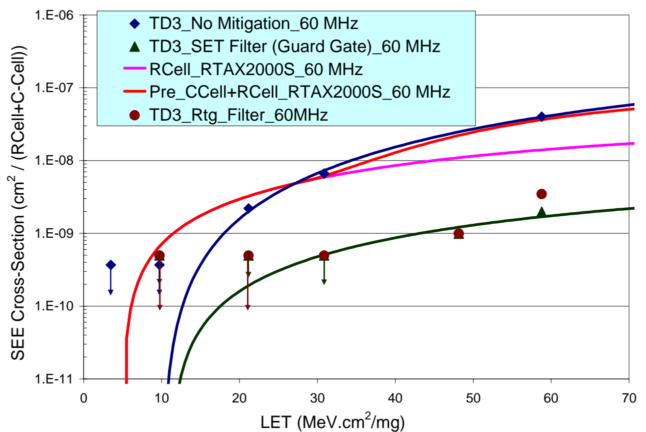

Figure 20 – SEE Cross-Sections for a Non-Mitigated & Mitigated Test Design on an RTAX2000S

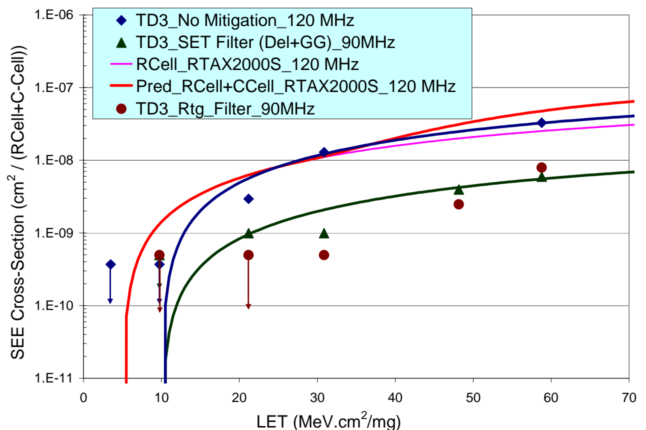

Figure 21 – SEE Cross-Sections for a Non-Mitigated & Mitigated Test Design on an RTAX2000S

Table 8. WEIBULL Parameters of R-Cell used with C-Cells-Configured as Inverters

Design	Frequency [MHz]	S	W	Limit [cm^2/C-Cell]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/C-Cell]
With No Mitigation	60	2.1	100	2.0E-7	10	$9.74<LET_{th}<21.17$	5.79E-8
With No Mitigation	120	1.3	100	1.0E-7	10	$9.74<LET_{th}<21.17$	6.39E-8
With Mitigation (GG + Delay)	60	1.5	100	6.0E-9	10	$9.74<LET_{th}<21.17$	2.19E-9
With Mitigation (GG + Delay)	120	1.3	100	1.7E-8	10	$9.74<LET_{th}<21.17$	6.84E-9

Furthermore, for the mitigated design with an SET filter of one nanosecond, errors were observed only starting from an LET of 48.15 MeV.cm^2/mg when running the design at 60 MHz, and the saturation cross-section was reduced by an order of magnitude compared to the non-mitigated design. When running the design at 90 MHz, errors were observed starting from an LET of 20.17 MeV.cm^2/mg. This shows clearly the efficacy of both mitigation solutions, since they can lead to extremely low orbital error rates, leading to low area overhead and time penalty.

Note that the cross-section of the mitigated design with delay and GG is expected to increase with the frequency because of the SET filter sensitivity to SET, since its majority voter constitutes a single point failure. Table 9 shows the used WEIBULL parameters for Figures 20 and 21. While Table 10 provides the derived orbital error-rates for both mitigated and non-mitigated designs at both frequencies (60 and 120 MHz) as well as a the estimated error rates of an RTAX2000S shift-register design operated at 120 MHz, using 100% of the C-Cells and 50 % of the R-Cells, where four C-Cells are always inserted between each two consecutive R-Cells.

Table 9. WEIBULL Parameters of R-Cell used with C-Cells-Configured as Inverters

Design	Frequency [MHz]	S	W	Limit [cm^2/C-Cell]	Onset [MeV.cm^2/mg]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/C-Cell]
Without Mitigation	60	2.1	100	2.0E-7	10	$9.74<LET_{th}<21.17$	5.79E-8
Without Mitigation	120	1.3	100	1.0E-7	10	$9.74<LET_{th}<21.17$	6.39E-8
With Mitigation (GG + Delay)	60	1.5	100	6.0E-9	10	$9.74<LET_{th}<21.17$	2.19E-9
With Mitigation (GG + Delay)	120	1.3	100	1.7E-8	10	$9.74<LET_{th}<21.17$	6.84E-9

Table 10. RTAX2000S Radiation Summary

RTAX2000S	Frequency [MHz]	LET_{th} [MeV.cm^2/mg]	Saturation Cross-Section [cm^2/Cell]	GEO Orbital Error Rate [Error/Cell/Day]	GEO Orbital Error Rate for RTAX2000S @120 MHz
Without Mitigation	120	$9.74<LET_{th}<21.17$	5.79E-8	5.21E-9	**1.9**/RTAX2000S/100 years
With Mitigation (GG + Delay)	90	$21.17<LET_{th}<30.86$	6.84E-9	2.11E-10	**7.76**/RTAX2000S/1000 years
With Mitigation (Routing Filter)	90	$21.17<LET_{th}<30.86$	7.92E-9	2.36E-10	**8.68**/RTAX2000S/1000 years
LVDS IO-Bank	90	$9.74<LET_{th}<21.17$	2.26E-7	2.93E-8	**2.93E-8** /LVDS IO-Bk/Day
HCLK or RCLK	-	$9.74<LET_{th}<21.17$	4.15E-8	5.22E-9	**5.22E-9** /HCLK or RCLK/Day

5. Conclusion

A full SEE characterization at high-frequencies (up to 120 MHz) has been performed on the RTAX-S antifuse-based FPGA family. The obtained results are presented and showed little SET sensitivity in most of the programmable architectural features of the FPGA. The R-Cell cross-section although small was increasing with the frequency reaching 5x 10^{-8} cm^2/R-Cell when operating at high-frequencies (upto 120 MHz) for the RTAX250S and 2x 10^{-8} cm^2/R-Cell for the RTAX2000S. The C-Cells however exhibit very little SET sensitivities due to their internal architectures. Indeed, when combining the R-Cells with the C-Cells, the resulting cross-sections were very much reduced and consequently the LET_{th} of the R-Cell increased to around 20 MeV.cm^2/mg. Finally, a transient event on each IO bank used exclusively for LVDS IOs at high frequencies has been detected and its cross-section measured. This global error was never observed for SE IO channels.

In addition, all orbital error-rates with no mitigation were very low and implied that no SET mitigation is needed. For very critical missions, these SET sensitivities can be mitigated by means of SET filtering with little area overhead and time penalty.

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BIOGRAPHY

Sana Rezgui *received the B.E. (1996) from ENIT in Tunisia and the M.E. (1997) in electrical engineering from UPS in Toulouse, France and the Ph.D. (2001) in Microelectronics from INPG in France. She was a visiting researcher at JPL/NASA (2001) for transfer of technologies on I.C. testing and their error rate prediction in radiation environments. She was employed by NEE ANN Polytechnic of Singapore as a lecturer and consultant for IC testing (2002). She joined the Aerospace and Defense Group (2003) in Xilinx, Inc. and led the SEE test consortium for their FPGAs. Since 2006, she works as a principal engineer in the Technology and Development Group of Actel Corporation. She has published or co-published over 30 technical papers, in the field of radiation effects and hardening.*

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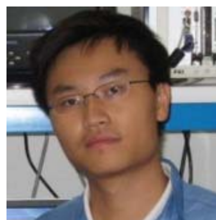

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John McCollum *worked 2 years at Faichild R&D on bipolar switching performance, specifically platinum doped life time control and the development of Ion Implantation. He worked 15 years at Intel developing Intel's first bipolar PROM, Ion Implantation, the world's first 16K DRAM, as well as 64K and 256K DRAMs. Mr. McCollum developed Intel's first dual layer metal CMOS technology for the 386 microprocessor. He co-founded Actel and worked the last 20 years on process, antifuse and flash cell development, and FPGA Architecture at Actel. He holds over 50 patents, covering Process Technology, Antifuse and NVM technology, FPGA Architecture, Analog Processing and Radiation Hardening. He has presented numerous papers at IEDM, MAPLD, CSME, SPWG, and the FPGA Symposium. He is currently a Fellow in the Technology Development Department.*