RTAX-S Testing and Reliability Update

Introduction

Actel has recently implemented enhanced procedures for the qualification and lot acceptance of the radiation-tolerant RTAX-S antifuse FPGAs. These procedures are based on extended testing using highly perceptive designs that stress antifuses within the product. It should be noted that there have been **no antifuse faults** to date, either in the commercial AX device or the radiation-tolerant RTAX-S device. Actel will continue to life test these products and use the data collected to enhance the reliability of the product. Current testing for the RTAX-S using both the Qualification Burn-In (QBI) and the Enhanced Antifuse Qualification (EAQ) now totals over 1.93 million hours of life testing for a total of 2,191 units with **no antifuse faults**. This attests to the overall reliable nature of the antifuse and hence the product. This document describes the enhanced procedures and presents results of the additional qualification and lot acceptance tests performed in conformance with the new procedures.

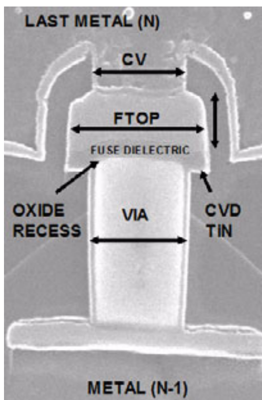
RTAX-S Technology Overview

The RTAX-S FPGA is the latest generation of radiation-tolerant metal-to-metal antifuse-based field programmable gate array devices from Actel. Predecessor product families include RT54SX, produced on 0.6 µm technology, and a shrink of these designs to produce RT54SX-S on 0.25 µm, fabricated initially at MEC and later as RTSX-SU at UMC (Table 1 and Table 2).

Table 1: **Metal-to-Metal Antifuse Space Flight FPGAs**

Product	Foundry	Process Geometry (µm)
RT54SX	MEC	0.60
RT54SX-S	MEC	0.25
RTSX-SU	UMC	0.25
RTAX-S	UMC	0.15

Table 2: **UMC Metal-to-Metal Antifuse Structure Comparison**

		SX-A (0.22 µm)	RTSX-S (0.25 µm)	Axcelerator®/RTAX-S (0.15 µm)
	CV (µm)	0.36	0.36	0.20
	FTP DOM (µm)	0.60	0.65	0.42
	FTOP AEI (µm)	0.55	0.60	0.40
	FTOP TiN Thickness (Å)	1,800~2,000	1,800~2,000	1,500
	Antifuse Dielectric Thickness (Å)	550	550	375
	CVD TiN Thickness (Å)	200	200	200
	VIA (µm)	0.36	0.36	0.22

There are three main reasons why the Antifuse structure in the RTAX-S is more robust than the Antifuse in earlier product families.

The three reasons can be outlined as follows:

- Process geometry change (from 0.6 µm to 0.25 µm to 0.15 µm)
- Antifuse structure design
- Switching current change

Process Geometry

RTAX-S is manufactured on a UMC standard 0.15 µm, seven-layer metal CMOS process with unique metal-to-metal programmable interconnect (antifuse) layers residing between the top two layers of metal. Metallization is aluminum-copper (AlCu) with Ti/TiN cladding; passivation is 5,000 Å oxide and 7,000 Å SiN. Fabrication of the layers comprising the antifuse structure is based on the same metal-to-metal antifuse structure as prior generations of antifuse devices fabricated at UMC, scaled to dimensions compatible with the 0.15 µm technology. A key element of acceptance of RTAX-S for flight applications is the demonstration that the susceptibility to changes in antifuse resistance exhibited in earlier MEC RTSX-S products is not present in RTAX-S.

Antifuse Structure Design

The antifuse structure in the RTAX-S benefits from a design and layout targeted to the use of 0.15 µm technology, in contrast to the restrictions and impacts associated with the mask level and shrink operations used to create a 0.25 µm compatible mask set from a 0.6 µm layout. The RTAX-S was designed at 0.15 µm and therefore has an optimized design for programming the antifuses. This results in a 10 to 20% increase in programming current in the critical, most highly stressed input antifuses. In addition, the antifuse structure has been scaled vertically due to the lower operating voltage (1.5 volts vs. 2.5 volts). This improves the mass transport of the plate material, as the top and bottom plate are 35% closer. Also, as the antifuse horizontal structure is scaled with the smaller geometry, the antifuse filament, which is larger as the programming current is higher, is placed into direct contact with the Tungsten plug and not off to the side, as was seen in the very few failures in the products based on 0.25 µm technology. All of the above results in more robust antifuse filaments that will tolerate higher switching currents.

Switching Current Change

Investigation of UMC 0.25 µm devices has established that the key aspect of antifuse reliability is thermal stress within the programmed antifuse that results from the flow of switching currents. These switching currents can contribute to changes in the antifuse resistance. Design provisions to reduce transient thermal stress in the antifuse have been shown to be effective in reducing the antifuse failure rate. While the programmed resistance values are lower, the peak current flowing in the antifuse is reduced in the 0.15 µm RTAX-S device. Peak current flow during logic state transitions of the buffers that drive signals through the antifuses is limited by the saturation current in the MOSFET devices; transistor saturation currents in the 0.15 µm transistors are reduced by 64% from those present in the 0.25 µm transistors. This reduction is primarily due to the reduction in the core array voltage from 2.5 V to 1.5 V. The thermal peak temperatures will be much less in the RTAX-S compared to the SX-A technology because the currents are less. SPICE simulations of Single S-antifuses have 67% I_{PEAK} during switching of the RTSX-S. In addition, the Actel Libero® Integrated Design Environment and Designer software includes S-Antifuse Loading (SAL), which eliminates in most designs the occurrence of Single S-Antifuses types in user designs. SPICE simulations of Single B-Antifuses in RTAX-S have 50% IPEAK of RTSX-SU. Dedicated buffer modules are an addition to the AX architecture and reduce the net loading on long or high fanout nets. This results in a more robust filament with a lower impedance and lower switching current (IPEAK), which results in dramatic reduction in peak temperatures when compared to the earlier product families.

Summary

The enhancements in the 0.15 µm technology have resulted in a more robust antifuse that has not shown a single antifuse failure during repeated testing with highly sensitive and perceptive tests (up to 4,000 hours at 132ºC T_J and 1.6 V V_{CCA}), similar to the ones used in the SX-A and RTSX-SU tests.

Qualification Burn-In (QBI)

This is the design that is used to qualify the RTAX-S device to the MIL-STD 883 Class B specification. The qualification process included generating a QBI design and using it to program the devices for Group C life test experiments. This design is used to test the CMOS process technology of the device and has a very high utilization of the different resources within the device such as the I/Os, combinational and sequential logic, Fast Carry Chains, FIFO, and RAM blocks. The I/Os are configured with the maximum possible different combinations of I/O standards, slew, and pull-up resistors (I/O standards LVTTL, PCI / PCI-X, LVPECL, and V_{REF} are used). The resource utilization is shown in Table 3. The results of the QBI tests are shown in Table 4.

Table 3: **QBI Design RTAX-S Resource Utilization**

			RTAX1000S-CQ352		RTAX2000S-CQ352	
Sequential	(R-cells)	Used:	5768 / 6048	95.37%	9965 / 10752	92.68%
Comb	(C-cells)	Used:	12091 / 12096	99.95%	21437 / 21504	99.69%
Logic	(R+C cells)	Used:	17859 / 18144	98.43%	31402 / 32256	97.35%
RAM/FIFO		Used:	36 / 36	100%	64 / 64	100%
I/O	w/Clocks	Used:	196 / 198	99%	196 / 198	99%
HCLK	(Hardwired)	Used:	4 / 4	100%	4 / 4	100%
CLK	(Routed)	Used:	4 / 4	100%	4 / 4	100%

Table 4: **RTAX-S QBI Test Results**

Product	Package	Wafer Lot Number	Group	Units	BI (hours)	AF Failures	Other Failures	Total (hours)
RTAX2000S	CQ352	D1L9R1	QBI	87	1,000	0	2	85,000
RTAX1000S	CQ352	D1GAH1	QBI	98	1,000	0	4	94,000
RTAX1000S	CQ352	D1GAH1	QBI	78	1,000	0	1	77,000
RTAX2000S	CQ352	D1N9H1	QBI	6	1,000	0	0	6,000
RTAX2000S	CQ352	D2S8K1	QBI	79	1,000	0	0	79,000

Enhanced Antifuse Qualification (EAQ)

All Actel radiation-tolerant FPGAs are qualified in accordance with the MIL-STD-883 Class B specification prevailing at the time of qualification. The procedures described in this document are in addition to the procedures performed in compliance with MIL-STD-883 Class B.

High Stress Test Designs

The test designs employed for RTAX-S enhanced antifuse qualification are specifically designed to isolate antifuse fault mechanisms. They accomplish this by achieving an extremely high utilization factor for logic modules and by implementing a variety of test structures, which thoroughly exercise all of the various antifuse types. The test designs are extremely sensitive to small changes in net propagation delay, which could be caused by a change in the impedance of an antifuse. Such an impedance change could indicate damage in that antifuse. Note that Actel may modify the high stress test designs without notice in order to achieve higher levels of antifuse coverage or better resolution or perception of timing changes.

EAQ Test Method

As a supplement to the MIL-STD-883 Class B qualification procedures for each space-flight FPGA family, a sample of RTAX-S units is programmed with the high stress design, and subjected to a dynamic high temperature operating life (HTOL) test for a minimum of 1,000 hours. The units may be sampled from multiple wafer lots. Additionally, multiple part types within the RTAX-S device family being qualified may be sampled.

The purpose of the EAQ test is to determine the antifuse failure rates. It should be noted that when there are no antifuse failures it becomes impossible to define an antifuse fault. The EAQ test is used to gather information on the long-term reliability of the antifuses used in RTAX-S FPGAs and to perform reliability testing beyond the requirements of MIL-STD-883 Class B. Table 5 through Table 8 list the test conditions and results for the EAQ tests performed, since inception of the procedure.

Table 5: **EAQ HTOL Results**

Device	Units	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTAX1000S	384	10336	944064	0	T_J = 132ºC, V_{CCA} = 1.6 V, V_{CCI} = 3.6 V
RTAX2000S	341	9680	222520	0	T_J = 132ºC, V_{CCA} = 1.6 V, V_{CCI} = 3.6 V
RTAX250S	200	336	33860	0	T_J = 132ºC, V_{CCA} = 1.6 V, V_{CCI} = 3.6 V
Total	925	20352	12000444	0	

Table 6: **EAQ LTOL Results**

Device	Units	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTAX1000S	292	250	73000	0	T_J = –54ºC, V_{CCA} = 1.6 V, V_{CCI} = 3.6 V
RTAX2000S	78	168	13104	0	T_J = –54ºC, V_{CCA} = 1.6 V, V_{CCI} = 3.6 V
Total	370	418	86104	0	

Table 7: **HSB HTOL Results for RTAX-S Space-Flight FPGAs**

Device	Units Tested	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTAX1000S	398	1,000	298,000	0	T_J = 132ºC, V_{CCA} = 1.60 V V_{CCI} = 3.6 V

Table 8: **HSB LTOL Results for RTAX-S Space Flight FPGAs**

Device	Units Tested	Hours	Device-Hours	Antifuse Failures	Test Conditions
RTAX1000S	298	250	74,500	0	T_J = –54ºC, V_{CCA} = 1.60 V V_{CCI} = 3.6 V

No antifuse faults were observed during the HTOL or LTOL testing of the RTAX-S FPGAs.

Enhanced Lot Acceptance (ELA)

In addition to enhanced qualification procedures for the RTAX-S FPGAs, Actel has also implemented supplementary testing performed on a per-wafer-lot basis, in order to ensure that no process-dependent antifuse fault mechanisms are present. The ELA tests are supplementary, and are performed in addition to the lot acceptance tests and screens that are performed on non space flight FPGAs.

There are three types of enhanced lot acceptance screening:

- Cross-section analysis of samples from each wafer
- High-temperature operating life (HTOL) test of units sampled from each wafer lot
- Thermal runaway characterization test of two units sampled from each wafer lot.

ELA Cross Section Analysis

In order to ensure that there are no construction issues which may lead to reliability problems, two dice are sampled from each wafer of incoming RTAX-S FPGAs. The dice are cross sectioned and a sample of electron micrographs are inspected by technology experts in the Actel Technology Development (TD) group. Any construction issues observed by the TD team will result in the wafer in question being quarantined until its reliability can be assured by more detailed testing.

Programming Software Revision

Actel has further enhanced traceability by recording the version of the Silicon Sculptor software used by the customer to program RTAX-S devices. Actel records this information on the unit during the programming process. This is very valuable information when debugging any Failure Analysis (FA) cases that get reported.

Thermal Runaway Characterization Test

As process nodes get smaller and geometries decrease, the transistors have a lower threshold as to when a device can get into thermal runaway. RTAX-S is based on a 0.15 µ process and as a result can reach a thermal runaway state at a smaller junction temperature than the earlier generation RTSX-SU 0.22 µ process based product. Given this expectation, Actel has taken two major steps to ensure that RTAX-S wafers do not go into thermal runaway. One of the steps is reduce the specification for the junction temperature of the product from 150°C to 125°C,which is typical for 0.15 µ CMOS process (as stated in the *RTAX-S/SL Family FPGAs* datasheet). The second step is to institute a thermal characterization test as part of the production process starting with wafer lots fabricated in 2007 and beyond. In this test, two units from every wafer lot are tested at ambient temperatures up to 135°C to characterize the device thermal stability at temperatures higher than the 125°C junction temperature. Any units that exhibit thermal runaway (sharp and uncontrollable increase of ICC current at high temperature) are scrapped along with the wafer lot.

ELA HTOL Test

A high temperature operating life test is performed on a sample from each wafer lot of RTAX-S FPGAs.

ELA HTOL Test Design

The design used during ELA testing will, in most cases, be identical to the high stress design used for EAQ. The objective of the design is to exercise as many different antifuses of as many different types as possible and to observe timing changes with resolution as fine as possible. In order to optimize resolution and coverage, Actel may change or update the ELA test design without notice.

ELA HTOL Test Method

The enhanced lot acceptance testing requires that a sample of packaged units be removed from the first assembly lot from each wafer lot of RTAX-S space-flight FPGAs. The sample size is determined by the product type. The larger RTAX-S parts are sampled at a lower rate, since there are fewer parts per wafer lot. The RTAX2000S is sampled at a minimum of 14 after allowing for a maximum of 3 programming failure units, RTAX1000S at a minimum of 24 after allowing for a maximum of 4 programming failure units, and the RTAX250S at a minimum of 100 units per wafer lot after allowing for a maximum of 10 programming failure units. The sampled units are subjected to HTOL testing for a minimum of 168 hours, operating at a junction temperature of 125ºC. After the HTOL, a full electrical test is performed on the sampled units at room temperature. This testing will be performed in parallel with the production screening process for the flight units, and must be completed prior to shipment of flight units from the wafer lot. Any failures detected during the electrical test will be subjected to a full fault analysis. If faults are encountered, the lot will be put on hold, pending resolution of the fault analysis. During this time, no customer shipments will be made from the lot.

ELA HTOL Results

Table 9 presents a sample of the results from the enhanced lot acceptance testing performed on the RTAX-S product families since inception of the enhanced procedure. The results in Table 9 show that the ELA data. The 1.93 million total device hours includes all qualification tests, Group C testing, and customer specific life tests.

Table 9: **ELA Results for RTAX-S Space-Flight FPGAs**

Product	Package	Wafer Lot Number	Group	Units	Bi (Hours)	Antifuse Failures	Other Failures	Total Hours
RTAX2000S	CG1152	D1PPY1	ELA	6	1000	0	0	6000
RTAX2000S	CQ352	D1GAG1	ELA	14	168	0	0	2352
RTAX2000S	CQ352	D1N9H1	ELA	14	168	0	0	2352
RTAX2000S	CQ352	D21PH1	ELA	14	168	0	0	2352
RTAX1000S	CG624	D1KH51	ELA	24	168	0	0	4032
RTAX1000S	CG624	D1KH51	ELA	37	1000	0	0	37000
RTAX1000S	CQ352	D1KH51	ELA	8	1000	0	0	8000
RTAX2000S	CQ352	D1R0G1	ELA	14	168	0	0	2352
RTAX2000S	CQ352	D1L9R1	ELA	14	168	0	0	2352
RTAX2000S	CQ352	D1NSG1	ELA	14	168	0	0	2352
RTAX2000S	CQ352	D1PPY1	ELA	14	168	0	0	2352
RTAX250S	CQ352	D1H381	ELA	100	168	0	0	16800
RTAX2000S	CQ352	D1N9H1	ELA	14	168	0	0	2352
RTAX2000S	CQ352	D1KHN1	ELA	58	1000	0	0	58000
RTAX2000S	CQ352	D1R0G1	ELA	20	1000	0	0	20000
RTAX2000S	CQ352	D1KHN1	ELA	58	168	0	0	9744
RTAX2000S	CQ352	D1R0G1	ELA	20	168	0	0	3360
RTAX1000S	CQ352	D1NR91	ELA	24	168	0	0	4032
RTAX2000S	CQ352	D1KHN1	ELA	14	168	0	0	2352
RTAX250S	CQ352	D1M6K1	ELA	100	168	0	0	16800
RTAX2000S	CG624	D2S8M1	ELA	14	168	0	0	2352

FIT Rate Calculation

There have been no antifuse faults observed in testing to date. Designs that have been used for testing are similar to the ones that were used to detect the low level fault rate of highly stressed antifuses in SX-A and RTSX-SU products. These highly perceptive designs have not shown a single antifuse fault on the RTAX-S product. With the data from the above testing, which included a total of 1.93 million device hours of HTOL from the Qualification Burn-In (QBI), Enhanced Antifuse Qualification (EAQ), and Enhanced Lot Acceptance (ELA) experiments, a CMOS FIT has been calculated based on the chi-square distribution with a minimum upper confidence limit of 60% per JESD74 and an activation energy of E_a = 0.7 eV. The CMOS FIT rate is FIT = 10.74 at 55ºC.

Conclusions

Actel has recently implemented enhanced procedures for the qualification and lot acceptance of the radiation-tolerant antifuse RTAX-S FPGAs for space-flight applications. Results obtained from the testing required by these enhanced procedures demonstrate the high reliability of Actel RTAX-S space-flight FPGAs. This report will be updated with the results of tests on additional wafer lots as they become available. Actel also intends to pursue QML V flow certification for the RTAX-S products once the process has been defined and put in place.

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