High-Volume nano FPGAs

Going Where no FPGA Has Gone Before

White Paper

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Introduction

Though once a novelty, electronic devices are now ubiquitous and a necessary part of every day life. From the boardroom to the operating room to the classroom, demand is up for electronic devices that help us work faster and more efficiently. The drive toward miniaturization and integration is transforming electronic devices into consumer commodities at an alarming rate. Gadgets we once placed on a desk or carried in a briefcase now fit comfortably in a shirt pocket. Even industrial, medical, and military markets, which have previously been low-volume, are shifting to the consumer-based model: higher volume production of smaller systems that perform better and cost less.

Demand for everything from cell phones to printers, insulin infusion pumps to hand-held GPS units, is on the rise. And complicating the market is the growing demand in more recently developed countries for the digital life style. Increased consumer spending power in countries like China, India, and Brazil is driving development, innovation, and customization in many electronic systems markets. Manufacturers have almost insurmountable challenges in meeting market demand and competition for new technology.

The perfect storm of consumer demand converging with design constraints is on the horizon. More demand for electronic devices means more demand for semiconductors. Time-to-market for high-demand products must be slashed. Design lead times have met the same fate. Design teams are squeezed between a rapidly changing market and the inherent limitations of their design processes. They are reaching the limits of current technology with no clear alternative.

Design Trends

In the early 1990s, performance was the most important design requirement. Design teams focused on wringing every last clock-cycle of performance out of a design. Cost was considerably lower on the requirements list, followed by Power.

By the turn of the century, performance was tuned to such a degree that further improvements either came at too great a development cost, or were not of much benefit to users. So cost replaced Performance atop the design requirements list. Performance fell to the bottom, and power was sandwiched in the middle. Satisfied with performance, users now wanted affordability.

Enter today. Power considerations take the lead in most design requirements. With performance and affordability addressed, users want long-lasting portability without being tethered to a battery charger. Lower power is the new design mantra, followed by small size and continued affordability. Performance has dropped out of the top three design considerations altogether.

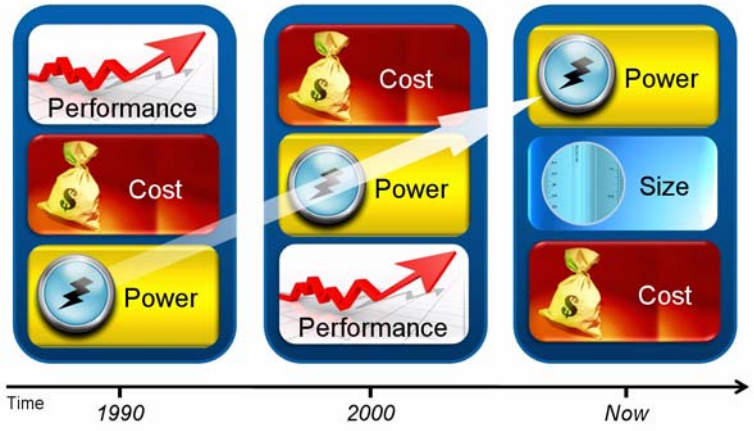

Figure 1: **Trends in Electronic Design, 1990 to Present**

Traditional Technologies

Historically, high-volume electronic systems have depended on one of two semiconductor technologies: application-specific standard products (ASSPs) and application-specific integrated circuits (ASICs). ASSPs are standard, off-the-shelf components that perform a specific function and appeal to a broad market. As an example, consider an integrated circuit (IC) that encodes/decodes audio or video data. ASICs, on the other hand, are single-chip solutions for very specific applications and are most likely developed for a specific customer. Think cell phone ASIC, where each mobile phone company requires specific features.

While the advantages of these design technologies include focused functionality and application customization, their drawbacks in a competitive, rapidly changing market make them almost impractical to use. Shortened time-to-market barely allows for a single design spin of a custom IC, let alone multiple spins to fix errors. And shortened product life cycles make it difficult for manufacturers to recoup their non-recurring engineering (NRE) costs, making actual profit impossible. Added to this expense are the often overlooked product life cycle costs that extend beyond design and production. Many systems will need upgrading during their service life, a challenge for the traditional custom integrated circuit development processes. Manufacturers must rethink their approach, not only to product design, but also to the entire product life cycle.

Programmable Approach

Success in today's competitive, high-volume production landscape is all about responding quickly to market demands. Electronic device manufacturers that react quickly to changing markets will succeed. To shorten time-to-market, design teams need an efficient design approach that supports fast design and prototyping, short component lead times, and the ability to easily upgrade features once the device is in use.

Enter the field-programmable gate array (FPGA). An FPGA contains multiple programmable logic blocks and a network of customizable interconnects for connecting the blocks together. Design teams program the FPGA by connecting logic blocks to perform specific functions. While FPGA history goes back to the mid-1980s, only recent advances in design and process technology have made high-volume use possible.

In general, FPGAs give design teams two key benefits: flexibility and fast time-to-market. Flexibility comes from enabling quick prototyping of multiple design options. Since designers are simply reprogramming an integrated circuit instead of respinning silicon, tweaking and debugging a design takes place in a fraction of the time required for an ASIC-based approach. A shortened design cycle translates to a faster time-to-market. Faster to market means a larger market share. And once a system is in use, upgrades are a simple matter of reprogramming the FPGA; no hardware changes are required. In short, an FPGA can be programmed to perform any function an ASIC can do, with the added benefit that changes can be made after a device is shipped and in use.

Despite their utility, however, FPGAs have a couple of drawbacks. Traditionally, FPGAs have relied on static random access memory (SRAM) technology, resulting in a large FPGA footprint and high power draw. These drawbacks alone preclude using FPGA technology in high-volume portable electronic device applications. Without revolutionary advances in FPGA technology, their utility in portable applications is limited. Fortunately, Actel Corporation has the answer.

Table 1: **Actel's Low-Power Flash Families**

IGLOO® Series			ProASIC®3 Series		
Industry's Lowest-Power FPGAs			Low-Power FPGAs		
IGLOO/e	**IGLOO PLUS**	**IGLOO nano**	**ProASIC3/E**	**ProASIC3L**	**ProASIC3 nano**
The ultra-low-power, programmable solution	The low-power FPGA with enhanced I/O capabilities	The industry's lowest power, smallest size solution	The low-power, low-cost, FPGA solution	The FPGA that balances low power, performance, and low cost	Lowest cost solution with enhanced I/O capabilities

Actel leads the market in developing highly functional, low-power, flash-based FPGA technology. Design teams have successfully used Actel's IGLOO and ProASIC3 product lines in a broad range of applications.

Actel's nano FPGA Technology

Actel's nano FPGAs aggressively drive flash technology improvements in five key areas: nanoPower, nanoSize, nanoLead-Time, nanoTemp, and nanoPrice.

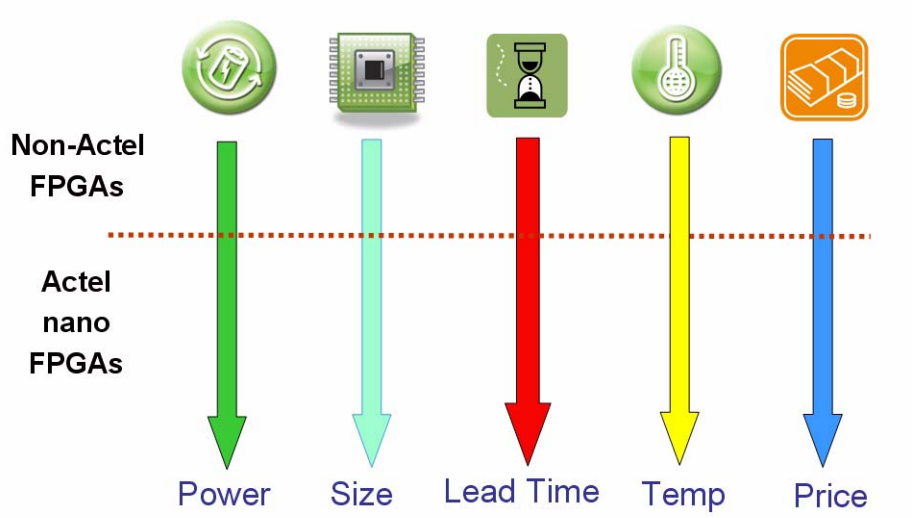

Figure 2: **Actel's nano FPGAs Drive FPGA Technology**

Actel nano FPGAs add two new product lines to the IGLOO and ProASIC3 FPGA families: IGLOO nano and ProASIC3 nano.

Table 2: **Actel's nano FPGA Features**

Product	Logic Densities	I/Os	System Perform.	Core Voltages	I/O Voltages	Typical Static Power	Power Modes	Packages	RAM	User NVM	PLL
IGLOO nano	10 k–250 k	34–71	200–250 MHz	1.2 V–1.5 V	1.2 V–3.3 V	2 µW	Flash*Freeze	µCS, CS QFN, QFP	Up to 36 kb	1 kb	Up to 1
ProASIC3 nano	10 k–250 k	34–71	350 MHz	1.5 V	1.5 V–3.3 V	3 mW	Sleep	QFN, QFP	Up to 36 kb	1 kb	Up to 1

nanoPower

Actel's nano FPGA devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. Both the IGLOO and ProASIC3 nano devices feature a very limited power-on current surge and no high-current transition period, both of which occur in many FPGAs.

IGLOO nano FPGAs utilize design and process techniques to minimize power consumption in all modes of operation. With power consumption as low as 2 µW, IGLOO nano FPGAs range in densities from 10 k to 250 k system gates. These devices support 1.2 V to 1.5 V core and I/O operation, ultra-low-power Flash*Freeze mode with bus hold capability, as well as advanced I/O features, such as hot-swapping and Schmitt trigger inputs.

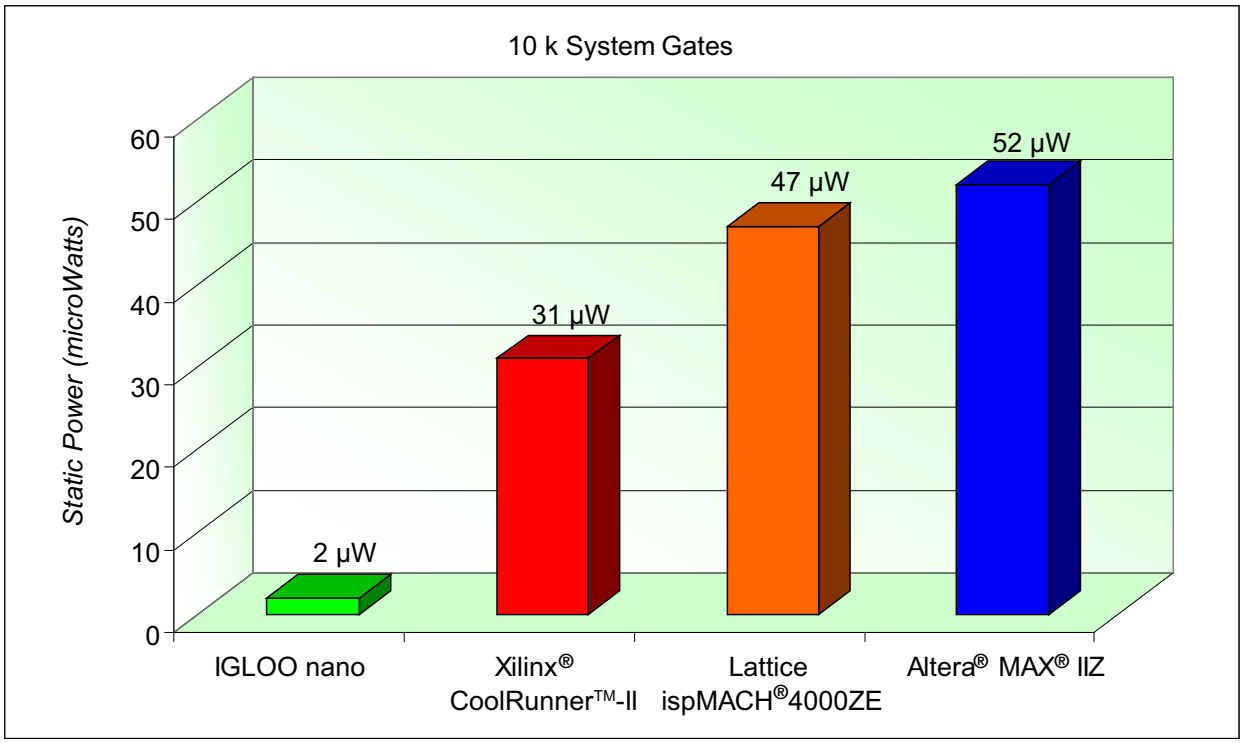

Figure 3: **Actel's IGLOO nano FPGAs are Lower Power by 15 – 25x**

nanoSize

Achieving a significant milestone for the industry, Actel offers its low-power IGLOO nano FPGAs in a 3x3 mm footprint, the smallest package available for any programmable logic device on the market. This tiny package complements Actel's existing portfolio of small packages (4x4 to 8x8 millimeters) and makes IGLOO nano FPGAs the ideal choice for power-sensitive, space-constrained handheld devices.

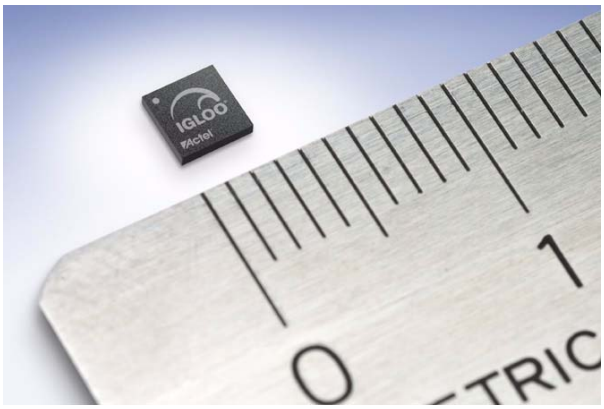

Figure 4: **Actel's IGLOO nano in a 3 x 3 mm UC36 Micro Chip-Scale Package**

nanoLead-Times

Both IGLOO nano and ProASIC3 nano FPGAs, in densities of 60 k, 125 k and 250 k gates, are immediately available in volume with zero lead times. Design teams also have immediate access to known good die, offering size and cost benefits as well as design integration advantages.

nanoTemp

Actel enhanced its standard commercial ambient operating temperatures, offering new ranges for IGLOO nano FPGAs from –20°C to +70°C. Many portable applications can now operate in sub-zero environments around the world.

nanoPrice

In high volume, pricing for the 10-k-gate A3PN010 device starts at $0.69 in a QNG48 package and $0.49 in known good die. Actel offers over 50 product variants under $1 for high-volume applications.

Known Good Die Support (KGD)

Known good die (KGD) use is common in the semiconductor industry. Using KGDs, design teams develop multi-chip modules (MCMs) or a stacked die by combining dies from different vendors to meet an application's size and feature requirements. The result is higher system integration combined with FPGA flexibility.

The IGLOO and ProASIC3 nano FPGA product lines employ nonvolatile, reprogrammable, flash-based technology, which enables KGD support—a unique offering in the programmable logic market. The capabilities of flash-based FPGA technologies enable the implementation of a live-at-power-up, single-chip, small-footprint die in a reprogrammable, easy-to-use device.

Actel's Flash-Based FPGAs

All nano FPGAs are based on Actel's industry leading flash-based FPGA technology. The following sections describe some of the key features of Actel's flash-based FPGAs:

Advanced Flash Technology

Actel's flash-based FPGA technology offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process. Standard CMOS design techniques implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches enables very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Flash*Freeze Technology

Actel's IGLOO FPGAs offer unique Flash*Freeze technology, allowing a device to enter and exit ultra-low-power Flash*Freeze mode. No external components are needed to turn off I/Os or clocks while retaining the design information, SRAM, and register content. Unlike SRAM-based FPGAs, IGLOO devices internally retain all necessary information to resume operation immediately (within 1 µs). In IGLOO nano and IGLOO PLUS FPGAs, I/Os can be individually configured to either hold their previous state or be tristated during Flash*Freeze mode. Flash*Freeze technology is combined with in-system programmability, giving design teams the capability to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field.

User Nonvolatile FlashROM

IGLOO and ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks. The FlashROM can be programmed via the JTAG programming interface, and its contents read back either through the same interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface, not from the internal logic array.

Single Chip

Flash-based FPGAs store configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Flash-based FPGAs, therefore, do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. The result: shorter bill-of materials, smaller PCB footprint, increased security, and better system reliability.

Live at Power-Up (LAPU)

Actel's flash-based FPGAs support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based FPGA devices greatly simplifies total system design and reduces total system cost. In addition, glitches and brownouts in system power will not corrupt the device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. Design teams can simplify PCB design by reducing or eliminating requirements for configuration PROM, voltage monitoring, and clock generation.

Security

Because nonvolatile, flash-based FPGAs do not require a boot PROM, there is no vulnerable external bitstream that can be easily copied. IGLOO and ProASIC3 FPGAs incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer. Actel's devices utilize a 128-bit flash-based FlashLock and a separate AES key to secure programmed intellectual property and configuration data. In addition, FPGA configuration and FlashROM data can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. Actel FPGAs have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. Actel's IGLOO and ProASIC3 product lines with AES-based security enable secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of IP thieves.

Actel's flash-based FPGAs offer a secure technology compared to ASICs, which can be reverse-engineered by removing metal layers and revealing the design.

Reduced Cost of Ownership

Reduced cost is realized through tangible benefits such as reduced part count and remote serviceability. Unlike SRAM-based FPGAs, Actel's flash-based FPGAs allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all programming information and enable secure remote updates of the FPGA logic. Designers can perform secure, remote, in-system reprogramming to support future design iterations and field upgrades. Actel's nano FPGAs mitigate the need for ASIC migration at high production volumes with cost-effective replacement solutions.

Conclusion

Electronic devices have found their way into every aspect of daily life. This popularity is driving demand for more portability and higher integration. While demand is increasing, design teams are challenged with meeting shorter time-to-market demands in their current design processes. Traditional ASIC and ASSP design technologies are limited by the time and cost required not only in the initial design, but also in upgrades and updates once a system is in use. FPGAs address these limitations, giving design teams a system development platform that is fast, flexible, and cost effective. Using FPGAs, design teams can implement a design in a fraction of the time, and at a fraction of the cost required for the traditional custom IC approach. Actel's industry-leading, low-power, flash-based FPGA technology enables the efficient design, manufacture, and maintenance of high-volume electronic devices. With nanoPower, nanoSize, nanoLead-times, nanoTemp, and nanoPrice, IGLOO nano and ProASIC3 nano products bring the advantages of flash-based FPGA technology to the high-volume, small form factor, portable electronic device market. Actel's nano FPGAs can truly go where no FPGA has gone before.

Related Documents

Product Briefs

IGLOO nano Low-Power Flash FPGAs

www.actel.com/documents/IGLOO_nano_PB.pdf

ProASIC3 nano Flash FPGAs

www.actel.com/documents/PA3_nano_PB.pdf

Handbook Chapters

*Actel’s Flash*Freeze Technology and Low-Power Modes*

www.actel.com/documents/LPFPGA_FS_PIB.pdf

Brochures

Industry’s Lowest Power FPGAs

www.actel.com/documents/LPFPGA_FS_PIB.pdf

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at www.actel.com.

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