The Many Flavors of Low-Power, Low-Cost FPGAs

Motivated by the belief that people should have a choice, Baskin-Robbins, a global chain of ice cream parlors, opened in 1945 with 21 flavors, an innovative concept at the time. In 1953, the store kicked off its famous "31 Flavors" slogan, representative of a flavor for every day of the month. More than 60 years later, the chain now offers more than 1,000 unique flavors of ice cream.

For today's designers using programmable logic, the unrelenting claims of low-power leadership can be as confusing as walking into Baskin-Robbins, only to find out all the tags have been removed from the containers. You peer through the glass, trying to discern what is in each one. You spot vanilla, but is it regular, French, or sugar-free?

What is the difference between the offerings? How can you determine the best "low-power" field-programmable gate array (FPGA) for your power- and cost-sensitive application? As with most engineering decisions, the final answer depends greatly on your specific design constraints, among which are likely to be power, performance (or speed), logic, and I/O count. The final choice of the most suitable FPGA device for your application is usually best framed in the context of these requirements.

A Proliferation of Power- and Cost-Sensitive Design

The tremendous growth in battery-operated and power-sensitive applications has created a global demand for low-power semiconductors. Today's power-sensitive designers face stricter system power limits, specifications, and standards that put a cap on the total power consumed by the system. Simultaneously, for these applications, the demand for increased features, performance, and complexity continues to grow, but not at the expense of draining the battery or increasing costs.

Designers have traditionally relied on application-specific integrated circuits (ASICs), not FPGAs, to meet their low-power constraints. With longer time-to-market, rising non-recurring engineering charges (NREs), and a lack of flexibility to address changing standards and late-stage design modifications, hardwired ASICs are riskier and often impractical for applications with short product life cycles. As a result, PLDs are becoming the preferred solution as competition intensifies and time-to-market has an increasingly greater impact on product success. In fact, more and more, designers are finding that a low-power, reprogrammable solution is required to adapt to evolving standards, speed time-to-market, and deliver the footprint and power consumption required for the next cutting-edge silicon solutions. Market research firm iSuppli predicts as much as $3 billion of the estimated $20 billion ASIC market could potentially shift to low-power FPGA solutions.

The Many Flavors of "Low-Power" FPGAs

Certainly not all programmable logic is well-suited to address low-power needs. In fact, some of today's "low-power" FPGAs draw upwards of 30 mA, which is often an order of magnitude or two higher than typical power-sensitive, battery-operated applications can tolerate. At start-up, SRAM-based devices experience well-documented inrush and boot-up configuration power spikes during system initialization that can cause excess battery drain. Alternately, single-chip, flash-based devices do not require an external configuration device (i.e., boot PROM or microcontroller) to support device programming at every power-up cycle, and the live-at-power-up feature eliminates the need for an external device to assist in system power-up. Removing the additional parts required by SRAM-based FPGAs not only reduces board space and system power consumption, but also increases reliability, simplifies inventory management, and lowers total system costs by as much as 70 percent compared with similar SRAM-based FPGA solutions.

Once the FPGA is on and configured, power consumption takes two basic forms—static and dynamic (also called active). Static power consumption is the current drawn by your FPGA when it is powered up, configured, and doing nothing; dynamic power is consumed when devices are actively working. Until recently, dynamic power was the dominant source of power consumption. Once helping to manage the dynamic power problem, device supply voltages (V_{CC}) had scaled downward with process shrinks and subsequent lower system voltages, but the days of continued scaling are gone. Compounding the issue further, each process node shrink means additional static power consumption for transistor-heavy SRAM-based FPGAs. This is due to worsening problems such as quantum tunneling and sub-threshold leakage, which create real challenges for devices targeted to power-conscious applications. And, with leakage worsening, static power has begun to dominate the power consumption equation as the biggest concern (Figure 1).
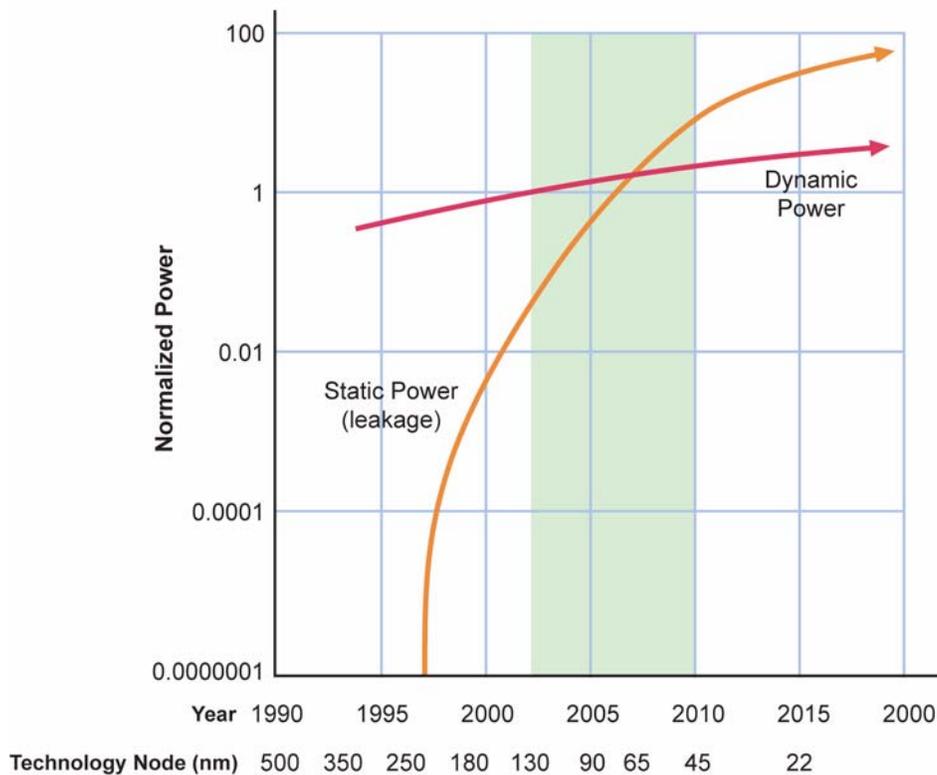

Figure 1: **Static Power Significant at 90 nm**

Figure 1 illustrates the increasing contribution of static power at shrinking process nodes.

To address some of these power concerns, several suppliers of SRAM-based FPGAs claim to offer "single-chip, flash-based" solutions. These "hybrid" solutions are merely combinations of flash memory components with the underlying SRAM FPGA technology—either integrated with the FPGA die into a single package or, alternatively, stacked or placed side-by-side. Unfortunately, the FPGA array is still volatile and is subject to the power drawbacks associated with these types of devices. With these solutions, the embedded flash memory blocks control only the initial configuration of the devices during power-up. True nonvolatile FPGAs are those that contain a nonvolatile FPGA array, enabling significantly reduced power consumption, improving response times, and delivering unparalleled reliability and uncompromising security.

Both the silicon-in-package (SIP) and the multi-chip package (MCP) hybrid approaches overcome some of the limitations of traditional SRAM-based solutions by providing a smaller footprint, a minor reduction in power consumption, and small advances in power-up time and security. But these are only incremental improvements over their pure SRAM-based peers. In some cases, these devices have been proven to consume 1,000 times more static power than true flash-based FPGAs.

Because true nonvolatile flash-based FPGAs do not use millions of power-hungry SRAM configuration bit cells, they have significantly lower static power than SRAM-based solutions, making them ideal for power-sensitive applications. In fact, the many flavors of flash-based, low-cost FPGAs include devices that have been optimized for power, speed, and I/O, some of the fundamental design requirements for power- and cost-sensitive design.

Figure 2 highlights the flavors of flash-based, low-power FPGA families from Actel Corporation.

Figure 2: **Flavors of FPGAs**

Optimized for Power

The industry's lowest power programmable solutions at 5 μW, the Actel IGLOO® family offers between 10 times and 1,700 times less static power, setting a new bar for low power consumption. This significantly lower power consumption can translate into weeks and months of standby battery life.

Figure 3 illustrates the tremendous static power advantage IGLOO has over competitive FPGA devices.
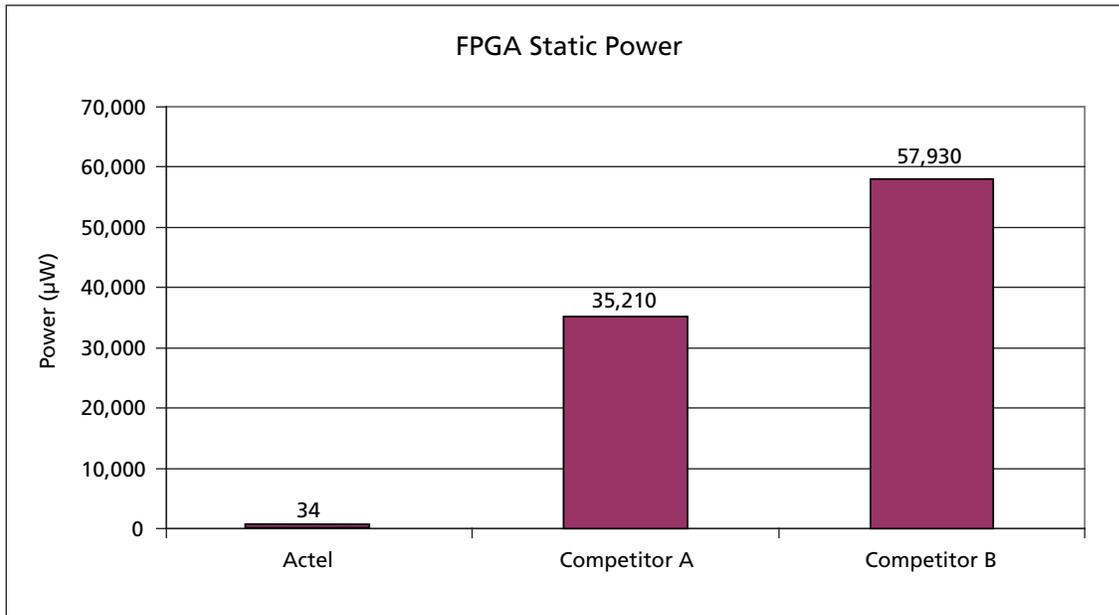
FPGA Static Power

Device	Power (μW)
Actel	34
Competitor A	35,210
Competitor B	57,930

Figure 3: **FPGA Static Power**

The IGLOO family supports up to 250 MHz operation and offers 1.2 and 1.5 V operation, densities up to 3 million system gates, and enhanced features such as PLLs, RAM, and user nonvolatile memory. Additional advantages of the flash-based IGLOO devices include flexible power-saving modes with rapid recovery to operation, low dynamic power consumption, and clock management. Available in a 4-millimeter (mm) package with a 0.4-mm ball pitch, the smallest package for any programmable logic device on the market, IGLOO FPGAs are particularly attractive for applications where the absolute lowest power and smallest size are critically important.

Today's power-sensitive designer attempts to achieve the lowest power possible and to accommodate long system idle times by allowing the system to enter and exit low-power modes quickly. To address this, the Actel IGLOO family employs Flash*Freeze technology to enable power consumption as low as 5 μW while maintaining FPGA content. Further, the Flash*Freeze pin enables designers to quickly and easily enter or exit the special low-power mode within 1 μs. Further, while in Flash*Freeze mode, designers need not power off voltage to the device or stop clocks or I/Os. Additionally, for low-power applications that require 32-bit processing, designers can use the ARM® Cortex™-M1 processor without license fee or royalties in M1-enabled IGLOO devices.

The portable market, in particular, has seen tremendous need for storage, LCDs, and human interface control due to the increasing popularity of personal media players, MP3 devices, PDAs, smart phones, navigation devices, and digital cameras. As a result, Actel offers comprehensive IGLOO-based portable storage and LCD control application solutions, such as development boards, reference designs and intellectual property (IP) cores, to enable rapid design of their portable and power-sensitive applications.

Optimized for Power and I/O

Flash-based, 5 µW Actel IGLOO PLUS FPGAs have been optimized for I/O-intensive applications, particularly those employing I/O-intensive memory bus manipulation, general-purpose I/O expansion, sequencing, interface translation, storage, and human interface touchscreen and keypad technology. Offering the industry's best power-, area-, logic-, and feature-per-I/O ratios in a programmable device for any given package size, an IGLOO PLUS device delivers 6 times better static power consumption, a 50 percent reduction in dynamic power consumption, a 200 percent improvement in I/O density, and as much as 2.7 times the logic density compared with competitive programmable logic solutions in similar packages. For example, a competitive SRAM-based programmable device in an 8 mm x 8 mm chip-scale package offers 25 k equivalent system gates, 78 I/Os, and 25 mW typical static power versus the 60 k system gates, 157 I/Os, and 10 µW of an AGLP060 IGLOO PLUS FPGA in the same package.

Actel IGLOO PLUS solutions also offer up to 16 times better power per I/O. Assuming a design requires 100 I/Os, the 120-I/O AGLP030 IGLOO PLUS device consumes 5 µW versus the roughly 60 µW of the nearest competitive solution.

Figure 4 highlights competitive static power per I/O profiles across 30 k and 60 k density programmable logic devices.
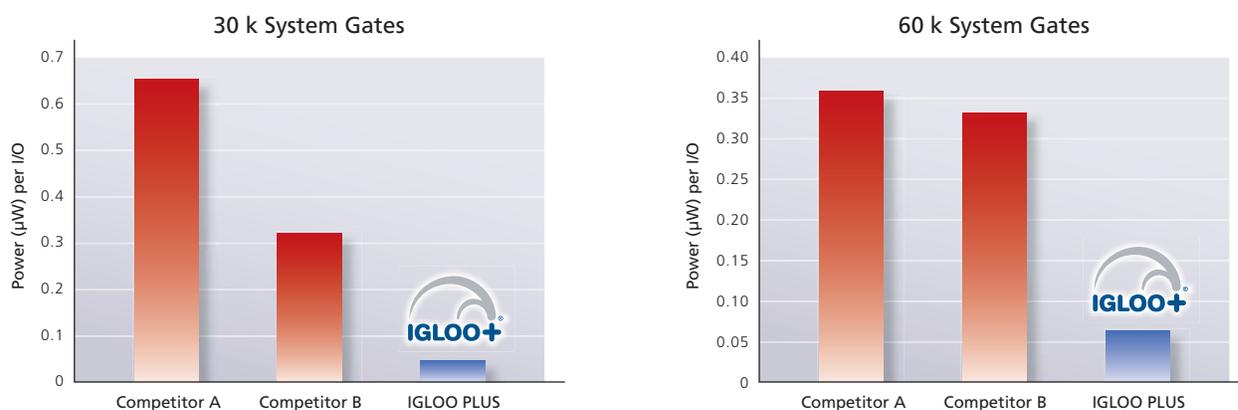

Figure 4: **Competitive Static Power per I/O**

In addition to up to 64 percent more I/Os per device than the company's award-winning IGLOO family, the IGLOO PLUS family also features four I/O banks for independent level shifting. Enabling the device to better support varying voltage levels, this is key for bridging between application processors and application-specific standard products (ASSPs), where differing I/O standards and voltages may be utilized. IGLOO PLUS devices support cost- and area-effective level shifting between 1.2, 1.5, 1.8, 2.5, and 3.3 V I/O standards and interface translation.

Additionally, IGLOO PLUS devices support independent Schmitt trigger inputs and hot-swapping. The Schmitt trigger input delivers greater noise immunity in the circuit, enabling designers to safely identify an input signal that rises slowly, such as a keyboard or human touchpad. The hot-swap capability offers additional flexibility, as designers can now support direct system connection while powering up. This is beneficial for applications such as portable media players and games, where solid state mass storage modules and human interface controllers are often connected to and disconnected from the system in real time.

The IGLOO PLUS family also supports Flash*Freeze bus hold, allowing users to hold the I/O states "on" while the device is in Flash*Freeze mode. In a digital picture frame, for example, the IGLOO PLUS device

can be placed in Flash*Freeze mode to save power and will continue displaying a picture on screen. When the picture needs to be changed, the IGLOO PLUS device can resume operation in a microsecond, having saved hundreds of microwatts of power while in the I/O hold state. This same capability is critical in smart phone, wireless audio, and video applications.

Balancing Power and Speed

For designers of high-performance, power-conscious systems, Actel's ProASIC®3L family of FPGAs combines 40 percent lower dynamic power and 90 percent lower static power than its previous-generation ProASIC3 FPGAs, with up to 350 MHz operation. As a result, designers in high-performance market segments, such as industrial, medical, and scientific, now have access to flexible, feature-rich solutions that offer speed, low power, and low cost.

Dynamic power is critical in applications where clocks are constantly switching and providing input to an FPGA, such as high-speed data pipelines for portable video and medical appliances. Like the company's award-winning 5 µW IGLOO FPGA family, ProASIC3L devices support a 1.2 V core and I/O voltage and Actel's innovative Flash*Freeze technology. Flash*Freeze enables designers to quickly switch the device from dynamic operation to static without switching off clocks or power supplies. In a typical high-speed design using comparable one-million gate FPGAs, SRAM-based competitive solutions consume 60 percent higher dynamic power and 100 times more static power than ProASIC3L devices, which consume just 100 mA of dynamic power and 1 mW of static power.

Figure 5 compares power and performance at one million system gates across competitive "low-power" FPGA solutions.
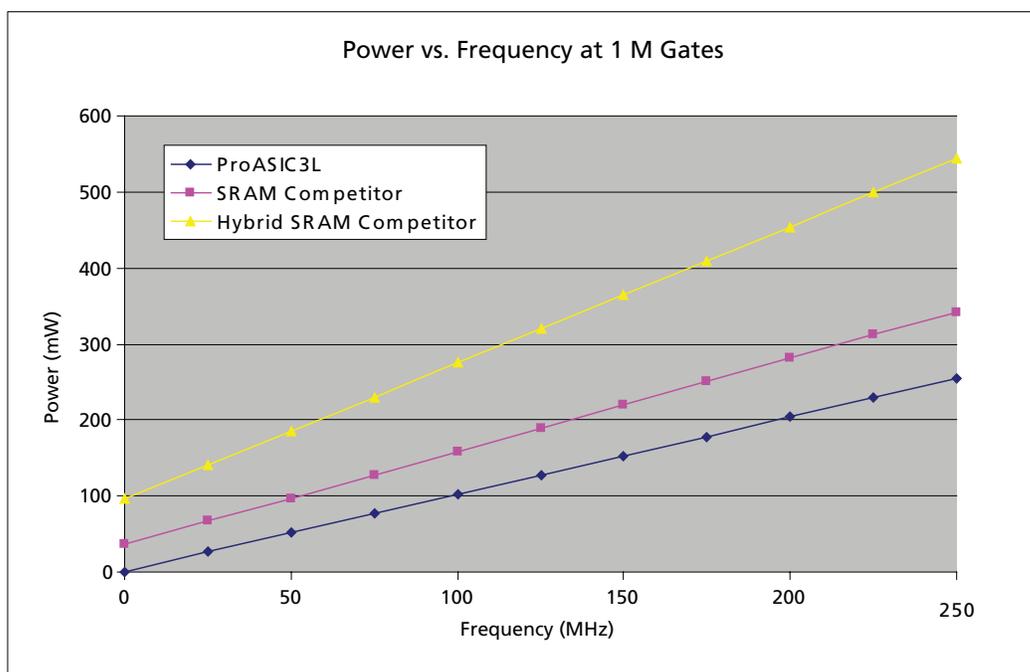

Figure 5: **Power vs. Frequency at 1 Million Gates**

The ProASIC3L family also supports the free implementation of the FPGA-optimized 32-bit ARM Cortex-M1 processor, allowing system designers to select the Actel flash-based FPGA solution that best meets their speed and power design requirements, regardless of application or volume.

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Optimized for Speed

Actel's low-power 1.5 V ProASIC3 FPGAs are optimized for performance. Featuring 350 MHz operation, the one-million-gate ProASIC3 A3P1000 FPGA, for example, delivers standby current consumption of only 8 mA under typical conditions, nearly an order of magnitude lower than competing SRAM-based devices. Further, with pricing as low as $0.99, designers in high-performance market segments, such as industrial, medical, and scientific, now have access to flexible, feature-rich solutions that offer speed, low power, and low cost.

Low-power applications that require 32-bit processing can use the ARM Cortex-M1 processor without license fee or royalties in M1-enabled ProASIC3 devices, providing the benefits of programmability and time-to-market at an ASIC-level unit cost.

Conclusion

For today's designers using programmable logic, determining the best device depends greatly on power, performance, logic, and I/O count design constraints. Like Baskin-Robbins, Actel believes designers should have a choice regarding the best low-power FPGA for their power- and cost-sensitive applications. For this reason, the company has built an attractive portfolio of the industry's most compelling low-power, low-cost FPGAs—a flavor for every palate.

For more information, visit our website at **www.actel.com**

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655
USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwatery
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Building 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
http://jp.actel.com

Actel Hong Kong
Room 2107, China Resources Building
26 Harbour Road
Wanchai, Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

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